TC4451/TC4452

12A High-Speed MOSFET Drivers

Features

- High Peak Output Current: 13A (typ.)
- Low Shoot-Through/Cross-Conduction Current in Output Stage
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Continuous Output Current: 2.6A (max.)
- Matched Fast Rise and Fall Times:
  - 21 ns with 10,000 pF Load
  - 42 ns with 22,000 pF Load
- Matched Short Propagation Delays: 44 ns (typ.)
- Low Supply Current:
  - With Logic '1' Input – 140 µA (typ.)
  - With Logic '0' Input – 40 µA (typ.)
- Low Output Impedance: 0.9Ω (typ.)
- Latch-Up Protected: Will Withstand 1.5A Output Reverse Current
- Input Will Withstand Negative Inputs Up To 5V
- Pin-Compatible with the TC4420/TC4429, TC4421/TC4422 and TC4421A/TC4422A MOSFET Drivers
- Space-Saving, Thermally-Enhanced, 8-Pin DFN Package

Applications

- Line Drivers for Extra Heavily-Loaded Lines
- Pulse Generators
- Driving the Largest MOSFETs and IGBTs
- Local Power ON/OFF Switch
- Motor and Solenoid Driver
- LF Initiator

General Description

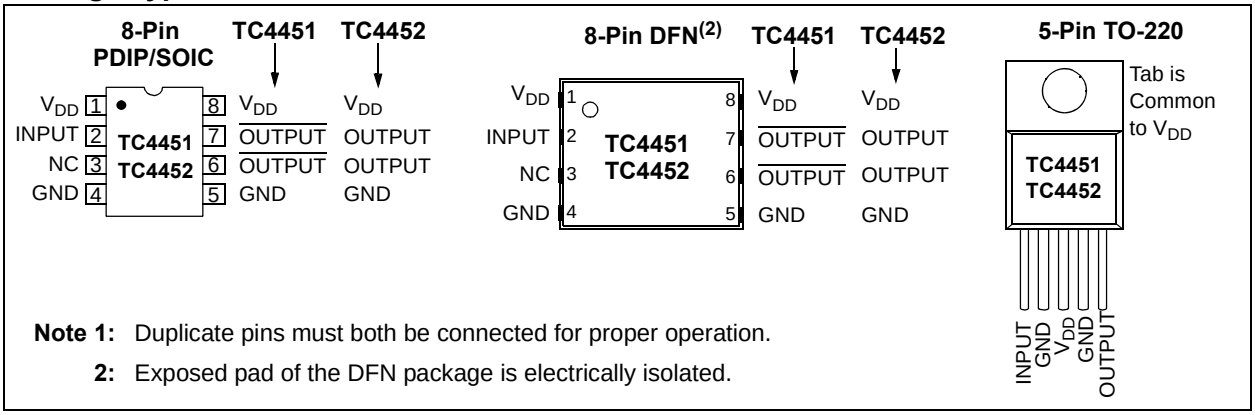
The TC4451/TC4452 are single-output MOSFET drivers. These devices are high-current buffer/drivers capable of driving large MOSFETs and Insulated Gate Bipolar Transistors (IGBTs). The TC4451/TC4452 have matched output rise and fall times, as well as matched leading and falling-edge propagation delay times. The TC4451/TC4452 devices also have very low cross-conduction current, reducing the overall power dissipation of the device.

These devices are essentially immune to any form of upset, except direct overvoltage or over-dissipation. They cannot be latched under any conditions within their power and voltage ratings. These parts are not subject to damage or improper operation when up to 5V of ground bounce is present on their ground terminals. They can accept, without damage or logic upset, more than 1.5A inductive current of either polarity being forced back into their outputs. In addition, all terminals are fully protected against up to 4 kV of electrostatic discharge.

The TC4451/TC4452 inputs may be driven directly from either TTL or CMOS (3V to 18V). In addition, 300 mV of hysteresis is built into the input, providing noise immunity and allowing the device to be driven from slowly rising or falling waveforms.

With both surface-mount and pin-through-hole packages, in addition to a wide operating temperature range, the TC4451/TC4452 family of 12A MOSFET drivers fit into most any application where high gate/line capacitance drive is required.

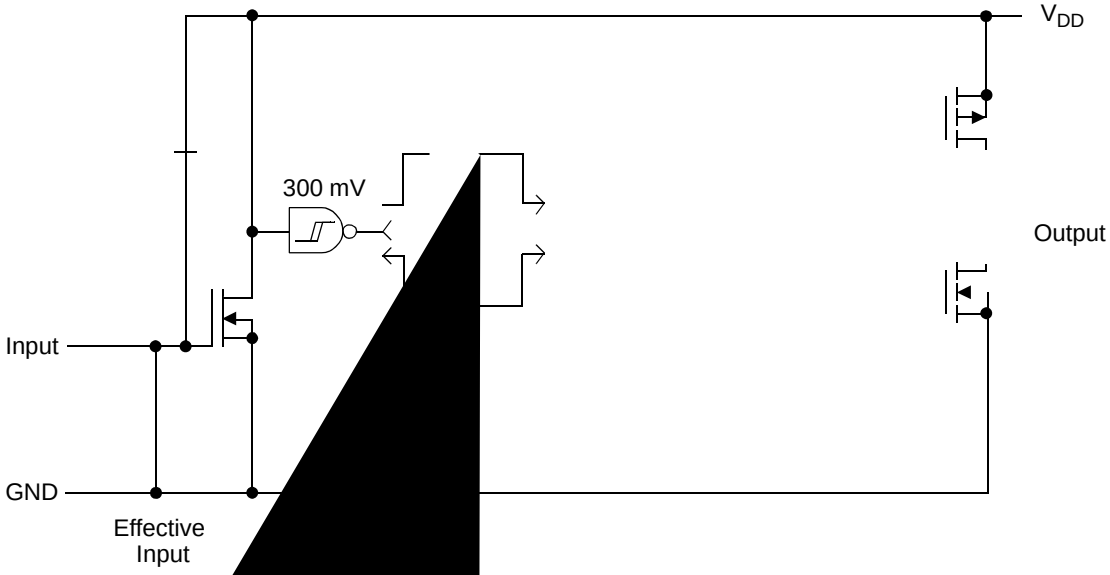
Package Types(1)



Note 1: Duplicate pins must both be connected for proper operation.

2: Exposed pad of the DFN package is electrically isolated.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... +20V
Input Voltage ..... (V_{DD} + 0.3V) to (GND – 5V)
Input Current (V_{IN} > V_{DD}) ..... 50 mA

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	1.5	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Current	I_{IN}	–10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Input Voltage	V_{IN}	–5	—	V_{DD} + 0.3	V	
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	1.0	1.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	0.9	1.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	13	—	A	V_{DD} = 18V
Continuous Output Current	I_{DC}	2.6	—	—	A	10V ≤ V_{DD} ≤ 18V **(Note 2, Note 3)**
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	>1.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µs
Switching Time (Note 1)						
Rise Time	t_R	—	30	40	ns	**Figure 4-1**, C_L = 15,000 pF
Fall Time	t_F	—	32	40	ns	**Figure 4-1**, C_L = 15,000 pF
Propagation Delay Time	t_{D1}	—	44	52	ns	**Figure 4-1**, C_L = 15,000 pF
Propagation Delay Time	t_{D2}	—	44	52	ns	**Figure 4-1**, C_L = 15,000 pF
Power Supply						
Power Supply Current	I_S	—	140	200	µA	V_{IN} = 3V
		—	40	100	µA	V_{IN} = 0V
Operating Input Voltage	V_{DD}	4.5	—	18.0	V	

Note 1: Switching times ensured by design.
2: Tested during characterization, not production tested.
3: Valid for AT and MF packages only. T_A = +25°C.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

Electrical Specifications: Unless otherwise noted, over operating temperature range with 4.5V $\leq V_{DD} \leq$ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	–10	—	+10	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	—	2.2	Ω	I_{OUT} = 10

TEMPERATURE CHARACTERISTICS

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

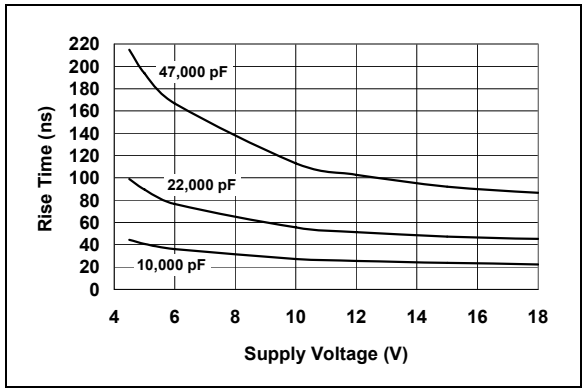


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

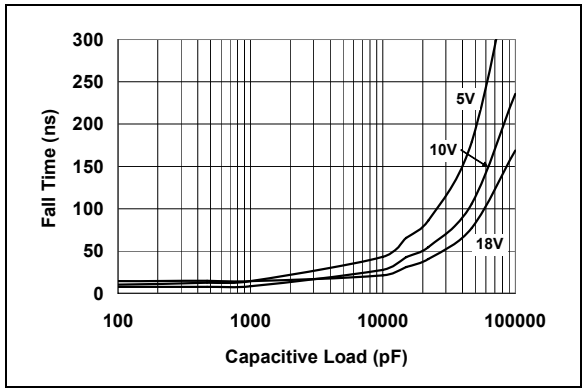


FIGURE 2-4: *Fall Time vs. Capacitive Load.*

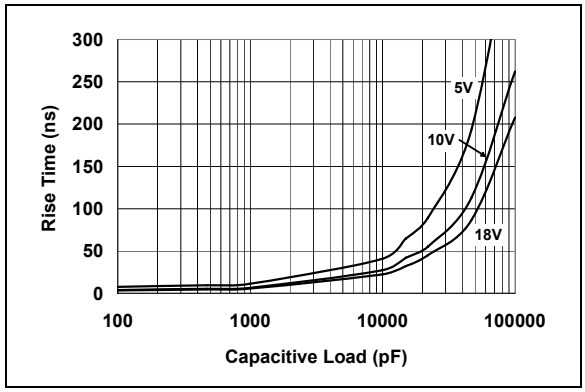


FIGURE 2-2: *Rise Time vs. Capacitive Load.*

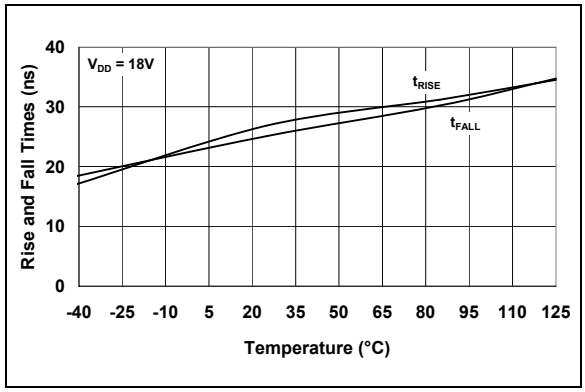


FIGURE 2-5: *Rise and Fall Times vs. Temperature.*

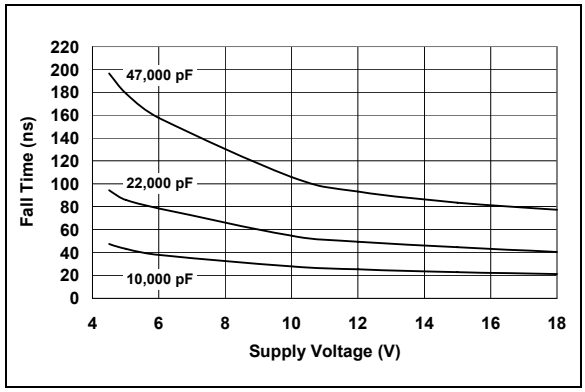


FIGURE 2-3: *Fall Time vs. Supply Voltage.*

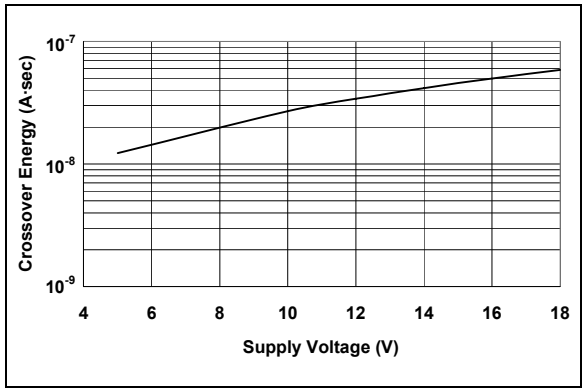


FIGURE 2-6: *Crossover Energy vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

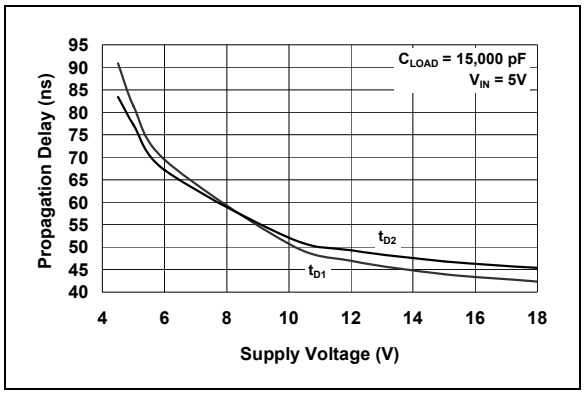


FIGURE 2-7: *Propagation Delay vs. Supply Voltage.*

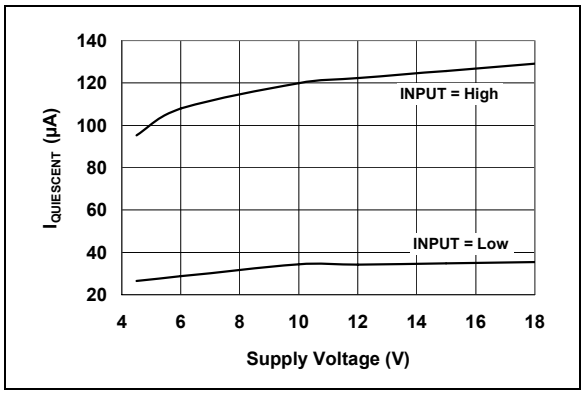


FIGURE 2-10: *Quiescent Supply Current vs. Supply Voltage.*

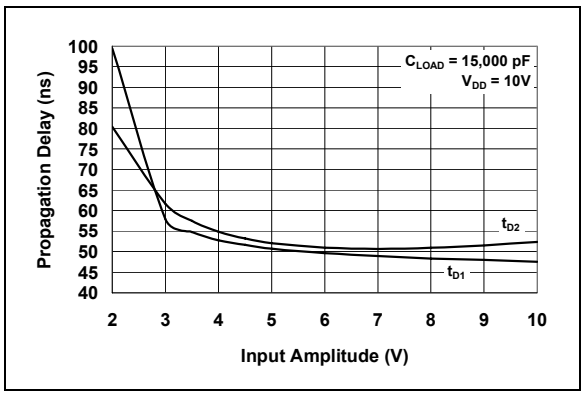


FIGURE 2-8: *Propagation Delay vs. Input Amplitude.*

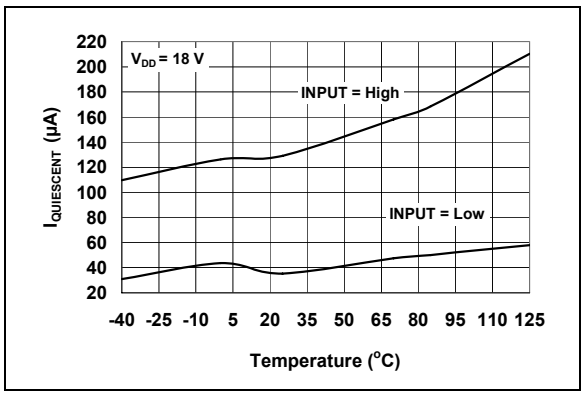


FIGURE 2-11: *Quiescent Supply Current vs. Temperature.*

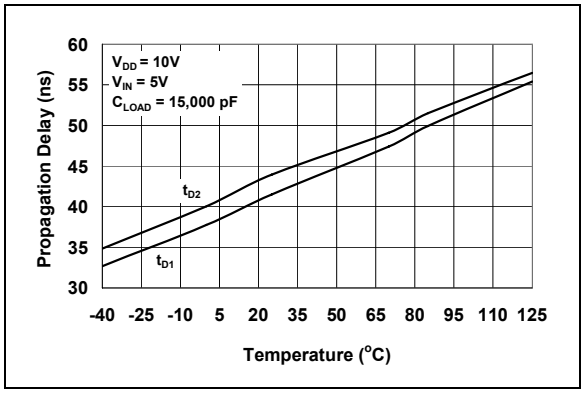


FIGURE 2-9: *Propagation Delay vs. Temperature.*

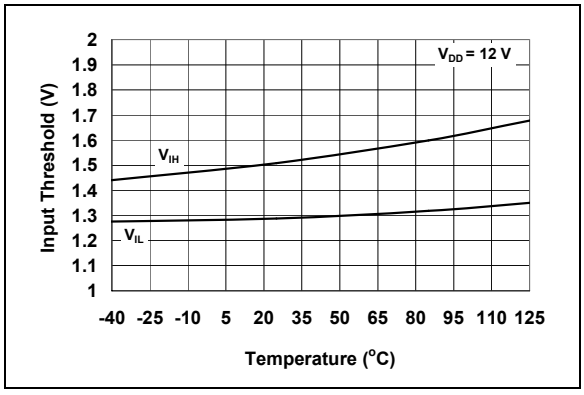


FIGURE 2-12: *Input Threshold vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

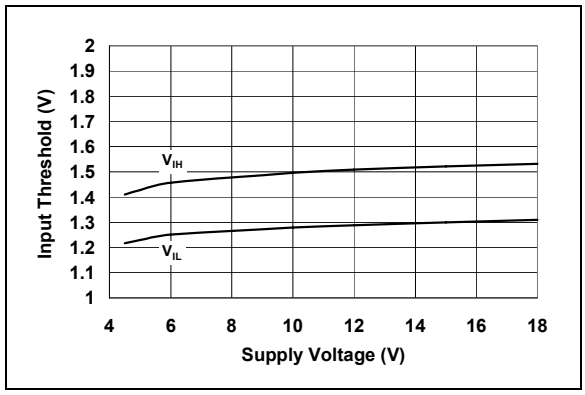


FIGURE 2-13: *Input Threshold vs. Supply Voltage.*

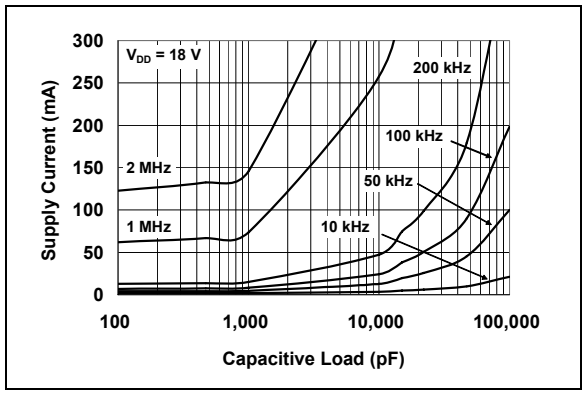


FIGURE 2-16: *Supply Current vs. Capacitive Load (V_{DD} = 18V).*

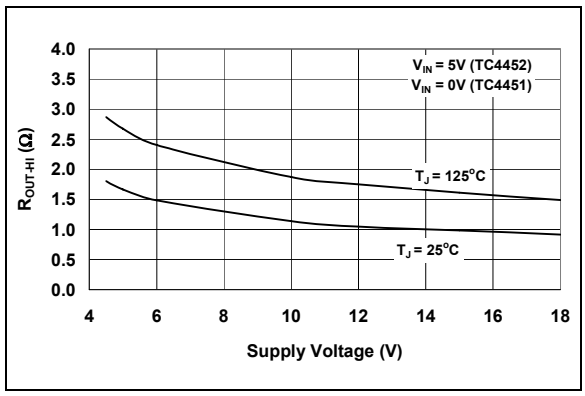


FIGURE 2-14: *High-State Output Resistance vs. Supply Voltage.*

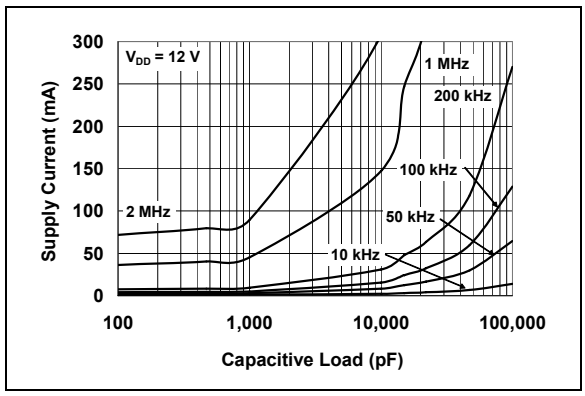


FIGURE 2-17: *Supply Current vs. Capacitive Load (V_{DD} = 12V).*

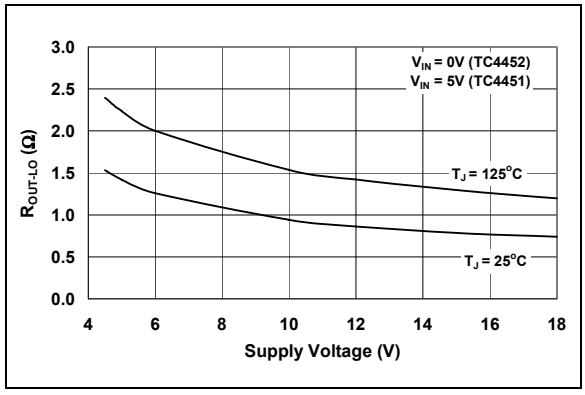


FIGURE 2-15: *Low-State Output Resistance vs. Supply Voltage.*

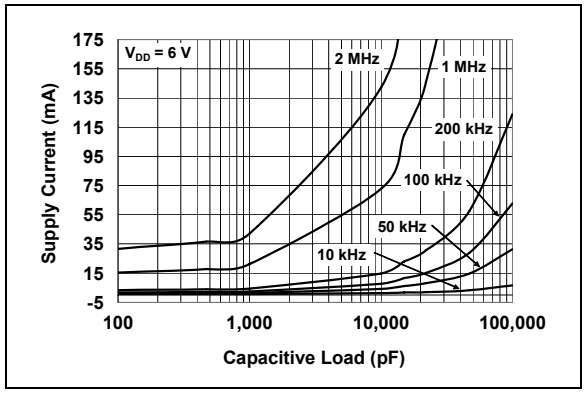


FIGURE 2-18: *Supply Current vs. Capacitive Load (V_{DD} = 6V).*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

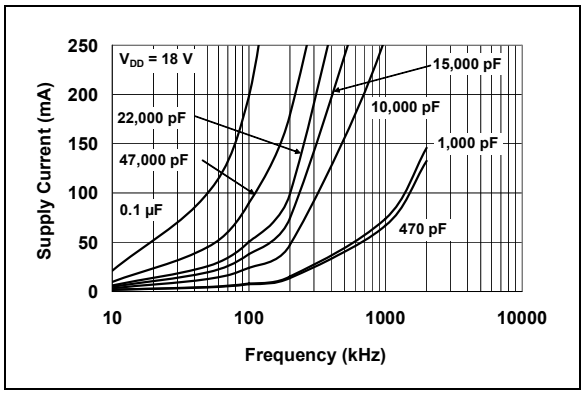


FIGURE 2-19: *Supply Current vs. Frequency (V_{DD} = 18V).*

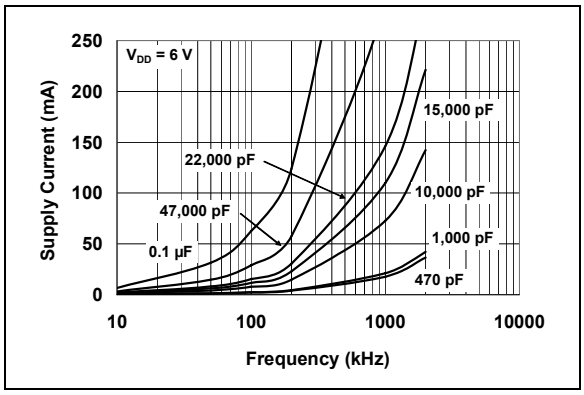


FIGURE 2-21: *Supply Current vs. Frequency (V_{DD} = 6V).*

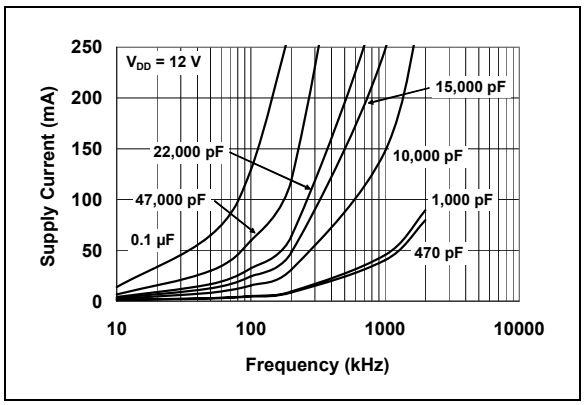


FIGURE 2-20: *Supply Current vs. Frequency (V_{DD} = 12V).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. 8-Pin PDIP, SOIC	Pin No. 8-Pin DFN	Pin No. 5-Pin TO-220	Symbol	Description
1	1	—	V_{DD}	Supply input, 4.5V to 18V
2	2	1	INPUT	Control input, TTL/CMOS-compatible input
3	3	—	NC	No connection
4	4	2	GND	Ground
5	5	4	GND	Ground
6	6	5	OUTPUT	CMOS push-pull output
7	7	—	OUTPUT	CMOS push-pull output
8	8	3	V_{DD}	Supply input, 4.5V to 18V
—	PAD	—	NC	Exposed metal pad
—	—	TAB	V_{DD}	Metal tab is at the V_{DD} potential

3.1 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V with respect to the ground pin. The V_{DD} input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor should be chosen based on the capacitive load that is being driven. A minimum value of 1.0 µF is suggested.

3.2 Control Input

The MOSFET driver input is a high-impedance, TTL/CMOS-compatible input. The input also has 300 mV of hysteresis between the high and low thresholds that prevents output glitching even when the rise and fall time of the input signal is very slow.

3.3 CMOS Push-Pull Output

The MOSFET driver output is a low-impedance, CMOS, push-pull style output capable of driving a capacitive load with 12A peak currents. The MOSFET driver output is capable of withstanding 1.5A peak reverse currents of either polarity.

3.4 Ground

The ground pins are the return path for the bias current and for the high peak currents that discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.

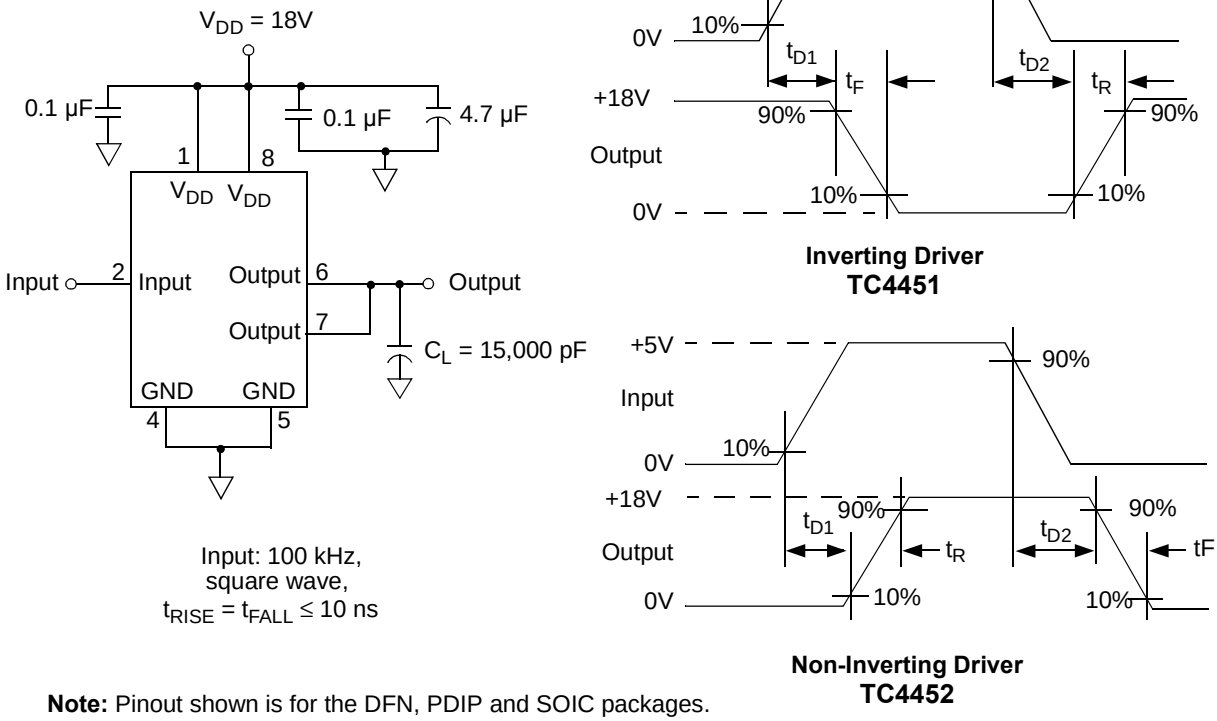
3.5 Exposed Metal Pad

The exposed metal pad of the 6x5 DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a Printed Circuit Board (PCB) to aid in heat removal from the package.

3.6 Metal Tab

The metal tab of the TO-220 package is connected to the V_{DD} potential of the device. This connection to V_{DD} can be used as a current carrying path for the device.

4.0 APPLICATIONS INFORMATION



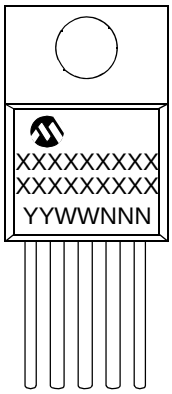
Note: Pinout shown is for the DFN, PDIP and SOIC packages.

FIGURE 4-1: *Switching Time Test Circuits.*

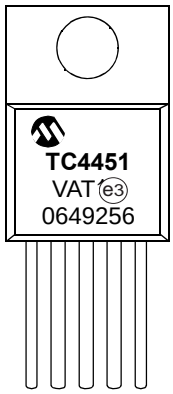
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

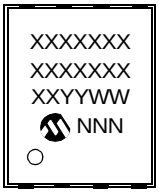
5-Lead TO-220



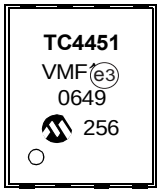
Example:



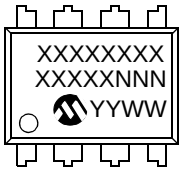
8-Lead DFN-S



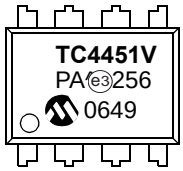
Example:



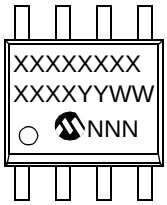
8-Lead PDIP (300 mil)



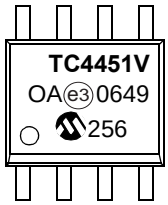
Example:



8-Lead SOIC (150 mil)



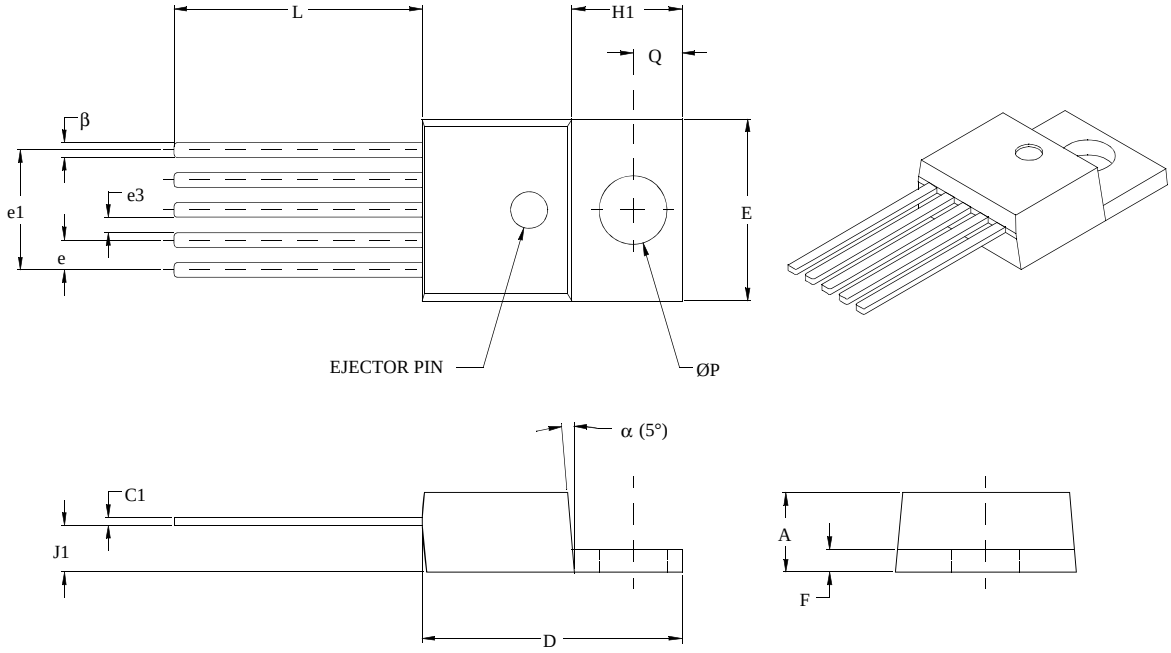
Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Transistor Outline (AT) (TO-220)



Units		INCHES*		MILLIMETERS	
Dimension Limits		MIN	MAX	MIN	MAX
Lead Pitch	e	.060	.072	1.52	1.83
Overall Lead Centers	e1	.263	.273	6.68	6.93
Space Between Leads	e3	.030	.040	0.76	1.02
Overall Height	A	.160	.190	4.06	4.83
Overall Width	E	.385	.415	9.78	10.54
Overall Length	D	.560	.590	14.22	14.99
Flag Length	H1	.234	.258	5.94	6.55
Flag Thickness	F	.045	.055	1.14	1.40
Through Hole Center	Q	.103	.113	2.62	2.87
Through Hole Diameter	P	.146	.156	3.71	3.96
Lead Length	L	.540	.560	13.72	14.22
Base to Bottom of Lead	J1	.090	.115	2.29	2.92
Lead Thickness	C1	.014	.022	0.36	0.56
Lead Width	β	.025	.040	0.64	1.02
Mold Draft Angle	α	3°	7°	3°	7°

***** Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254 mm) per side.

JEDEC equivalent: TO-220

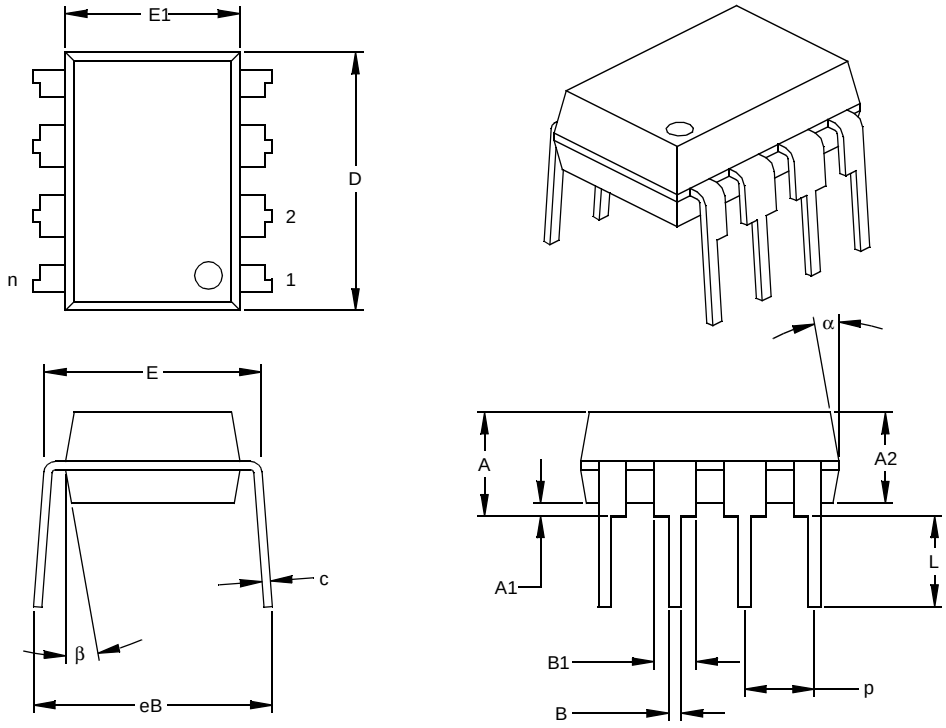
Drawing No. C04-036

Revised 08-01-05

8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S) – Saw Singulated

	INCHES
	NOM
	.050 BSC
	.008
	.197
	.236

8-Lead Plastic Dual In-line (PA) – 300 mil (PDIP)

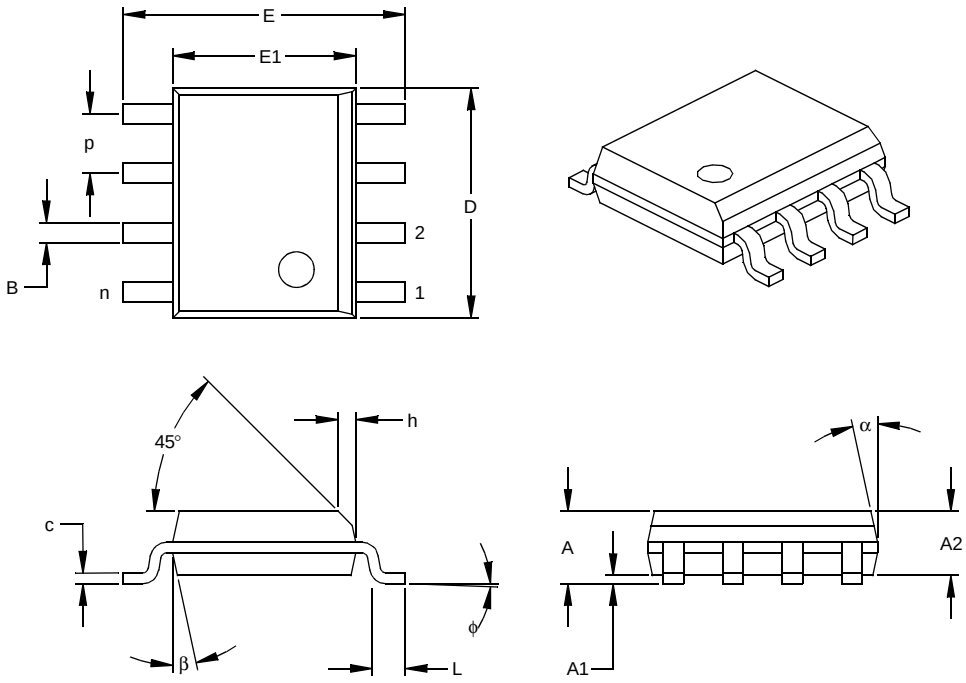


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (OA) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (February 2006)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XXX
Device	Temperature Range	Package	Tape & Reel

Device:	TC4451:	12A High-Speed MOSFET Driver, Inverting
	TC4452:	12A High-Speed MOSFET Driver, Non-Inverting
Temperature Range:	V =	-40°C to +125°C
Package: *	AT =	TO-220, 5-lead
	MF =	Dual, Flat, No-Lead (6x5 mm Body), 8-lead
	MF713 =	Dual, Flat, No-Lead (6x5 mm Body), 8-lead (Tape and Reel)
	PA =	Plastic DIP (300 mil Body), 8-lead
	OA =	Plastic SOIC (150 mil Body), 8-lead
	OA713 =	Plastic SOIC (150 mil Body), 8-lead (Tape and Reel)

*All package offerings are Pb Free (Lead Free).

Examples:

a) TC4451VAT: 12A High-Speed Inverting MOSFET Driver, TO-220 package

b) TC4451VOA: 12A High-Speed Inverting MOSFET Driver, SOIC package

c) TC4451VMF: 12A High-Speed Inverting MOSFET Driver, DFN package

a) TC4452VPA: 12A High-Speed Non-Inverting MOSFET Driver, PDIP package

b) TC4452VOA: 12A High-Speed Non-Inverting MOSFET Driver, SOIC package

c) TC4452VMF: 12A High-Speed Non-Inverting MOSFET Driver, DFN package

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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