MPQ4272

36V, 3A Dual Buck Converters with I²C Interface for Automotive Power Delivery, AEC-Q100

DESCRIPTION

The MPQ4272 integrates dual-channel, monolithic step-down converters with an I²C interface. Each channel can deliver up to 3A of output current across a wide input supply range, with excellent load and line regulation.

The MPQ4272 is designed for USB charger applications with dual ports. Both channels can work with an external USB power deliver (PD) controller.

The I²C interface and one-time programmable (OTP) memory provide flexibility with configurable features.

Fault condition protections include current limiting, output over-voltage protection (OVP), and thermal shutdown (TSD).

The MPQ4272 requires a minimal number of readily available, standard external components. It is available in a QFN-21 (4mmx5mm) package.

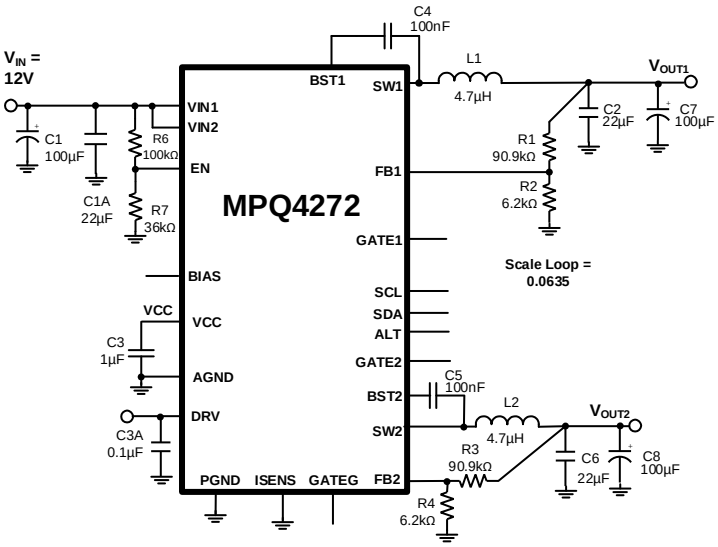
FEATURES

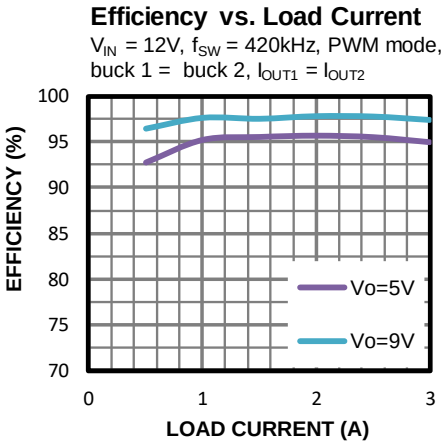
- Dual 3A or Shared 6A Buck Converter
- Supports USB PD 3.0
- Wide 4V to 36V Operating Input Voltage Range
- 1V to 21V Output Voltage Range with 12.6mV Resolution, V_{OUT} Scale Loop = 0.0635
- Selectable 250kHz, 420kHz, 1.1MHz, or 2.1MHz Switching Frequency
- Frequency Spread Spectrum
- Low-Dropout Mode
- Line Drop Compensation
- Accurate Adjustable CC Output Current Limit (50mA/Step via the I²C)
- 22mΩ High-Side and 26mΩ Low-Side Low $R_{DS(ON)}$ Internal Buck Power MOSFETs
- I²C Interface and Over-Temperature Protection (OTP) with PMBus-Compatible Parameters:
  - PFM/PWM Mode, Current Limit, Output Voltage, Frequency Spread Spectrum, Phase Delay, and Line Drop Compensation
- V_{BUS} Isolation N-Channel MOSFET Gate Driver
- Battery Short-to-Ground Protection
- Load-Shedding Alert
- EN Shutdown Active Discharge
- Available in a QFN-21 (4mmx5mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- USB Power Delivery
- USB-Dedicated Charging Ports (DCP)
- Automotive DC/DC Supplies

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number**	Package	Top Marking	MSL Rating
MPQ4272GVE-0000-AEC1*	QFN-21 (4mmx5mm)	*See Below*	1
MPQ4272GVE-0001-AEC1*			
MPQ4272GVE-0011-AEC1*			
MPQ4272GVE-xxxx-AEC1*			

* For Tape & Reel, add suffix -Z (e.g. MPQ4272GVE-xxxx-AEC1-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the OTP. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code. MPQ4272GVE-0000 is the default version.

TOP MARKING

MPSYWW

MP4272

LLLLLL

E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4272: Part number
LLLLLL: Lot number
E: Wettable flank

EVALUATION KIT EVKT-MPQ4272

EVKT-MPQ4272 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVQ4272-VE-00A	MPQ4272 evaluation board	1
2	EVKT-USBI2C-02 bag	Includes USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	MPQ4272GVE-0000-AEC1	IC with default configuration	2

Order directly from MonolithicPower.com or our distributors.

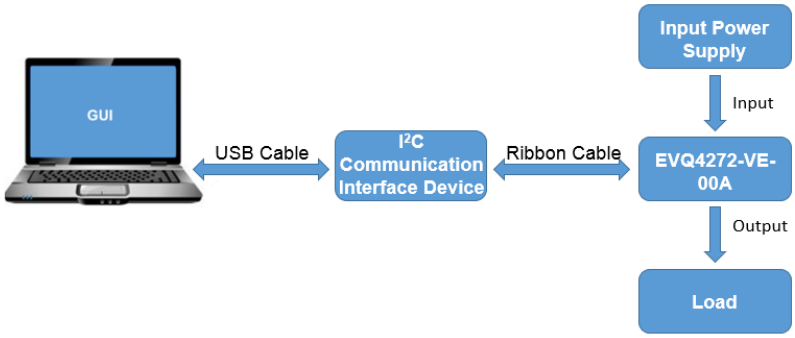
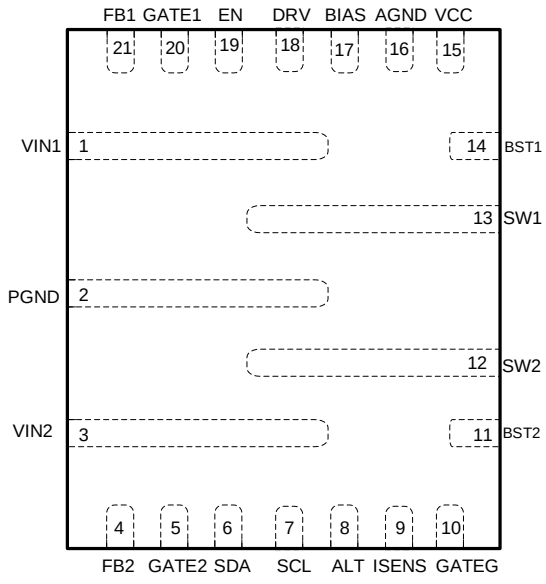


Figure 1: EVKT-MPQ4272 Evaluation Kit Set-Up

PACKAGE REFERENCE

TOP VIEW



QFN-21 (4mmx5mm) with Wettable Flanks

PIN FUNCTIONS

Pin #	Name	Description
1	VIN1	**Supply voltage.** The MPQ4272 operates from a 4V to 36V input voltage. An input capacitor (C_{IN}) prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible. VIN1 is the drain for channel 1's internal power device. VIN1 also provides the power supply for the entire chip. VIN1 and VIN2 should be connected together.
2	PGND	**Power ground.** Reference ground of the first channel. PGND requires special considerations when designing the PCB layout. Connect PGND to GND with copper traces and vias.
3	VIN2	**Supply voltage**. The MPQ4272 operates from a 4V to 36V input voltage. C_{IN} prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible. VIN2 is the drain for channel 2's internal power device. VIN1 and VIN2 should be connected together.
4	FB2	**Feedback pin for buck 2.**
5	GATE2	**Gate driver.** Gate driver to turn on the isolation N-channel MOSFET on the V_{BUS} line.
6	SDA	**I²C data line.**
7	SCL	**I²C clock signal input.**
8	ALT	**PMBus alert pin.** Open-drain output. Active low.
9	ISENS	**Second current limit sense pin.**
10	GATEG	**Gate drive pin to drive the external MOSFET.** The external MOSFET is used for ground short-to-battery protection.
11	BST2	**Bootstrap 2.** Connect a 0.1µF capacitor between the SW2 and BST2 pins to form a floating supply across the high-side switch driver.
12	SW2	**Switch 2 output.** Use a wide PCB trace to connect SW2 to the pad.
13	SW1	**Switch 1 output.** Use a wide PCB trace to connect SW1 to the pad.
14	BST1	**Bootstrap 1.** Connect a 0.1µF capacitor between the SW1 and BST1 pins to form a floating supply across the high-side switch driver.
15	VCC	**Internal 5V LDO regulator output**. Decouple VCC with a 1µF capacitor.
16	AGND	**Analog ground.** Connect AGND to PGND. AGND should also be connected to the VCC capacitor's ground node.
17	BIAS	**Bias input pin of internal VCC LDO**. Connect the BIAS pin to a 5V or 9V V_{OUT} to improve system efficiency. Add an RC low-pass filter from output to the BIAS pin.
18	DRV	**LDO output.** 1mA load capability. The output voltage can be set by the I²C. Decouple DRV with a 0.1µF capacitor.
19	EN	**Enable control pin.** Apply a logic high voltage on this pin to enable the IC. Pull EN to logic low to disable the IC. The EN pin has an internal pull-down resistor.
20	GATE1	**Gate driver.** Gate driver to turn on the isolation N-channel MOSFET on the V_{BUS} line.
21	FB1	**Feedback pin for buck 1.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage ($V_{IN1/2}$) 40V
$V_{SW1/2}$..... .....-0.3V (-5V for <10ns)
.....to V_{IN} + 0.3V (43V for <10ns)
$V_{BST1/2}$..... $V_{SW1/2}$ + 5.5V
V_{BIAS}, $V_{GATE1/2}$, V_{ISENS} .....-0.3V to +30V
V_{EN} .....-0.3V to +10V (2)
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (3) (6)
QFN-21 (4mmx5mm) 5.08W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings (4)

Human body model (HBM) 2000V
Charged device model (CDM) 750V

Recommended Operating Conditions (5)

Operation input voltage range .....4V to 36V
Operation output voltage range .....
.....1V to V_{IN} x D_{MAX}
Output current.....3A for each channel
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

EVQ4272-VE-00A (6)	24.6	6.3 °C/W
QFN-21 (4mmx5mm) (7)	44	9 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For details on the EN pin's absolute maximum rating, see the Enable (EN) Control section on page 17.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. HBM with regard to GND.
5) The device is not guaranteed to function outside of its operating conditions. The PMBus V_{OUT} command does not support voltages exceeding 21V. If V_{OUT} must exceed 21V, a feedback resistor is required.
6) Measured on EVQ4272-VE-00A, 4-layer PCB, 55mmx55mm.
7) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{Q_STD}	V_{EN} = 0V, T_J = 25°C		0.5	5	μA
		T_J = -40°C to + 125°C		0.5	30	μA
Quiescent supply current	I_Q	No switching, both channels enabled		0.3		mA
EN rising threshold	V_{EN_RISING}		-5%	1.6	+5%	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pull-down resistor	R_{EN}	V_{EN} = 2V		2		MΩ
Thermal shutdown (8)	T_{STD}	OTP = 011b		170		°C
Thermal hysteresis (8)	T_{STD_HYS}			20		°C
VCC regulator	V_{CC}	I_{CC} = 0mA to 50mA, T_J = -40°C to +125°C	4.5	5.0	5.25	V
Step-Down Converters (Ch1 and Ch2)						
V_{IN} under-voltage lockout (UVLO) rising threshold	V_{IN_UVLO}	Monitor VIN1 only	3.2	3.35	3.5	V
V_{IN} UVLO threshold hysteresis	V_{UVLO_HYS}			300		mV
HS-FET on resistance	$R_{DS(ON)\_HS}$			22		mΩ
LS-FET on resistance	$R_{DS(ON)\_LS}$			26		mΩ
FB reference voltage	V_{FB0}	Set V_{OUT} = 1.25V	0.092	0.1	0.108	V
	V_{FB1}	Default, V_{OUT} = 5V	-2%	0.400	+2%	V
	V_{FB2}	Set V_{OUT} = 9V	-1.5%	0.720	+1.5%	V
	V_{FB3}	Set V_{OUT} = 20V	-1.5%	1.600	+1.5%	V
Output over-voltage protection (OVP)	V_{OVP_F}		114	120	125	%
Output OVP recovery	V_{OVP_R}		104	109	114	%
High-side current limit	I_{HS_PEAK}			13		A
Valley current limit		Falling edge		8		A
Low-side current limit	I_{LS_SINK}			-3.6	-2	A
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +150°C			30	
Output CC current limit	I_{LIMIT}	I²C set 1, T_J = 0°C to 85°C, 420kHz	-5%	3.6	+5%	A
Oscillator frequency	f_{SW1}	I²C set 1	-20%	250	+20%	kHz
	f_{SW2}	I²C set 2 (default)	-20%	420	+20%	
	f_{SW3}	I²C set 3	-20%	1100	+20%	
	f_{SW4}	I²C set 4	-20%	2100	+20%	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Frequency dithering				±12		%
Maximum duty cycle (8)	D_{MAX1}	FREQ = 420kHz		95		%
	D_{MAX2}	In dropout mode		99		%
Minimum off time (8)	t_{OFF_MIN}			100		ns
Minimum on time (8)	t_{ON_MIN}			80		ns
Soft-start time	t_{SS}	Output from 10% to 90%, V_{OUT} = 5V, constant slew rate for other V_{OUT}		0.8		ms
Second Current Limit Sense						
ISENS rising threshold	I_{SENS_R}	The buck is disabled once triggered, gate 1 and gate 2 are off	130	160	190	mV
ISENS falling threshold	I_{SENS_F}		70	100	130	mV
ISENS deglitch time (8)	t_{SENS}	Release edge		20		µs
ISENS pull-down current	I_{ISENS1}	V_{ISENS} = 12V		17		mA
	I_{ISENS2}	V_{ISENS} = 80mV		2.5		mA
GATEG pull-down resistance	R_{GATEG}			12	25	Ω
GATE1, GATE2						
Output voltage	V_{GATE1_2}	V_{IN} = 12V, V_{CC} = 5V	16	17	18	V
Source current	I_{GATE1_2}		-30%	21.5	+30%	µA
DRV voltage	V_{DRV}		5.7	5.95	6.2	V
		Load = 1mA	5.45	5.82	5.95	V
I²C Interface Specifications (High-Speed Mode)						
Alert pull-low resistance				10	25	Ω
Alert leakage		Pull-up with 5V			1	µA
Input logic high	V_{IH}	I²C pulled up to VDD (1.8V to 5V)	1.4			V
Input logic low	V_{IL}				0.45	V
Output voltage logic low	V_{OUT_L}				0.4	V
SCL clock frequency	f_{SCL}			400		kHz
SCL high time	t_{HIGH}		60			ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}			60		ns
Set-up time for repeated start condition	t_{SU_STA}		160			ns
Hold time for repeated start condition	t_{HD_STA}		160			ns
Bus free time between a start and stop condition	t_{BUF}		160			ns
Set-up time for stop condition	t_{SU_STO}		160			ns
SCL and SDA rise time	t_R		10		300	ns
SCL and SDA fall time	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				400	pF

Note:

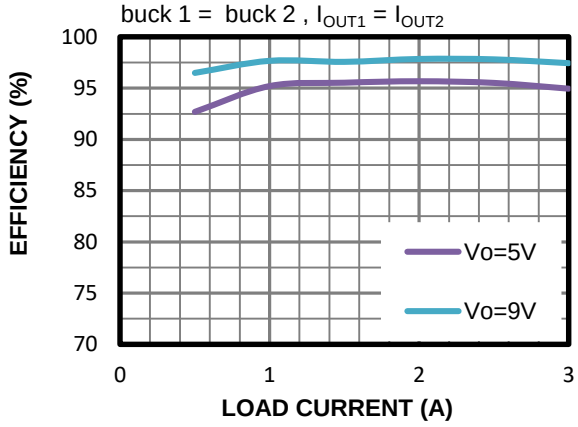
8) Guaranteed by characterization testing.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

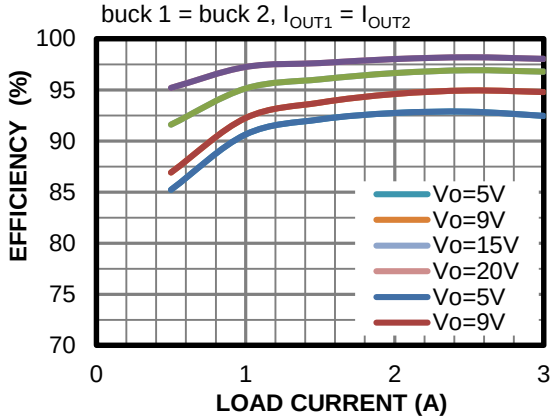
Efficiency vs. Load Current

V_{IN} = 12V, f_{SW} = 420kHz, PWM mode, buck 1 = buck 2 , I_{OUT1} = I_{OUT2}



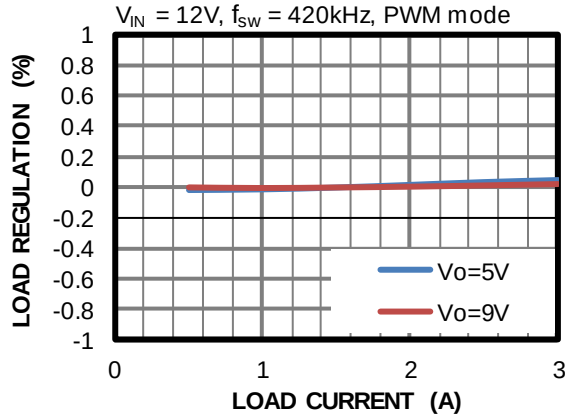
Efficiency vs. Load Current

V_{IN} = 24V, f_{SW} = 420kHz, PWM mode, buck 1 = buck 2, I_{OUT1} = I_{OUT2}



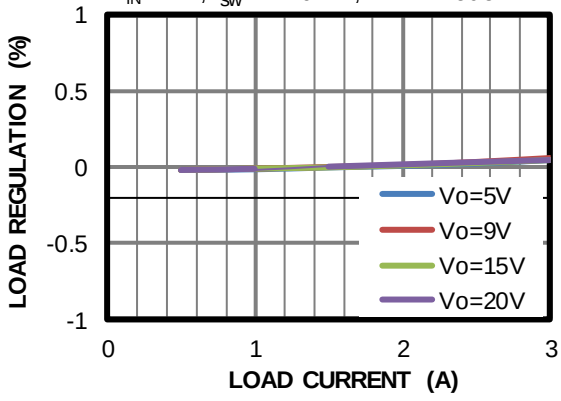
Load Regulation

V_{IN} = 12V, f_{SW} = 420kHz, PWM mode



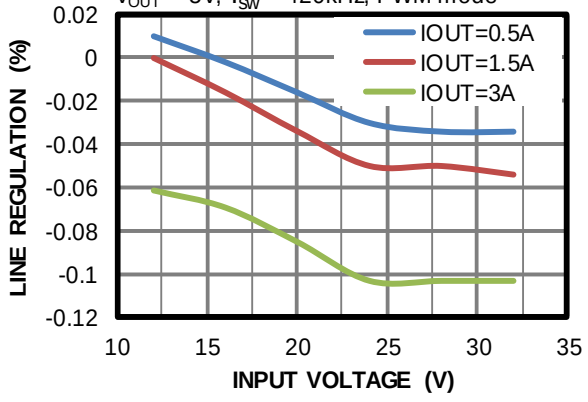
Load Regulation

V_{IN} = 24, f_{SW} = 420kHz, PWM mode



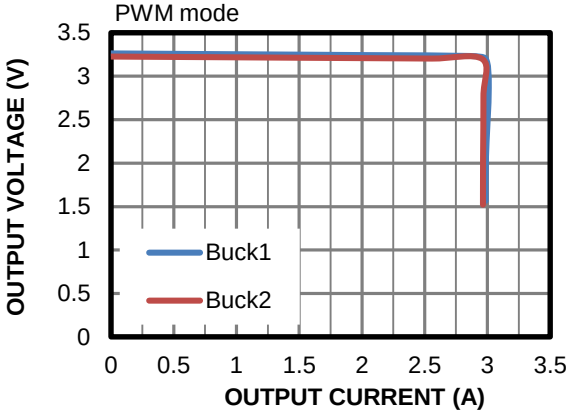
Line Regulation

V_{OUT} = 5V, f_{SW} = 420kHz, PWM mode



CC Curve

V_{IN} = 12V, V_{OUT} = 3.3V, CC = 3A, PWM mode

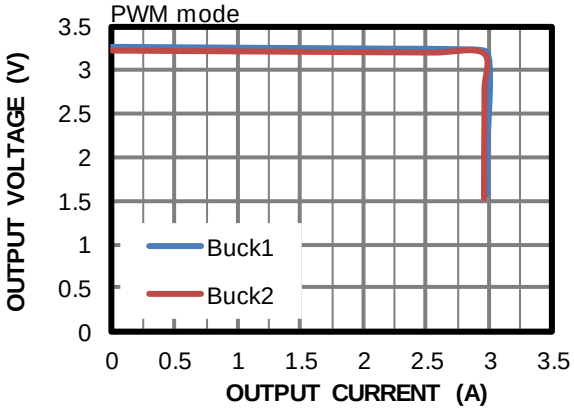


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

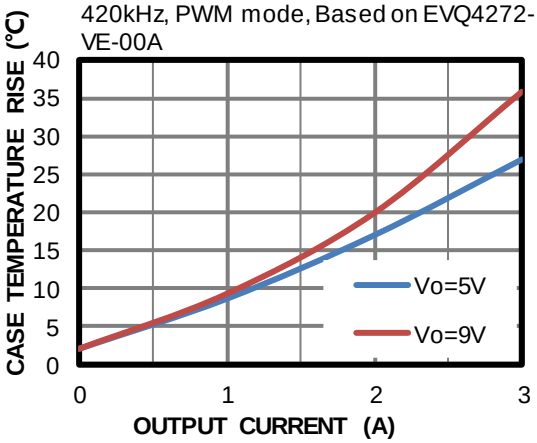
CC Curve

V_{IN} = 12V, V_{OUT} = 3.3V, CC = 3A, PWM mode



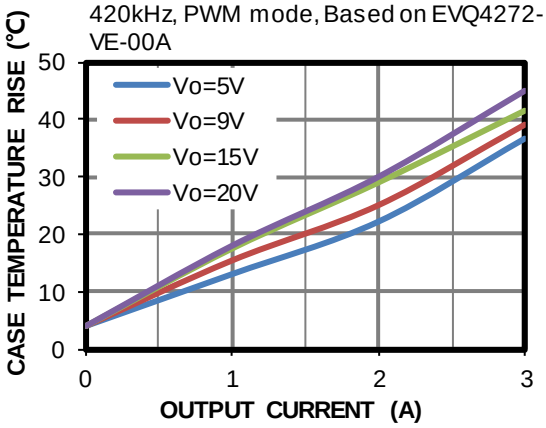
Case Temperature Rise

V_{IN} = 12V, Buck1 = Buck2, Io1 = Io2, F_{sw} = 420kHz, PWM mode, Based on EVQ4272-VE-00A



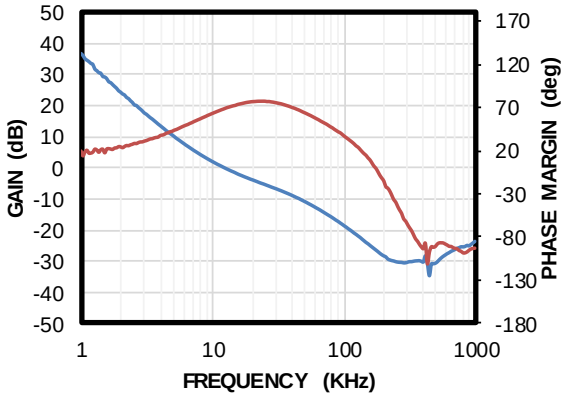
Case Temperature Rise

V_{IN} = 24V, Buck1 = Buck2, Io1 = Io2, F_{sw} = 420kHz, PWM mode, Based on EVQ4272-VE-00A



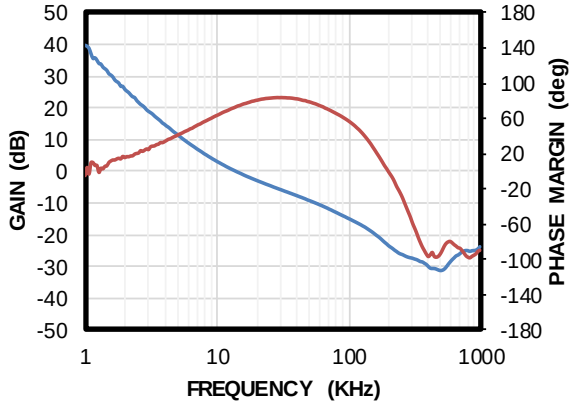
Bode Plot

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, C_{OUT} = 100µF (hybrid e-capacitor, ESR = 20mΩ) + 22µF (ceramic), BW = 12.6kHz, PM = 70.04°



Bode Plot

V_{IN} = 12V, V_{OUT} = 9V, I_{OUT} = 3A, PM = 72.82°, C_{OUT} = 100µF (hybrid e-capacitor, ESR = 20mΩ) + 22µF (ceramic), BW = 14kHz

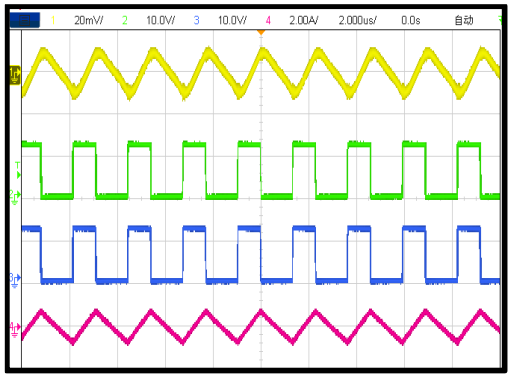


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

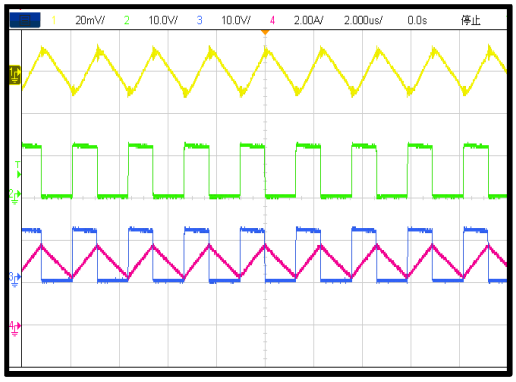
Output Ripple

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 0A, PWM mode



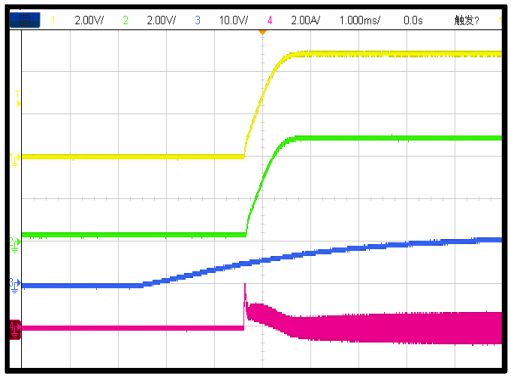
Output Ripple

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 3A, PWM mode



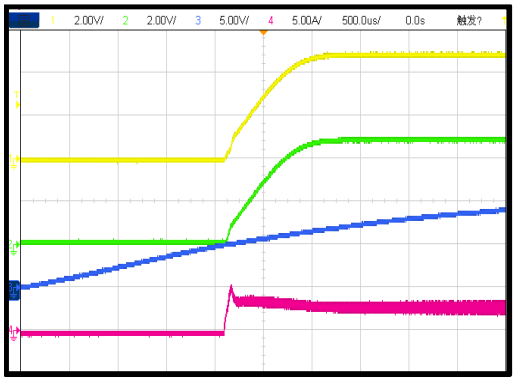
Start-Up

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 0A, PWM mode



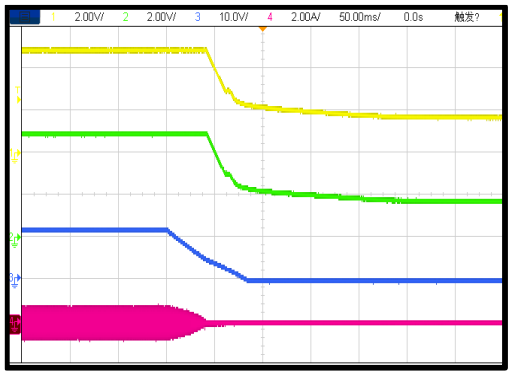
Start-Up

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 3A, PWM mode



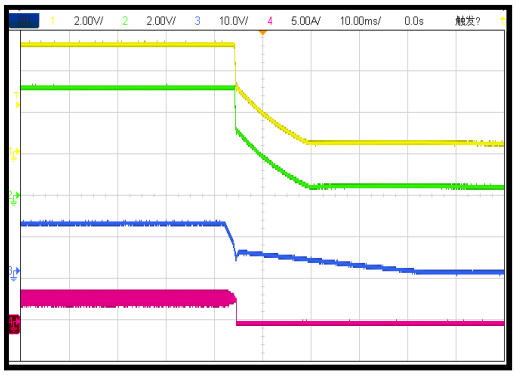
Shutdown

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 0A, PWM mode



Shutdown

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 3A, PWM mode

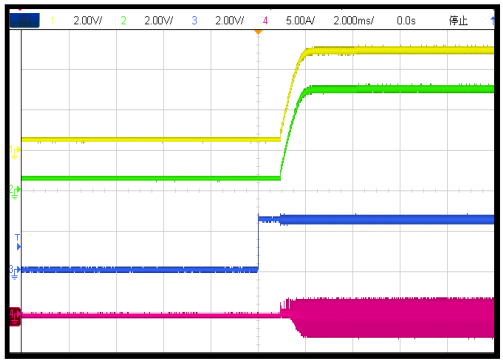


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

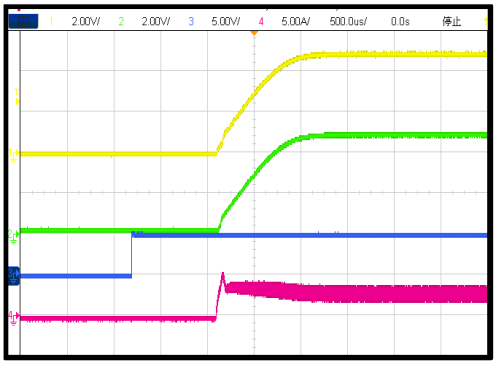
Start-Up through EN

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 0A, PWM mode



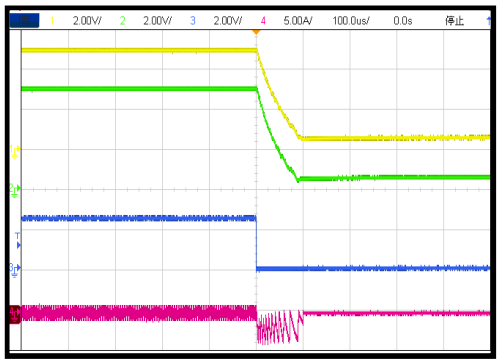
Start-Up through EN

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 3A, PWM mode



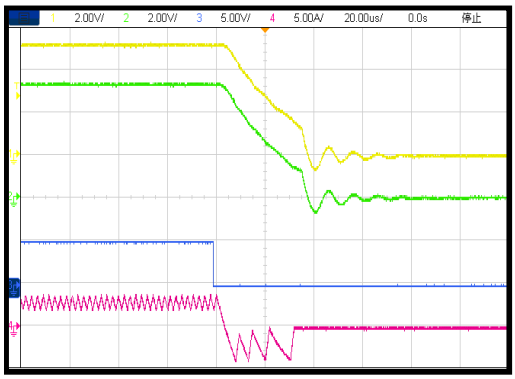
Shutdown through EN

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 0A, PWM mode



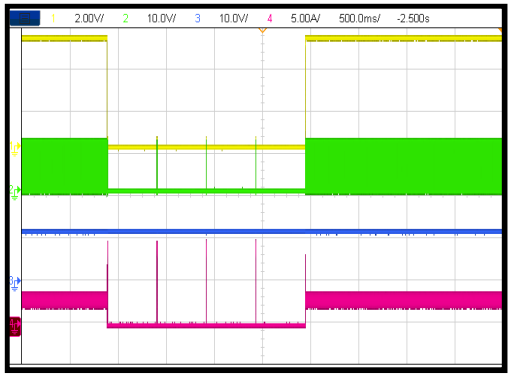
Shutdown through EN

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 3A, PWM mode



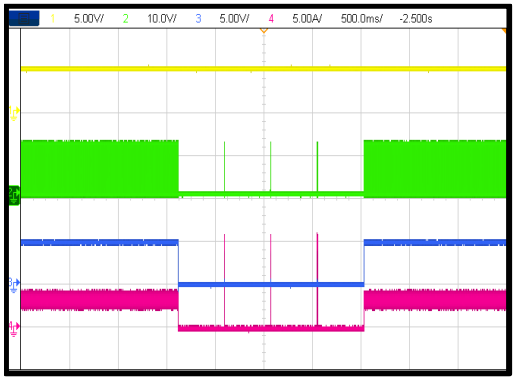
Buck 1 V_{OUT} Short-Circuit Protection Entry and Recovery

V_{IN} = 12V, buck 1 V_{OUT} = 5V,
buck 2 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 3A



Buck 2 V_{OUT} Short-Circuit Protection Entry and Recovery

V_{IN} = 12V, buck 2 V_{OUT} = 5V, buck 1 V_{OUT} = 5V,
I_{OUT1} = I_{OUT2} = 3A

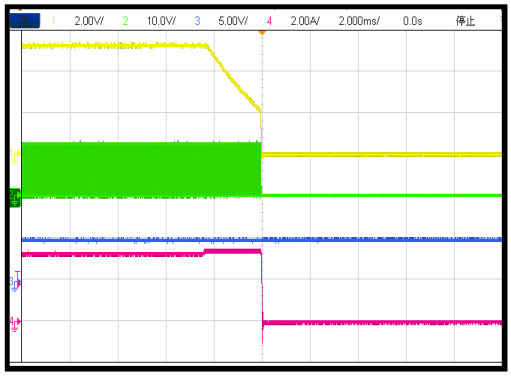


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM Mode, T_A = 25°C, unless otherwise noted.

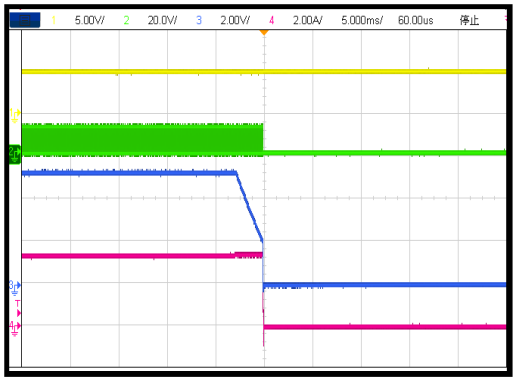
Buck 1 V_{OUT} OCP Test

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V, I_{OUT2} = 0A, CL = 3.6A, I_{OUT1} ramps up slowly



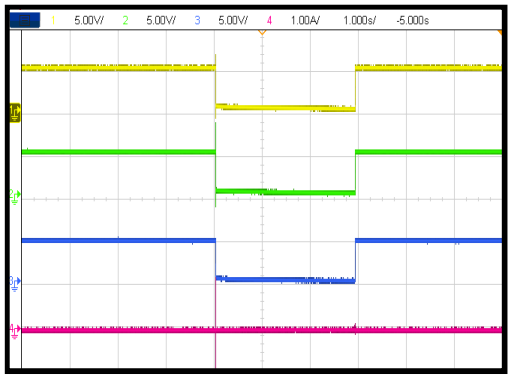
Buck 2 V_{OUT} OCP Test

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V, I_{OUT1} = 0A, CL = 3.6A, I_{OUT2} ramps up slowly



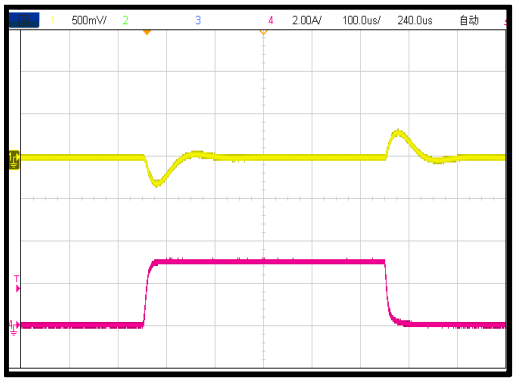
GND2 Short-to-Battery Test

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 0A



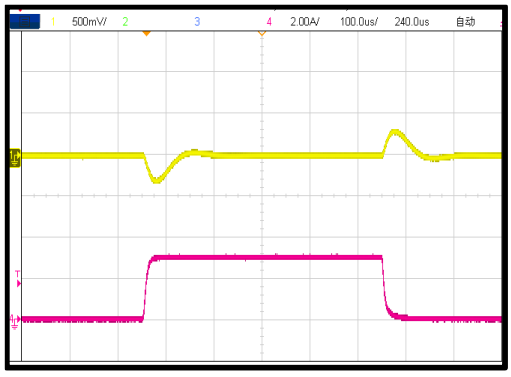
Load Transient (Buck 1 V_{OUT})

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V, I_{OUT1} = 0A to 3A, slew rate = 2.5A/µs



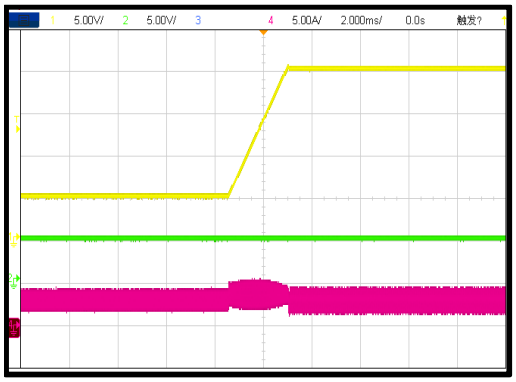
Load Transient (Buck 2 V_{OUT})

V_{IN} = 12V, buck 1 V_{OUT} = buck 2 V_{OUT} = 5V, I_{OUT2} = 0A to 3A, slew rate = 2.5A/µs



Output Voltage Transition (Buck 1 V_{OUT} Set via the I²C)

V_{IN} = 24V, buck 2 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 3A, buck 1 V_{OUT} = 5V to 20V

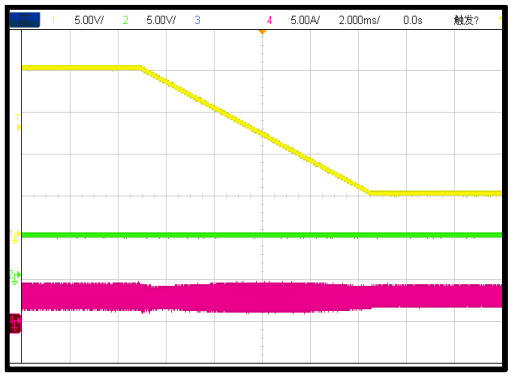


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

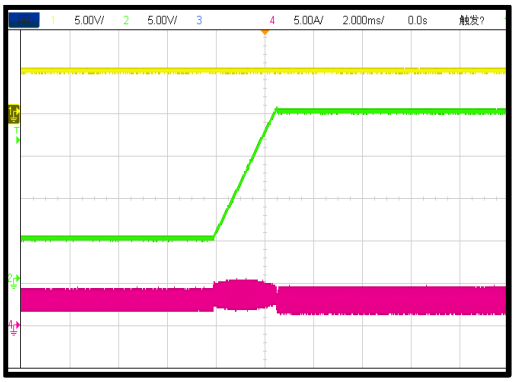
Output Voltage Transition (Buck 1 V_{OUT} Set via the I²C)

V_{IN} = 24V, buck 2 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 3A, buck 1 V_{OUT} = 20V to 5V



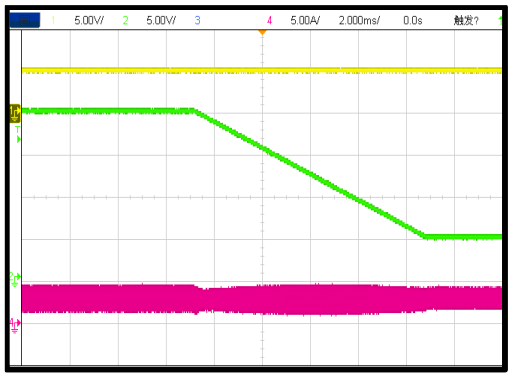
Output Voltage Transition (Buck 2 V_{OUT} Set via the I²C)

V_{IN} = 24V, buck 1 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 3A, buck 2 V_{OUT} = 5V to 20V



Output Voltage Transition (Buck 2 V_{OUT} Set via the I²C)

V_{IN} = 24V, buck 1 V_{OUT} = 5V, I_{OUT1} = I_{OUT2} = 3A, buck 2 V_{OUT} = 20V to 5V



FUNCTIONAL BLOCK DIAGRAM

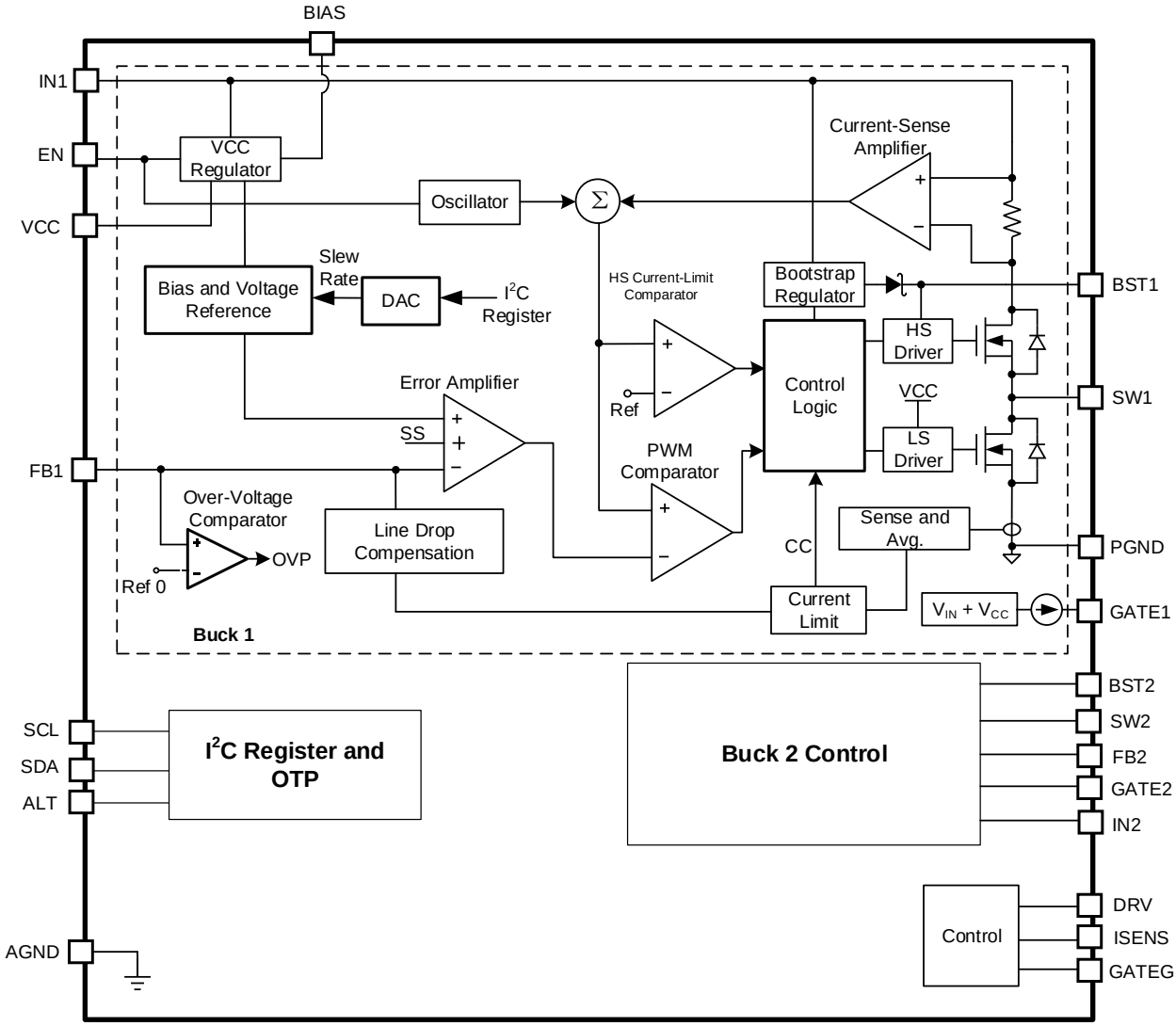


Figure 2: Functional Block Diagram

OPERATION

BUCK CONVERTER

The MPQ4272 integrates two dual-channel, monolithic, synchronous, rectified, step-down switch-mode converters with internal power MOSFETs. It offers a compact solution to achieve a dual 3A of continuous output current across a wide input supply range, with excellent load and line regulation.

Each step-down converter operates with fixed-frequency, peak current mode control to regulate the output voltage (V_{OUT}). There is an internal oscillator that generates two phase-shift reference clocks. Each reference clock initiates the PWM cycle of each channel, which turns on the integrated high-side MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the HS-FET turns off, it remains off until the next clock cycle begins.

Error Amplifier (EA) of Each Channel

The error amplifier (EA) compares the internal feedback voltage (V_{FB}) to the internal reference voltage (V_{REF}) and outputs V_{COMP}. V_{COMP} controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

BIAS and VCC Regulator

Most of the internal circuitries are powered by the internal VCC regulator. The MPQ4272 has two internal regulators (LDO1 and LDO2) (see Figure 3).

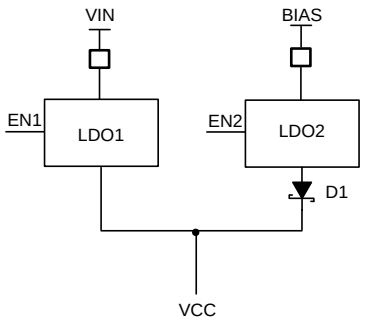


Figure 3: LDO Structure

LDO1 takes the VIN input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, the regulator output is in full regulation, and VCC is 5V. When V_{IN} drops below 5V, the output degrades.

The second regulator (LDO2) is powered by the BIAS pin. Connect the BIAS pin to an external power supply (>4.8V). LDO2 turns on when BIAS > 4.8V. Once LDO2 is enabled, LDO1 is disabled. For output applications equal to or exceeding 5V, connect BIAS to the output to improve efficiency. The diode (D1) between BIAS and the internal circuit is used for current reverse blocking. If the BIAS function is not used, connect the BIAS pin to GND.

VCC requires an external 1µF ceramic decoupling capacitor.

Enable (EN) Control

The MPQ4272 offers enable (EN) control. The EN pin has two levels with different thresholds. At the first level, EN > 0.7V, and VCC is enabled. At the second level, EN > 1.6V, and the chip begins normal operation. EN is clamped internally using a 10V series Zener diode (see Figure 4). Use two resistor dividers to connect the EN pin to the V_{IN} supply and to GND. The EN rising threshold is 1.6V, so V_{IN} must exceed 6.05V to enable the circuit. Do not add a capacitor above 1nF on the EN pin.

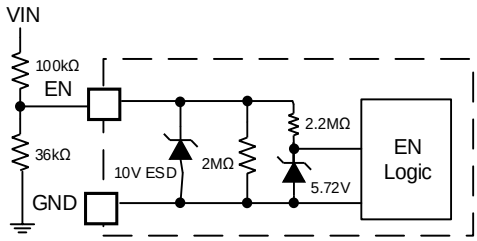


Figure 4: 10V Zener Diode Connection

It is recommended to connect a 100kΩ resistor between VIN and EN, and a 36kΩ resistor between EN and GND. The VIN start and stop switching thresholds can be calculated with Equation (1) and Equation (2), respectively:

$$V_{IN\_ON}(V) = V_{EN\_ON}(V) \times (1+\frac{R_{TOP}}{R_{BOT}}) = 6.05V \quad (1)$$

$$V_{IN\_OFF}(V) = V_{EN\_OFF}(V) \times (1+\frac{R_{TOP}}{R_{BOT}}) = 5.29V \quad (2)$$

The EN rising threshold is 1.6V, and the EN falling threshold is 1.4V. This means that the V_{IN} rising threshold is 6.05V, and the V_{IN} falling threshold is 5.29V.

If EN is connected directly to a voltage source without a pull-up resistor, limit the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage (V_{IN}). The UVLO rising threshold is 3.35V, and its falling threshold is 3.05V.

Internal Soft Start (SS)

Soft start (SS) prevents V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage (V_{SS}) that ramps up from 0V to 5V. When V_{SS} is below V_{REF}, the EA uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference.

If the MPQ4272 output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and low-side MOSFET (LS-FET) until the voltage on the internal SS capacitor exceeds the internal V_{FB}.

Low-Dropout Mode

The MPQ4272 has a low-dropout function when V_{IN} is almost equal to V_{OUT}. After the minimum off time is triggered, the on time is extended and the switching frequency starts to decrease. When the maximum on time is triggered, the MPQ4272 works in maximum duty cycle operation (about 99.4%).

Constant Current (CC) Mode Over-Current Protection (OCP)

The MPQ4272 senses the low-side current and uses this information to emulate the output current (I_{OUT}) amplitude. If I_{OUT} exceeds the set current-limit threshold, the MPQ4272 enters constant current (CC) limit mode. In this mode, the current amplitude is limited.

As the load resistance drops, V_{OUT} also drops until V_{FB} falls below the under-voltage (UV) threshold. Once a UV condition is triggered, the MPQ4272 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4272 exits hiccup mode once the over-current (OC) condition is removed.

When V_{OUT} is set above 6.3V, the MPQ4272 hiccup UV threshold is about 2.4V. When V_{OUT} is set below 5.5V, the hiccup UV threshold is about 30% of the feedback reference value.

Buck Output Over-Voltage Protection (OVP)

The MPQ4272 has output over-voltage protection (OVP). If V_{OUT} exceeds 120% of V_{REF}, the HS-FET stops turning on. The LS-FET turns on to discharge V_{OUT} until the low-side current reaches -3.6A. When the next internal clock starts, the LS-FET turns on again and repeats this process. Once V_{FB} drops to 109% of V_{REF}, the MPQ4272 resumes normal operation.

Input Over-Voltage Protection (OVP)

The MPQ4272 has input over-voltage protection (OVP). If both output OVP and the input OVP fault rising threshold (about 39.5V) are triggered at the same time, the device stops switching. When V_{IN} falls below the input OVP fault falling threshold (about 37V), the device starts switching again. The MPQ4272 continues switching when the input OVP warning threshold is triggered. The input OVP warning rising threshold is about 37.5V, and the falling threshold is about 35V.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V, with a hysteresis of 150mV. The BST1 capacitor voltage is regulated internally by VCC through D2, M1, and C2 (see Figure 5).

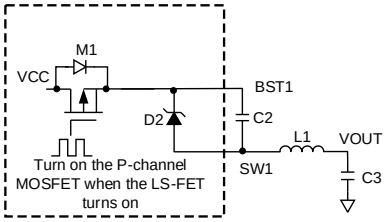


Figure 5: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both VIN1 and EN exceed their respective thresholds and I²C operation is set up, the chip is enabled.

The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN going low, VIN going low, an I²C operation off command, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rails are pulled down. The floating driver is not subject to this shutdown command.

EN Shutdown Discharge

When the EN pin is pulled low, the buck converter enters output discharge mode. Meanwhile, the internal soft-start capacitor starts to discharge. The discharge mode keeps working until the soft-start capacitor discharges to a very low level.

In this mode, the LS-FET turns on and remains on until the low-side current reaches the negative current limit (about -3.6A). Then the LS-FET turns off. It turns on again when the next clock cycle begins.

Output Line Drop Compensation

The MPQ4272 is capable of compensating for a V_{OUT} drop (e.g. high impedance caused by a long trace) to keep a fairly constant load-side voltage. The MPQ4272 uses the sensed load current through the LS-FET to sink a current (I_{COMP}) at the FB pin (see Figure 6).

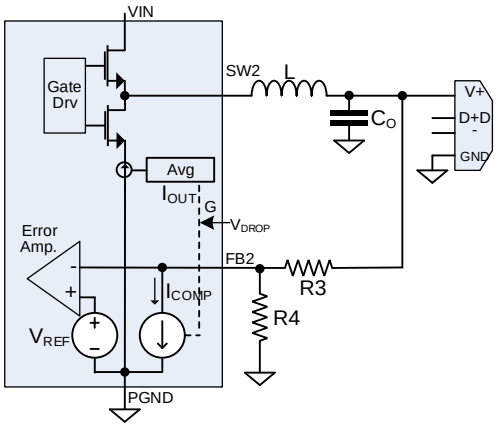


Figure 6: Line Drop Compensation

I_{COMP} can be calculated with Equation (3):

$$I_{COMP} = G \times I_{OUT} \quad (3)$$

V_{OUT} can be estimated with Equation (4):

$$v_{OUT} = \left(\frac{R_3}{R_4} + 1\right) \times v_{REF} + R_3 \times G \times I_{OUT} \quad (4)$$

The line drop compensation amplitude under certain output current conditions is equal to R_3 x G x I_{OUT}.

The gain (G) is fixed internally, but it can be configured via the I²C. R_3 can be used to adjust the line drop compensation amplitude.

Battery Short-to-Ground Protection Driver

The MPQ4272 integrates a battery short-to-ground protection driver (GATEG pin). When the output ground (GND 2) shorts to the battery, the ISENS pin's secondary current limit is triggered, the GATEG pin is pulled low, and Q2 turns off (see Figure 7).

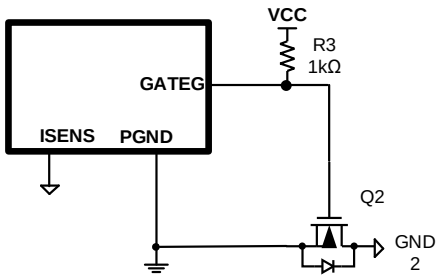


Figure 7: Battery Short-to-Ground Protection

The secondary current limit threshold is equal to 160mV divided by the Q2 $R_{DS(ON)}$. This can protect the GND current from ramping up when the car battery (B+) is falsely shorted to USB GND 2. Meanwhile, the buck output is disabled when secondary current limit is triggered.

If this protection is not required, short ISENS to PGND and float the GATEG pin.

Table 1 shows the different statuses for the GATEG pin.

Table 1: GATEG Pin Status

Condition	GATEG Status
VIN < UVLO threshold	Open drain
EN < UVLO threshold	Open drain
Operation = off	Open drain
I_{SENS_R} > 160mV	0

V_{BUS} Isolation N-Channel MOSFET Driver

GATE1 and GATE2 source a weak 20μA pull-up current to turn on Q1 and Q2. This allows V_{BUS} to turn on. The maximum GATE1 / GATE2 driving voltage is equal to V_{IN1} + V_{CC} (or 25V maximum) via an internal charge pump. A 300kΩ resistor (R7) or Zener diode is required to clamp the maximum Q1 V_{GS} (see Figure 8). In this configuration, the reverse current is blocked during shutdown. When EN is commanded off via the I²C or the device shuts down through the EN pin, the VBUS voltage (V_{BUS}) is discharged first before GATE1 and GATE2 turn off.

When the second current limit is triggered (I_{SENSE} > 160mV), GATE1 and GATE2 also turn off.

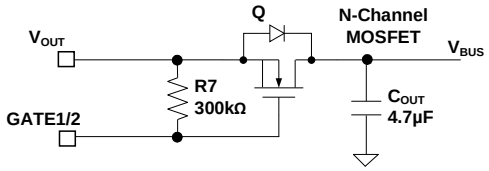


Figure 8: V_{BUS} Isolation Schematic for GATE1 and GATE2

SYSTEM

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (about 140°C), the chip is enabled. The thermal shutdown (TSD) threshold can be configured via the I²C and OTP. The default value is 010b.

I²C Timing

The I²C is active once VIN and EN exceed their UVLO thresholds.

PMBUS INTERFACE

PMBus Serial Interface Description

The power management bus (PMBus) is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the lines, a master device generates an SCL signal and device address, and arranges the communication sequence. This is based on I²C operation principles.

Start and Stop Conditions

The start and stop conditions are signaled by the master device, which signifies the beginning and end of the PMBus transfer. A start command (S) is defined as the SDA signal transitioning from high to low while the SCL is high. A stop command (P) is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 9).

The master then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data is followed by an acknowledge (ACK) bit.

PMBus Update Sequence

The MPQ4272 requires a start condition, a valid PMBus address, a register address byte, and a data byte for a single data update. The device acknowledges that it has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MPQ4272. The device performs an update on the falling edge of the LSB byte.

PMBus Bus Message Format

Figure 10 shows the PMBus message format. The unshaded cells indicate that the bus host is actively driving the bus, and shaded cells indicate that the MPQ4272 is driving the bus. Additional components are defined below:

- S = Start condition
- Sr = Repeated start condition
- P = Stop condition
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

“A” represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is received successfully by a device.

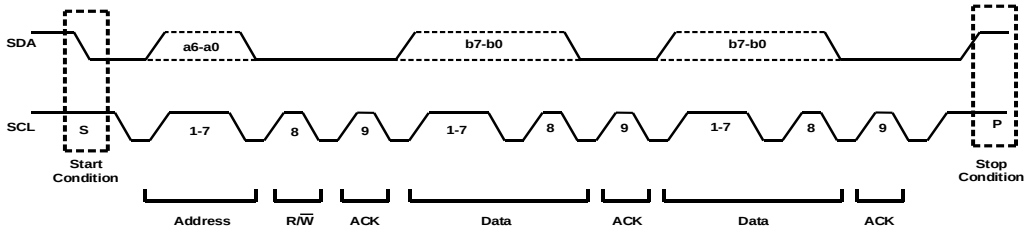


Figure 9: Data Transfer Over the PMBus

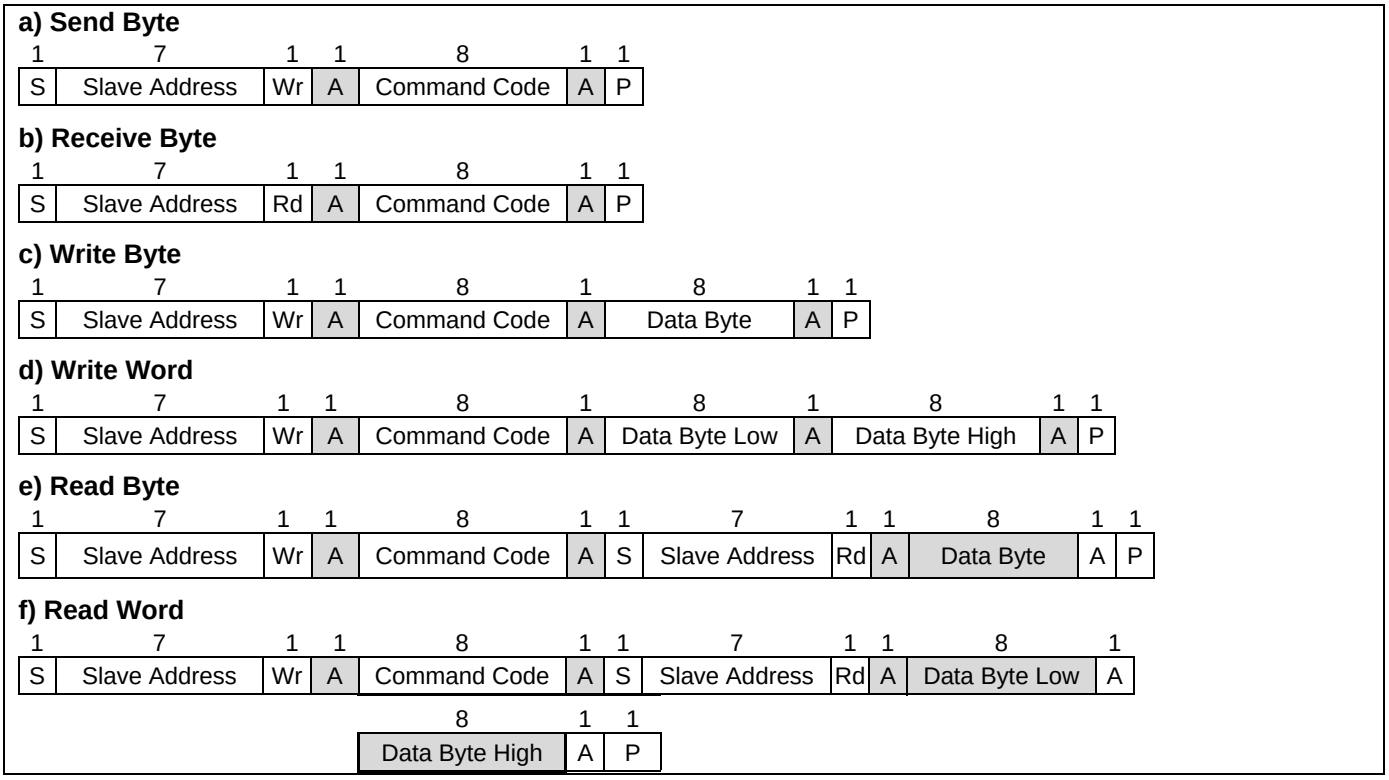


Figure 10: PMBus Message Format

REGISTER DESCRIPTION

I²C/PMBus Register

CMD Name	CMD Code	Description	Type	Data Format	Units	OTP	Default Value (9)
PAGE (1 page). “0xFF” means the both buck converters are being controlled.	0x00	See the PAGE section on page 25	R/W byte	Reg	-	N	0
OPEARTION (Page 0 and Page 1)	0x01	On/off	R/W byte	Reg	-	Y	Off
CLEAR_FAULTS (1 page)	0x03		Send byte	Reg	-	N	-
WRITE_PROTECT (1 page)	0x10		R/W byte	Reg	-	N	-
STORE_USER_ALL (1 page)	0x15	Support 1 time OTP only	Send byte	Reg	-	N	-
RESTORE_USER_ALL (1 page)	0x16		Send byte	Reg	-	N	-
VOUT_MODE (1 page)	0x20	Output voltage format and exponent (2^{-10})	R byte	Reg	-	N	2^{-10} (0x16)
VOUT_COMMAND (Page 0 and Page 1)	0x21		R/W word	Linear L16	V	Y	5V
VOUT_SCALE_LOOP (Page 0 and Page 1)	0x29		R/W word	Linear L11	-	Y	0.08
STATUS_BYTE (Page 0 and Page 1)	0x78		R byte	Reg	-	N	-
STATUS_WORD (Page 0 and Page 1)	0x79		R word	Reg	-	N	-
STATUS_VOUT (Page 0 and Page 1)	0x7A		R byte	Reg	-	N	-
STATUS_INPUT (1 page)	0x7C		R byte	Reg	-	N	-
STATUS_TEMPERATURE (1 page)	0x7D		R byte	Reg	-	N	-
STATUS_CML (1 page)	0x7E		R byte	Reg	-	N	-
MFR_Buck_CTRL1 (Page 0 and Page 1)	0xD0	PWM/PFM, output discharge, hiccup timer, output OVP EN, phase delay	R/W byte	Reg	-	Y	-
MFR_Buck_CTRL2 (1 page)	0xD1		R/W byte	Reg	-	Y	-
MFR_CURRENT_LIMIT (Page 0 and Page 1)	0xD2	Sets the CC current limit continuously	R/W byte	Reg	-	Y	3.6A
MFR_CTRL3 (1 page)	0xD3	I²C address, OTP threshold	R/W byte	Reg	-	Y	-
MFR_CTRL4 (1 page)	0xD4	Frequency, slew rate, OTP warning threshold	R/W byte	Reg	-	Y	-
MFR_CRC_ERROR_FLAG (1 page)	0xD5	Set high when restoring OTP data CRC check error occurs	R byte	Reg	-	N	0
OTP_CONFIGURATION_CODE (1 page)	0xD6	Represents the device	R/W byte	Reg	-	Y	-
OTP_REVISION_NUMBER (1 page)	0xD7	1 byte is about 0x01	R/W byte	Reg	-	Y	-
MFR_STATUS_MASK (1 page)	0xD8	Masks the ALT pin indication	R/W byte	Reg	-	Y	-

Note:

9) All default register values are for the MPQ4272-0000 suffix.

PMBUS COMMAND INTRODUCTION

Data Format (Linear16 and Linear11)

Linear16 (L16) format is used for the V_{OUT} command (see Figure 11).

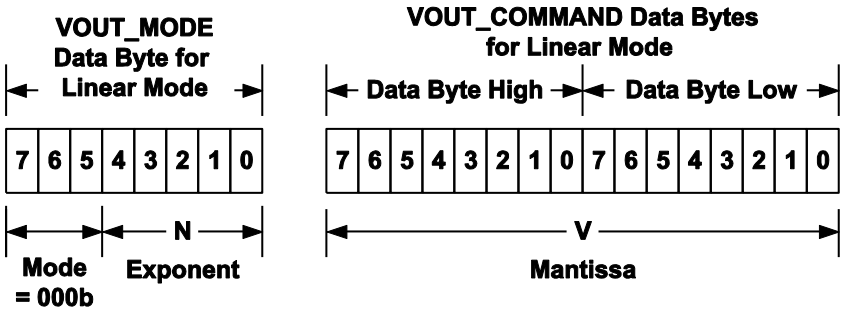


Figure 11: Linear16 Format

The Mode bits are set to 000b. The voltage (in V) can be calculated with Equation (5):

$$Voltage = V \times 2^{N} \quad (5)$$

Where Voltage is the parameter of interest (in V), V is a 16-bit unsigned binary integer, and N is a 5-bit two's complement binary integer.

Linear11 (L11) format is used for other commands, such as the V_{OUT} scale loop, output current, and temperature (see Figure 12).

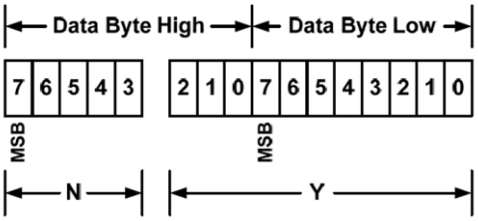


Figure 12: Linear11 Format

The relation between Y, N, and the real-world value (X) can be estimated with Equation (6):

$$X = Y \times 2^{N} \quad (6)$$

Where X is the real-world value, Y is an 11-bit two's complement integer, and N is 5-bit two's complement integer.

Devices that use the linear format must accept and be able to process any value of N.

PAGE 0 and PAGE 1

PAGE

The PAGE command provides the ability to configure, control, and monitor the device through only one physical address. Note that there are multiple outputs on one device.

Bits[7:1] Value	Bit[0] Value	Description
Reserved	0 (default)	Buck 1 and output 1 are selected
Reserved	1	Buck 2 and output 2 are selected
0xFF		Control both channels simultaneously

In regards to Page 0 and Page 1 operation, the registers that only have one page can be read and written under Page 1 mode. For example, the CLEAR_FAULT register only has one page, but it can be accessed and changed when PAGE is set to 0 or 1.

When PAGE is set to 0xFF, all buck 1 and buck 2 registers (including the MFR registers) are written to the same value when the I²C master sends a write command.

OPERATION

The OPERATION command configures the operational state of the converter. Set OPERATION to 0x80 to enable the output. Set OPERATION to 0x00 or 0x40 to disable the output.

Bits	Purpose	Bit Value	Description
7	On/off state. Note that the EN pin has a higher control priority than this bit.	0 (default)	The output is off.
		1	The output is on.
6:0	Reserved.		

CLEAR_FAULTS

The CLEAR_FAULTS command clears any fault bits that have been set. This command clears all bits in all status registers simultaneously. The device also releases its ALT signal output if the ALT signal is asserted.

If the device has latched off due to a fault protection, the CLEAR_FAULTS command does not force the device to restart.

If the fault is still present when the bit is cleared, the fault bit is immediately set again, and the host is notified. This command is write-only. There is no data byte for this command.

WRITE_PROTECT

The WRITE_PROTECT command controls writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Data Byte Value	Description
1000 0000	Disable all writes except for the WRITE_PROTECT command.
0100 0000	Disable all writes except for the WRITE_PROTECT, OPERATION, and PAGE commands.
0010 0000	Disable all writes except for the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands.
0000 0000	Enable writes to all commands. This is the default value.

STORE_USER_ALL

The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the operating memory to the matching locations in the OTP (non-volatile user store memory). Any items in operating memory that do not have matching locations in the user store are ignored.

The STORE_USER_ALL command can be used while the device is operating. However, the device rejects the I²C write operation until the OTP program is finished. During this process, the I²C read command is still supported. While storing the user memory to the OTP, the device does a cyclic redundancy check (CRC) calculation, and stores the CRC result in a 1-byte OTP cell.

The output turns off first during this operation, then starts up again after the OTP program is finished.

This command has no data bytes. This command is write-only. Only the MPQ4272-0000 IC allows a one-time STORE_USER_ALL operation. Other suffix codes are already OTP-configured in the factory, so they do not support user configurations.

RESTORE_USER_ALL

The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the OTP to the matching locations in the operating memory (I²C register). The values in the operating memory are overwritten by the value retrieved from the user store. Any items in user store that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used while the device is operating. However, the device rejects the I²C write operation until the OTP restoration process is finished. During this process, the I²C read command is still supported. While restoring OTP data to the user memory, the device does a CRC calculation and compares the calculated result to the stored CRC result in the OTP cell. The OTP value is restored to the operating memory only when the values match one other.

The output turns off first during this operation, then starts up again after the OTP program is finished.

This command is write-only. There is no data byte for this command.

VOUT_MODE

Command	VOUT_MODE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	MODE			N				
Default Value	0	0	0	1	0	1	1	0

The MPQ4272 only supports linear mode. Mode bits are set to 000b by default. N is set to a fixed value of -10.

VOUT_COMMAND

The VOUT_COMMAND sets the output voltage (V_{OUT}). It follows Linear16 data format.

Command	VOUT_COMMAND															
Format	Linear16															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Data byte high								Data byte low							
Default Value (5V)	5120 decimal															

V_{OUT} (in V) can be calculated with Equation (7):

$$V_{OUT} = V \times 2^{-10} \quad (7)$$

Where V is a 16-bit unsigned binary integer of VOUT_COMMAND, bits[15:0].

The actual V_{OUT} resolution or minimum step is 0.8mV/K, where K is the value set by VOUT_SCALE_LOOP. For example, if the feedback resistor ratio (V_{OUT} / V_{FB}) equals 12.5, then K = 1/12.5 = 0.08. The real VOUT_COMMAND resolution is 10mV (see Figure 13).

The internal reference voltage is equal to V_{OUT} x K. The internal reference voltage ranges between 0.1V and 1.63V, with a 0.8mV step.

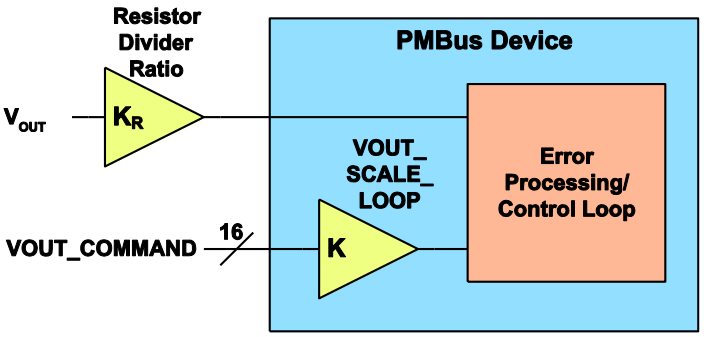


Figure 13: Resistor Divider Ratio

VOUT_SCALE_LOOP

V_{OUT} is typically sensed through a resistor divider (see Figure 14). The resistor divider reduces or scales V_{OUT} so that when V_{OUT} is correct, the value supplied to the control circuit is equal to V_{REF}. This command has 2 data bytes encoded in linear format. It functions similarly to the VOUT_COMMAND data format, and its value is unitless.

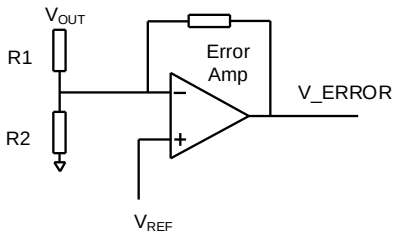


Figure 14: Output Voltage Sense

Command	VOUT_SCALE_LOOP															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	N					Data byte high			Data byte low							
Default Value (0.08)	-10 decimal, 10110 binary					82 decimal, 000 0101 0010 binary										

VOUT_SCALE_LOOP is determined by V_{FB} / V_{OUT} or R2 / (R1 + R2), calculated with Equation (8):

$$VOUT\_SCALE\_LOOP = X \times 2^{-10} \quad (8)$$

Where X is an 11-bit, unsigned binary integer of VOUT_SCALE_LOOP, bits[10:0]. The default value is 0.08.

In real applications, the user should always set VOUT_SCALE_LOOP value equal to the external R2 / (R1 + R2) value. To select VOUT_SCALE_LOOP, follow the steps below:

1. Confirm the maximum V_{OUT}. The MPQ4272's maximum FB reference voltage is 1.638V. Once the maximum V_{OUT} is confirmed, there is a minimum feedback ratio value: (R1 + R2) / $R2_{MIN}$ = VOUT_MAX / 1.638.
2. Confirm the minimum V_{OUT} change resolution. The MPQ4272's minimum FB reference voltage resolution is 0.8mV. The V_{OUT} change resolution is equal to 0.8mV x (R1 + R2) / R2. This means that the maximum feedback ratio (R1 + R2) / $R2_{MAX}$ = $V_{OUTMIN\_DVS\_STEP}$ / 0.8.
3. Choose a proper R2 / (R1 + R2) value that meets the requirements from step 1 and step 2.
4. Set the VOUT_SCALE_LOOP value according to step 3.

For example, in USB PD applications, a 3.3V to 21V output with a 20mV resolution is required for 60W PPS APDO. To obtain the required values, follow the steps below:

1. (R1 + R2) / $R2_{MIN}$ = 21V / 1.638V = 12.82
2. (R1 + R2) / $R2_{MAX}$ = 20mV / 0.8mV = 25
3. Choose (R1 + R2) / R2 = 15.7. Note that this value can be set to any value between 12.82 and 25.
4. VOUT_SCALE_LOOP = 0.0635 according to step 3. In real USB PD applications, set R1 to 93.1kΩ and R2 to 6.2kΩ for a higher V_{OUT} to meet MFI certification requirements.

STATUS_BYTE

The STATUS_BYTE command returns 1 byte of information with a summary of the most critical faults. The STATUS_BYTE message content is described in greater detail below.

Bit	Bit Name	Description
7	BUSY	A fault is detected because the device is busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason (e.g. the device is not enabled). This bit is a non-latch protection. It automatically updates its status without a CLEAR_FAULTS command.
5	VOUT_OV_FAULT	An output over-voltage (OV) fault has occurred.
4	IOUT_OC_FAULT	An output over-current (OC) fault has occurred. If the device reaches the CC current limit or enters hiccup mode, this bit is set.
3	VIN_UV_FAULT	An input under-voltage (UV) fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred (e.g. over-temperature protection or a CRC error).
0	NONE_OF_THE_ABOVE	A fault or warning not listed in bits[7:1] has occurred.

STATUS_WORD

The STATUS_WORD command returns 2 bytes of information with a summary of the MPQ4272's fault conditions. Based on the information in these bytes, the host can get more information by reading the appropriate status registers.

The low byte of the STATUS_WORD is the same register as the STATUS_BYTE command.

Byte	Bits	Bit Name	Description
Low	7:0	-	See the STATUS_BYTE register on page 28.
High	7	VOUT	A V_{OUT} fault or warning has occurred.
	6	IOUT/POUT	An I_{OUT} condition has occurred. If the device reaches the CC current limit or enters hiccup mode, this bit is set.
	5	INPUT	A V_{IN} fault or warning has occurred.
	4	OC_EXIT	This bit indicates if I_{OUT} exits the CC current limit. If I_{OUT} changes from CC (before entering hiccup mode) to non-CC mode, this bit is set high. Recovery from hiccup mode does not set this bit. Send a CLEAR_FAULTS command to reset this bit.
	3	PG_STATUS#	If the POWER_GOOD signal is present, this bit is ineffective. This bit is a non-latch protection. It automatically updates its status without a CLEAR_FAULTS command. If V_{OUT} < 80% of the set-up value, this bit is set to indicate that V_{OUT} is not good. When V_{OUT} > 90% of the set-up value, this bit is cleared, and V_{OUT} is power good. The PG signal rising edge is about 80%, and the falling edge is about 90%.
	2	RESERVED	Reserved.
	1	OTHER	A bit in the STATUS_OTHER register is set.
	0	UNKNOWN	A fault type not listed in bits[15:1] of the STATUS_WORD register has been detected.

Most bits remain set, but there are two exceptions: the OFF and PG_STATUS# bits. These bits always reflect the current state of the device and the POWER_GOOD signal (if present).

STATUS_VOUT

The STATUS_VOUT command returns 1 byte of data to indicate whether a fault or warning has occurred.

Bits	Bit Name	Description
7	VOUT_OV_FAULT	Output over-voltage (OV) fault indicator.
6	VOUT_OV_WARNING	Output OV warning indicator.
5	VOUT_UV_WARNING	Output under-voltage (UV) warning indicator.
4	VOUT_UV_FAULT	Output UV fault indicator.
3:0	RESERVED	Reserved.

STATUS_INPUT

The STATUS_INPUT command returns 1 byte of data to indicate whether a fault or warning has occurred. This command is only one page.

Bit	Bit Name	Description
7	VIN_OV_FAULT	Input over-voltage (OV) fault indicator.
6	VIN_OV_WARNING	Input OV warning indicator.
5	VIN_UV_WARNING	Input under-voltage (UV) warning indicator.
4	VIN_UV_FAULT	Input UV fault indicator.
3	RESERVED	Reserved.
2	RESERVED	Reserved.
1	RESERVED	Reserved.
0	RESERVED	Reserved.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns 1 byte of data to indicate whether a fault or warning has occurred. This command is only one page.

Bits	Bit Name	Description
7	OT_FAULT	Over-temperature (OT) fault indicator. This bit has the same OTP threshold that is set by MFR_OT_FAULT_LIMIT.
6	OT_WARNING	Over-temperature (OT) warning indicator. See the I²C register section (OT_WARNING_THRESHOLD) on page 33 for more details.
5	UT_WARNING	Under-temperature warning indicator. The under-temperature warning threshold is -20°C, with a 10°C hysteresis.
4	UT_FAULT	Under-temperature fault indicator. The under-temperature fault threshold is -40°C, with a 10°C hysteresis.
3	OT_WARNING_EXIT	The OT_WARNING falling edge sets this bit high. There is a 20°C hysteresis.
2:0	RESERVED	Reserved.

MFR COMMAND DESCRIPTION

I²C Register Map

Name	REG (0x)	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MFR_BUCK_CTRL1	D0	R/W	DROPOUT EN	LINE_DROP_ COMPENSATION_ GAIN			OUTPUT _OVP_ EN	HICCUP _TIMER	OUTPUT_ DIS CHARGE_ EN	PFM/ PWM_ MODE
MFR_BUCK_CTRL2	D1	R/W	GATE1_2_ EN	-	PHASE_ DELAY		-	DRV_VOLTAGE		DITHER_ ENABLE
MFR_CURRENT_LIMIT	D2	R/W	CONSTANT_CURRENT_LIMIT (1A to 6.4A/50mA Step)							
MFR_CTRL3	D3	R/W	I²C_ADDRESS (A5:A1)					OTP_THRESHOLD		
MFR_CTRL4	D4	R/W	FREQ (250kHz, 420kHz, 1.1MHz, or 2.1MHz)		SLEW_ RATE		-	OT_WARNING_THRESHOLD		
MFR_CRC_ERROR_FLAG	D5	R	-							CRC_ ERROR
OTP_CONFIGURATION_ CODE	D6	R/W	Represents the device. 0x08.							
OTP_REVISION_NUMBER	D7	R/W	Product suffix (e.g. 0x01)							
MFR_STATUS_MASK	D8	R/W	Mask the ALT pin indication when a fault or event occurs.							

I²C Slave Address

The default I²C slave address is 61h.

I²C Address A7:A1	
Binary	**Hex**
1100 001 (default)	61h
I²C-adjustable for A5:A1	Set by MFR_CTRL3_D, bits[7:3]

MFR_BUCK_CTRL1

Address: 0xD0
Reset value: Set by the OTP
Type: Read and write
Pages: 2 pages

Bits	Bit Name	Description
D[7]	DROPOUT_EN	0: No dropout mode 1: Enable dropout mode when V_{IN} is almost equal to V_{OUT} (default)
D[6:4]	LINE_DROP_ COMPENSATION_ GAIN	000: 0. 001: 0.5μA/A 010: 1μA/A (default for buck 1 and buck 2) 011: 2μA/A 100: 4μA/A 101: 8μA/A
D[3]	OUTPUT_OVP_EN	Enables output over-voltage protection (OVP). The default value is 1. 0: Output OVP is disabled 1: Output OVP is enabled
D[2]	HICCUP_TIMER	Controls the buck over-current protection (OCP) hiccup timer control. The default value is 0. 0: The hiccup timer is 500ms 1: The hiccup timer is 2 seconds

D[1]	OUTPUT_ DISCHARGE_EN	Enables the output discharge function. It is an active discharge. The LS-FET turns on to discharge the output until it reaches the negative current limit. The LS-FET turns on again when a new clock cycle starts. This discharge function is operational until the soft-start signal drops to zero. The default value is 1. 0: Disable the output discharge function 1: Enable the output discharge function
D[0]	PFM/PWM_MODE	Sets the buck to work in auto-PFM/PWM mode or forced PWM mode. The default value is 1. 0: Auto-PFM/PWM mode 1: Forced PWM mode

MFR_BUCK_CTRL2

Address: 0xD1
Reset value: Set by the OTP
Type: Read and write
Pages: Only 1 page

Bits	Name	Description
D[7]	GATE1_2_EN	0: Disable the GATE1 and GATE2 output for a lower I_Q 1: Enable the GATE1 and GATE2 output function (default)
D[5:4]	PHASE_DELAY	Selects the buck switching clock's phase delay (from buck 1 to buck 2). The default value is 10. 00: 0° phase delay 01: 90° phase delay 10: 180° phase delay 11: 270° phase delay
D[2:1]	DRV_VOLTAGE	Sets the DRV pin output voltage. The default value is 01. 00: 5.5V 01: 6V 10: 6.2V 11: 6.5V
D[0]	DITHER_ENABLE	0: No dither (default) 1: Enable frequency spread spectrum

MFR_CURRENT_LIMIT

Address: 0xD2
Reset value: Set by the OTP
Type: Read and write
Page: 2 pages

This command sets the buck output constant current (CC) limit threshold.

Name	IOUT_LIM							
Format	Direct, unsigned binary integer							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value (3.6A)	72 integer							

The real-world IOUT_OC (in A) can be calculated with Equation (9):

$$IOUT\_OC\ (A) = IOUT\_LIM \times 0.05 \quad (9)$$

Where IOUT_LIM is an 8-bit unsigned binary integer of IOUT_LIM, bitsD[7:0].

The IOUT_OC resolution or minimum step is 50mA. The minimum current limit value of IOUT_OC is 1A, and the maximum value is 6.4A. The device is not guaranteed to operate outside this setting range.

MFR_CTRL3

Address: 0xD3
Reset value: Set by the OTP
Type: Read and write
Page: Only 1 page

Sets the thermal shutdown trigger threshold.

Bits	Bit Name	Description
D[7:3]	I²C_ADDRESS	Sets the I²C slave address A5:A1 bit. The default value is 00001.
D[2:0]	OTP_THRESHOLD	Sets the over-temperature (OT) threshold. The default value is 010. 000: 140°C 001: 150°C 010: 160°C 011: 170°C 100~111: Reserved

MFR_CTRL4

Address: 0xD4
Reset value: Set by the OTP
Type: Read and write
Page: Only 1 page

Sets the thermal warning trigger threshold.

Bits	Bit Name	Description
D[7:6]	FREQ	Sets the buck switching frequency. The default value is 01. 00: 250kHz 01: 420kHz 10: 1.1MHz 11: 2.1MHz
D[5:4]	SLEW_RATE	Sets the adjustable V_{REF} slew rate. The default is 10 (VOUT_SLEW_RATE = VREF_SLEW_RATE x Feedback Ratio). 00: 0.08mv/μs V_{REF} rising slew rate; 0.02mv/μs V_{REF} falling slew rate 01: 0.16mv/μs V_{REF} rising slew rate; 0.04mv/μs V_{REF} falling slew rate 10: 0.4mv/μs V_{REF} rising slew rate; 0.1mv/μs V_{REF} falling slew rate 11: 0.8mv/μs V_{REF} rising slew rate; 0.2mv/μs V_{REF} falling slew rate
D[2:0]	OT_WARNING_ THRESHOLD	Sets the over-temperature (OT) warning threshold. There is a 20°C hysteresis for recovery. The default value is 100. 000: 80°C 001: 90°C 010:100°C 011: 110°C 100: 120°C 101: 130°C 110: 140°C 111: 150°C

MFR_CRC_ERROR_FLAG

Address: 0xD5
Reset value: Set by the OTP
Type: Read-only
Page: Only 1 page

Bit	Bit Name	Description
D[0]	CRC_ERROR_FLAG	If a CRC error occurs while restoring the OTP memory to the I²C, this bit is set to 1. If a CRC error occurs, the OTP data is discarded, and the system uses the default I²C or OTP register value.

MFR_STATUS_MASK

Address: 0xD8
Reset value: Set by the OTP
Type: Read and write
Page: 2 pages

This register can only mask off the ALT pin behavior; the STATUS register still indicates each event.

Bit	Bit Name	Description
7	VOUT_MSK	0: No mask (default) 1: Mask enabled
6	IOUT/POUT MSK	0: No mask. This bit masks IOUT_OC_FAULT, IOUT/POUT, and OC_EXIT (default) 1: Mask enabled
5	INPUT_MSK	0: No mask 1: Mask enabled (default)
4	TEMP_MSK	Temperature-related mask bit. 0: No mask (default) 1: Mask enabled
3	PG_STATUS#_MSK	High-level PG mask off control bit. 0: No mask (default) 1: Mask enabled
2	PG_ALT_EDGE_MSK	0: No mask. The ALT pin indicates both the PG_STATUS# rising and falling edges (default) 1: Mask enabled. The ALT pin only indicates the PG_STATUS# falling edge, which means V_{OUT} has gone from a suboptimal to a good transition
1	BUSY_FAULT_MASK	0: No mask (default) 1: Mask enabled
0	CML_FAULT_MASK	0: No mask (default) 1: Mask enabled

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% greater than the maximum load current. Select an inductor with a small DC resistance for optimal efficiency. The inductor value can be calculated with Equation (10):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (10)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be estimated with Equation (11):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (11)$$

If V_{IN} is 24V and V_{OUT} is 20V, choose L to be 8µH. For automotive input and PD applications, choose the inductor ripple current to be approximately 30% to 50% of the maximum load current (see Table 1). It is recommended to use a fully shielded inductor to improve EMI performance.

Table 1: Recommended L for Different f_{SW} Values (D_{MAX} at ΔI_L = 30% to 50% of IO_MAX)

V_{IN} / V_{OUT} (below)	f_{SW} = 250kHz	f_{SW} = 420kHz	f_{SW} = 1.1MHz	f_{SW} = 2.1MHz
V_{IN} = 12V Buck1/2 = 5V I_{OUT} = 3A	8.2µH	4.7µH	2.2µH	1µH
V_{IN} = 24V Buck1/2 = 20V I_{OUT} = 3A	10µH	8.2µH	2.2µH	1µH

Selecting theBuck Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low-ESR capacitors for optimum performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For CLA applications, a 100µF electrolytic capacitor and two 10µF ceramic capacitors are recommended.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be calculated with Equation (12):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (12)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, estimated with Equation (13):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (13)$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with Equation (14):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (14)$$

Selecting Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Calculate the output voltage ripple with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (15)$$

Where L_1 the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (16):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (16)$$

The MPQ4272-UC's loop compensation is optimized for ceramic output capacitors.

Generally, 4pcs 22µF ceramic output capacitors are recommended for good loop stability and transient response. The bandwidth is about 1/10 of the switching frequency, with a phase margin exceeding 45°.

For polymer capacitor designs, the ESR zero frequency must exceed the internal, high-frequency compensation pole. It is recommended for the ESR to be below or equal to 1 / (2 x π x C_{OUT} x f_{SW}). Table 2 lists the recommended C_{IN} and C_{OUT} values for different output power ratings.

Table 2: Recommended C_{IN} and C_{OUT} Values for Different Output Power Ratings at f_{SW} = 420kHz

Maximum Output	Input Capacitor	Output Capacitor
V_{IN} = 12V Buck1/2 = 5V/9V, I_{OUT} = 3A	**4 x 22µF + 2 x 0.1µF**	**4 x 22µF + 0.1µF**
	22µF: Ceramic capacitor, 25V	22µF: Ceramic capacitor, 25V
	100nF: Ceramic capacitor, 25V	100nF: Ceramic capacitor, 10V
V_{IN} = 24V Buck1/2 = 5V, 9V, 15V, or 20V, I_{OUT} = 3A	**100µF + 3 x 10µF + 2 x 0.1µF**	**100µF + 22µF + 4.7µF**
	100µF: Electrolytic capacitor, 35V	100µF: Electrolytic capacitor, ESR < 50mΩ, 25V
	10µF: Ceramic capacitor, 35V	22µF: Ceramic capacitor, 25V
	100nF: Ceramic capacitor, 50V	4.7µF: Ceramic capacitor, 25V

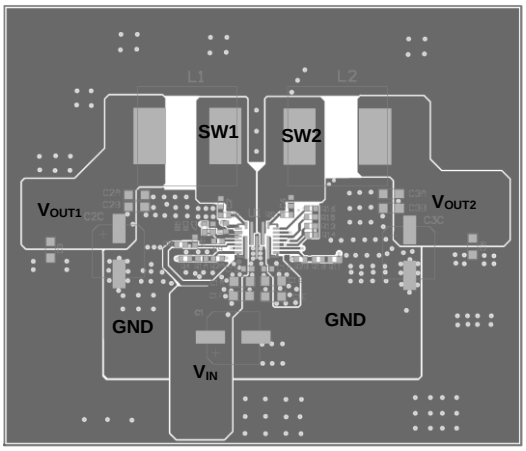
PCB Layout Guidelines (10)

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 15 and follow the guidelines below:

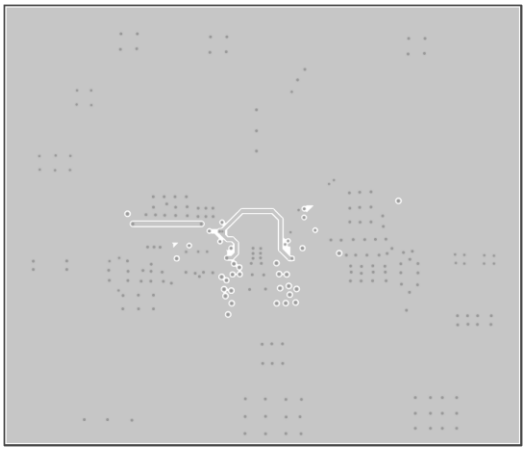
1. Use short, direct, and wide traces to connect the output nodes.
2. Place vias to GND after the output filter if required.
3. Use a large copper plane for PGND. Add multiple vias to improve thermal dissipation.
4. Connect AGND to PGND.
5. To improve EMI performance, place ceramic input decoupling capacitors as close as possible to VIN1, VIN2, and PGND.
6. Add two 0.1µF ceramic capacitors close to the VIN1 and VIN2 pins, respectively.
7. Place the input filter on the bottom layer to improve EMI performance.
8. Place the VCC decoupling capacitor as close to VCC as possible.

Note:

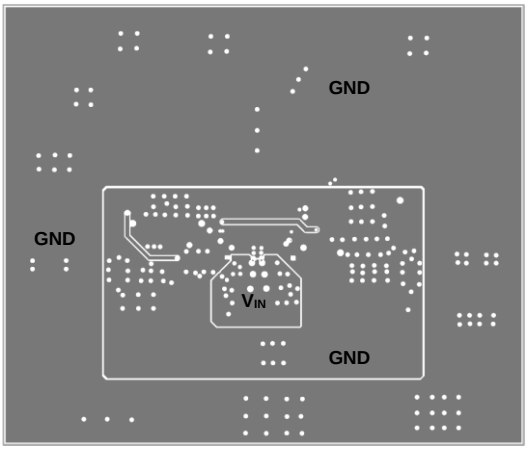
10) The recommended layout is based on the typical application circuit (see Figure 16 on page 38).



Top Layer



Mid-Layer 1



Bottom Layer

Figure 15: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

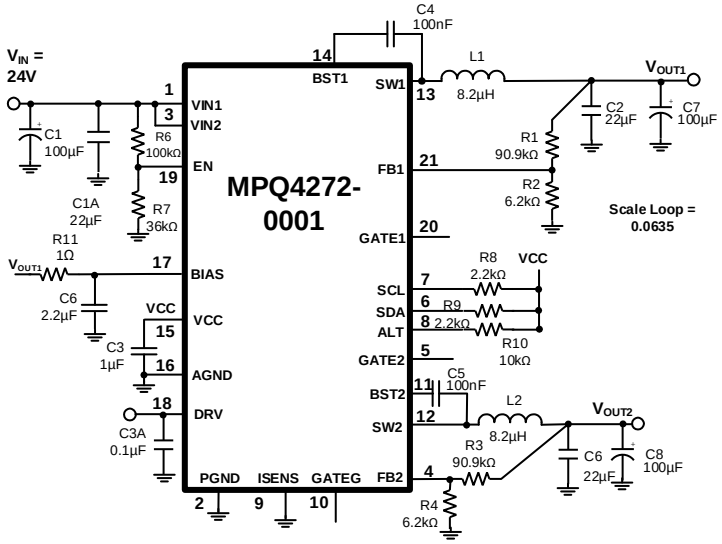


Figure 16: V_{IN} = 24V, V_{OUT1} = V_{OUT2} = 3.3V to 21V (Default Off)

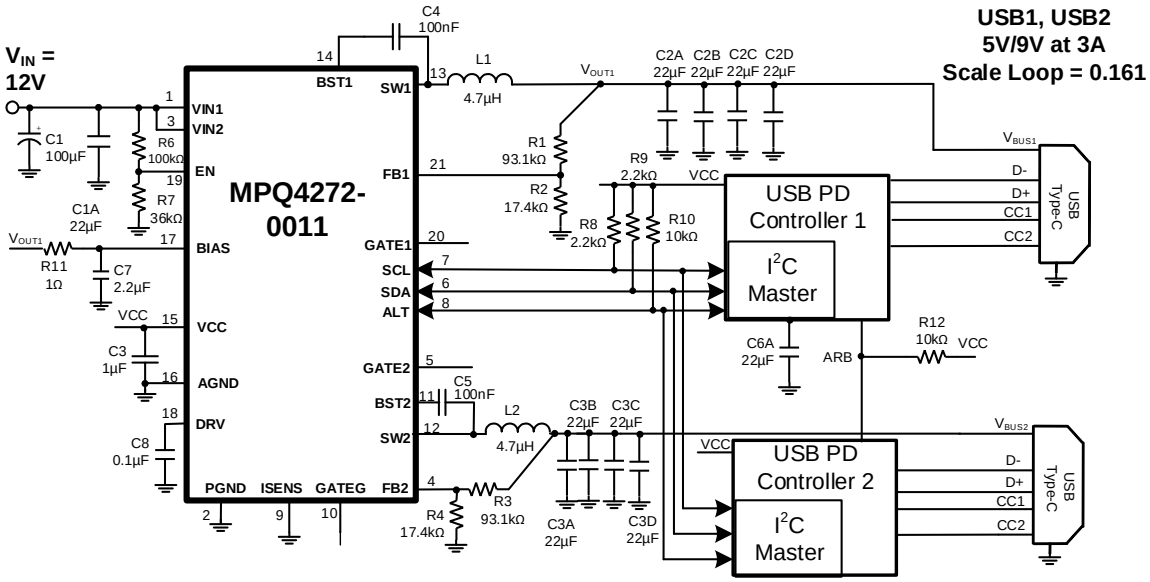


Figure 17: V_{IN} = 12V, USB1 = 5V/9V at 3A, USB2 = 5V/9V at 3A

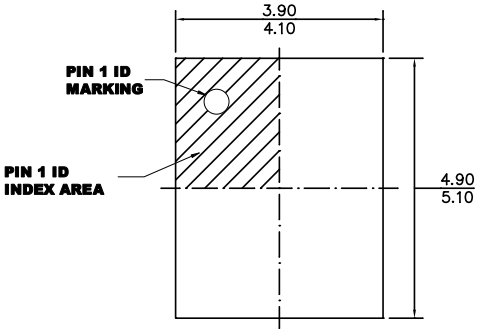
OTP REGISTER VALUE SELECTED TABLE BY DEFAULT (MPQ4272-0001)

OTP Items	Description	Default Value
GATE1_2_EN	Enables/disables	Disabled
I²C address	Sets the I²C slave address, bits[A5~A1]	61h
FREQ	Sets the buck switching frequency	420kHz
Slew rate	Sets the adjustable V_{REF} slew rate	0.4mv/μs V_{REF} rising slew rate; 0.1mv/μs V_{REF} falling slew rate
Dither enable	Enables/disables frequency spread spectrum	Disabled
DRV voltage	Driver pin V_{OUT} (LDO output)	6V
Phase delay	Selects the buck switching clock's phase delay (from buck 1 to buck 2)	0° phase delay
Over-temperature protection threshold	Thermal shutdown protection (TSD) threshold	170°C
Over-temperature protection warning threshold	Thermal warning threshold	150°C
OTP configuration code	OTP configuration code (defined by MPS)	0x01

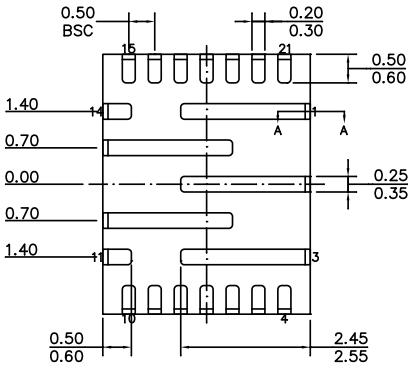
OTP Items	Description	CH1 Default Value	CH2 Default Value
OPERATION	MPQ4272 default is on or off	Off	Off
V_{OUT}	Output voltage	5V	5V
V_{OUT} scale loop	1 / (V_{OUT} feedback ratio)	0.0635	0.0635
EN OVP	Enables/disables output over-voltage protection (OVP)	Enabled	Enabled
Hiccup timer	Over-current protection (OCP) off timer	500ms	500ms
Output discharge EN	Enables/disables	Enabled	Enabled
Dropout EN	Frequency decreases in dropout mode	Enabled	Enabled
PFM/PWM mode	Auto-PFM/PWM or forced PWM mode	Forced PWM mode	Forced PWM mode
Current limit	Output current limit	3.6A	3.6A
Line drop compensation gain	μA/A	0μA/A	0μA/A
V_{OUT} mask	Mask or no mask for the ALT pin indication	Masked	Masked
I_{OUT}/P_{OUT} mask		Not masked	Not masked
Input mask		Masked	Masked
Temperature mask		Not masked	Not masked
PG_STATUS mask		Masked	Masked
PG_ALT_EDGE mask		Masked	Masked
Other mask		Masked	Masked

PACKAGE INFORMATION

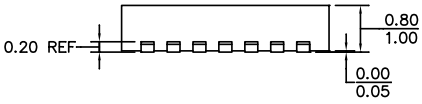
QFN-21 (4mmx5mm) with Wettable Flanks



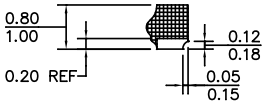
TOP VIEW



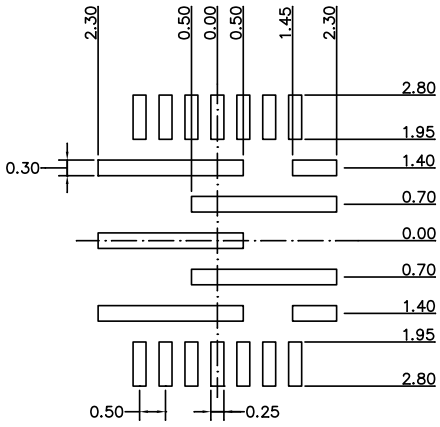
BOTTOM VIEW



SIDE VIEW



SECTION A-A

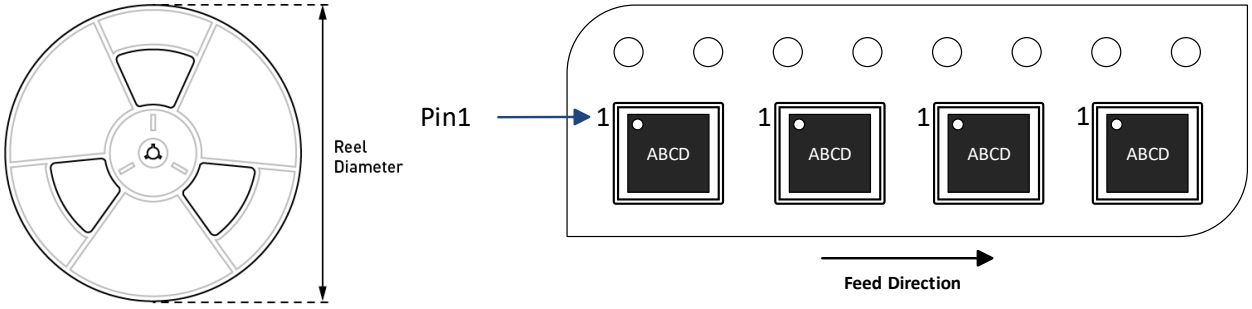


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PINS 1, 2, AND 3, AND PINS 12 AND 13 HAVE THE SAME LENGTH AND WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4272GVE-xxxx-AEC1-Z	QFN-21 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/24/2021	Initial Release	-