ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE74160, NTE74161, NTE74162, NTE74163 Integrated Circuit TTL – Synchronous 4–Bit Counters

Description:

The NTE74160 thru NTE74163 are synchronous, presettable counters in a 16–Lead DIP type package that feature an internal carry look–ahead for application in high–speed counting designs. The NTE74160 and NTE74162 are decade counters and the NTE74161 and NTE74164 are 4–bit binary counters. Synchronous operation is provided by having all flip–flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count–enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip–flops on the rising edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low–to–high transitions at the load input of the NTE74160 thru NTE74163 should be avoided when the clock is low if the enable inputs are high at or before the transition The clear function for the NTE74160 and NTE74161 is asynchronous and a low level at the clear input sets all four of the flip–flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function of the NTE74162 and NTE74163 is synchronous and a low level at the clear input sets all four flip–flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). low–to–high transitions at the clear input of the NTE74162 and NTE74163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition

The carry look–ahead circuitry provides for cascading counters for n–bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count–enable inputs and a ripple carry output. Both count–enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high–level output pulse with a duration approximately equal to the high–level portion of the Q_A output. This high–level overflow ripple carry pulse can be used to enable successively cascaded stages. High–to–low–level transitions at the enable P or T inputs should occur only when the clock input is high.

Features:

- Available in 4 Types:
  - Decade with Direct Clear: NTE74160
  - Binary with Direct Clear: NTE74161
  - Decade with Synchronous Clear: NTE74162
  - Binary with Synchronous Clear: NTE74163
- Internal Look−Ahead for Fast Counting
- Carry Output for n−Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode−Clamped Inputs

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 5.5V
Interemitter Voltage (Note 2) 5.5V
Power Dissipation, P_D 305mW
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . −65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.
Note 2. This is the voltage between two emitters of a multiple−emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	−	−	−800	μA
Low−Level Output Current	I_{OL}	−	−	16	mA
Clock Frequency	f_{clock}	0	−	25	MHz
Width of Clock Pulse	$t_{w(clock)}$	25	−	−	ns
Width of Clear Pulse	$t_{w(clear)}$	20	−	−	ns
Setup Time	t_{su}				
Data Inputs A, B, C, D		20	−	−	ns
$\overline{ENP}$		20	−	−	ns
$\overline{LOAD}$		25	−	−	ns
$\overline{CLR}$ (Note 3)		20	−	−	ns
Hold Time at Any Input	t_h	0	−	−	ns
Operating Temperature Range	T_A	0	−	+70	°C

Note 2. This applies only for NTE74162 and NTE74163, which have synchronous clear inputs.

Electrical Characteristics: (Note 4, Note 5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2	–	–	V
Low Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA	2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current CLK or ENT	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	80	μA
All Other Inputs			–	–	40	μA
Low Level Input Current CLK or ENT	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−3.2	mA
All Other Inputs			–	–	−1.6	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 6	−18	–	−57	mA
Supply Current, All Outputs High	I_{CCH}	V_{CC} = MAX, Note 7	–	59	94	mA
Supply Current, All Outputs Low	I_{CCL}	V_{CC} = MAX, Note 8	–	63	101	mA

Note 4. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 5. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 6. Not more than one output should be shorted at a time and duration of short−circuit should not exceed one second.

Note 7. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

Note 8. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 400Ω, C_L = 15pF, Note 9	25	32	–	MHz
Propagation Delay Time (From CLK Input to RCO Output)	t_{PLH}		–	23	35	ns
	t_{PHL}		–	23	35	ns
Propagation Delay Time (From CLK Input to Any Output)	t_{PLH}		–	13	20	ns
(From $\overline{LOAD}$ Input Low to Q Output)	t_{PHL}		–	15	23	ns
Propagation Delay Time (From CLK Input to Any Output)	t_{PLH}	R_L = 2kΩ, C_L = 15pF, Note 8	–	17	25	ns
(From $\overline{LOAD}$ Input High to Q Output)	t_{PHL}		–	19	29	ns
Propagation Delay Time (From ENT Input to RCO Output)	t_{PLH}		–	11	16	ns
	t_{PHL}		–	11	16	ns
Propagation Delay Time (From $\overline{CLR}$ Input to Any Q Output)	t_{PLL}		–	26	38	ns

Note 9. .Propagation delay for clearing is measure from the clear input for the NTE74160 and NTE74161 or from the clock transition for the NTE74162 and NTE74163.

Pin Connection Diagram