UM11772

TEA2093DB2202 synchronous rectifier evaluation board

Rev. 1 — 13 June 2022 User manual

Document information

Information	Content
Keywords	TEA2093DB2202, TEA2093TS, asymmetrical half-bridge converter, synchronous rectifier (SR) driver, TSOP-6, high efficiency, power supply, evaluation board
Abstract	This user manual describes the TEA2093DB2202 evaluation board. A functional description is provided, including instructions about how to connect the board, for the best results and performance. The TEA2093DB2202 evaluation board contains the secondary part of a single output asymmetrical half-bridge converter, excluding the output capacitors and the feedback control hardware. To use the TEA2093DB2202 evaluation board correctly, an asymmetrical half-bridge converter board in which the evaluation board can replace the secondary rectifier part is required.

Revision history

Rev	Date	Description
v.1	20220613	Initial version

1 Important notice

IMPORTANT NOTICE

For engineering development or evaluation purposes only

NXP provides the product under the following conditions:

This evaluation kit is for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed-circuit board to make it easier to access inputs, outputs and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by connecting it to the host MCU computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application heavily depends on proper printed-circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The product provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end device incorporating the product. Due to the open construction of the product, it is the responsibility of the user to take all appropriate precautions for electric discharge. In order to minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

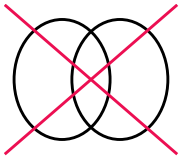
2 Safety warning

The board application is AC-mains voltage powered. Avoid touching the board while it is connected to the mains voltage and when it is in operation. An isolated housing is obligatory when used in uncontrolled, non-laboratory environments. Galvanic isolation from the mains phase using a fixed or variable transformer is always recommended.

Figure 1 shows the symbols on how to recognize these devices.

019aab173

a. Isolated



019aab174

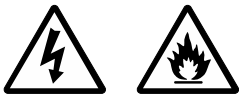
b. Not isolated

Figure 1. Isolation symbols

3 Introduction

WARNING

Lethal voltage and fire ignition hazard



The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

The TEA2093DB2202 evaluation board and user manual are intended for engineers involved in the evaluation and the design of switch-mode power supplies (SMPS).

This document contains all the information required to replace the secondary-side rectification of an existing SMPS with an asymmetrical half-bridge topology with the TEA2093DB2202 evaluation board.

4 Finding kit resources and information on the NXP website

NXP Semiconductors provides online resources for this user manual and its supported devices at https://www.nxp.com.

This design example user manual can be found at: https://www.nxp.com/TEA22093DB2202.

4.1 Collaborate in the NXP community

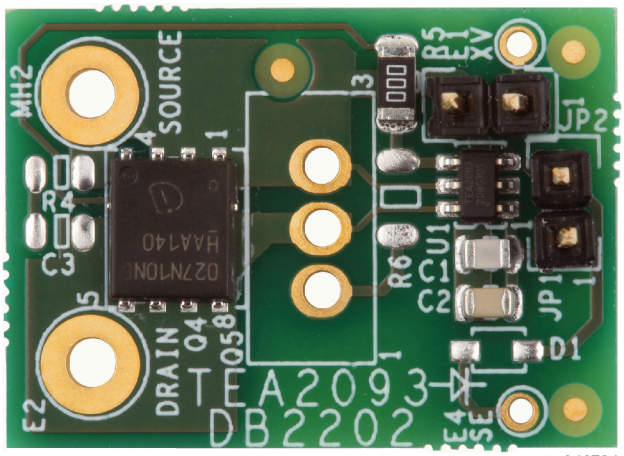
In the NXP community you can share ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community can be found at https://community.nxp.com.

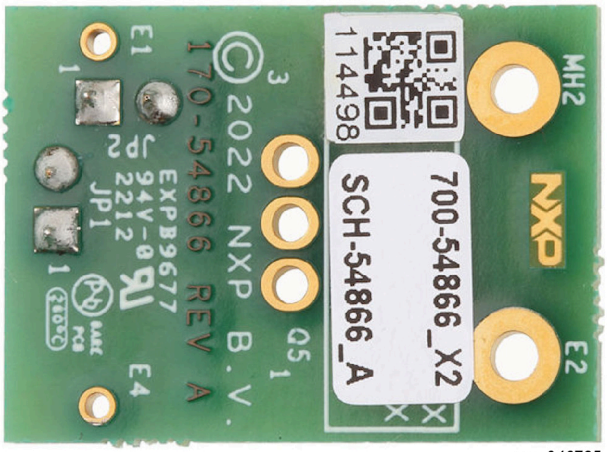
5 Getting ready

5.1 Box contents

The box contains the TEA2093DB2202 evaluation board, which incorporates the TEA2093TS in a TSOP-6 package and a MOSFET in a TDSON-FL package with a typical R_{DSon} of 2.3 mΩ. Figure 2 shows the front side and the back side of the TEA2093DB2202 evaluation board. The TEA2093DB2202 evaluation board is a single-layer board, which includes plated-through vias for external connections and a TO-220 MOSFET as a replacement for the mounted MOSFET Q4.



a. Top side



b. Bottom side

Figure 2. TEA2093DB2202 evaluation board photographs

5.2 Additional hardware

The TEA2093DB2202 evaluation board must be placed on an existing SMPS. Details can be found in Section 6.3 and Section 7.

6 Getting to know the hardware

6.1 Overview

The TEA2093DB2202 evaluation board contains a TEA2093TS SR controller in a TSOP-6 package and a 100 V MOSFET in a TDSON-FL package. It replaces the secondary-side rectification part of an SMPS with an asymmetrical half-bridge topology. Additionally, the TEA2093DB2202 evaluation board contains an option to replace the mounted MOSFET by a MOSFET in a TO-220 package.

The TEA2093TS is a dedicated controller IC for synchronous rectification (SR) on the secondary side of asymmetrical half-bridge converters. It incorporates the sensing stage and the driver stage for driving the SR MOSFET, which rectifies the output of the secondary transformer winding.

The TEA2093TS can generate its own supply voltage or operate with an external applied voltage. The self-supply function is intended for: .

- Battery-charging applications with a 2 V (USB BC) output voltage
- Applications with high-side rectification without an auxiliary winding
- Multiple output voltage applications with or without auxiliary winding

6.2 Features

- Easy replacement of secondary-side rectifier
- A 100 V/2.7 mΩ MOSFET is incorporated
- Self-supplying for low-side rectification with low output voltage (CC mode)
- Self-supplying for high-side rectification without the use of an auxiliary winding
- Operates with standard-level and logic-level SR MOSFETs

6.3 Block diagram

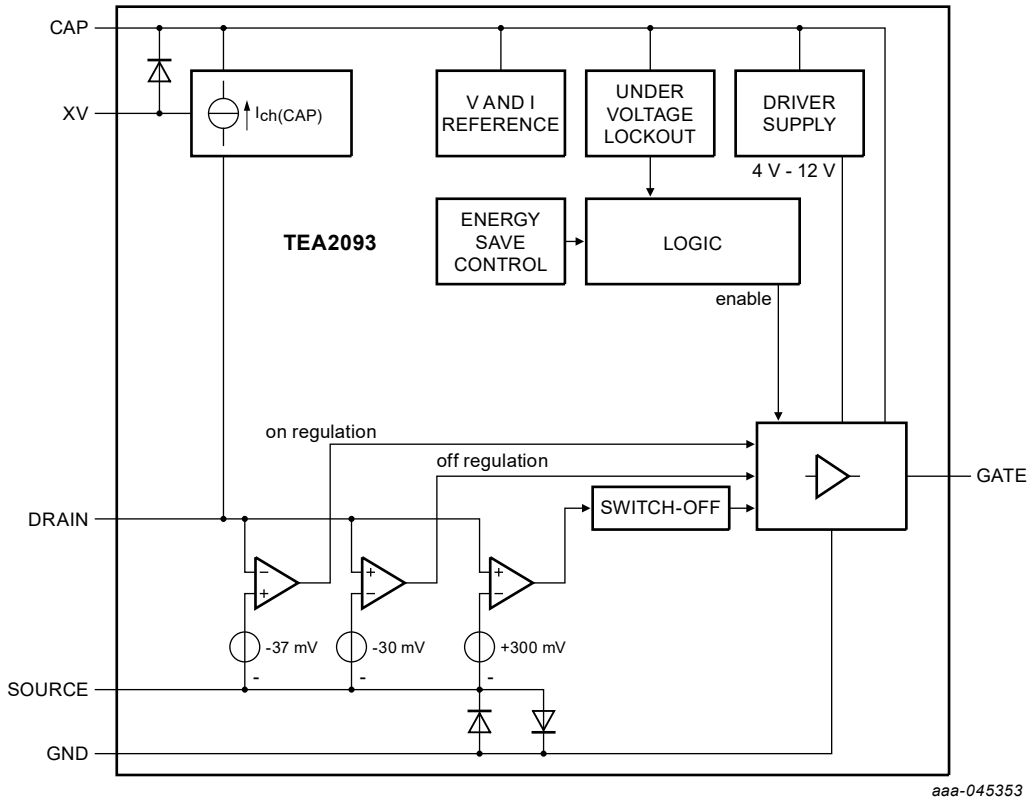


Figure 3. TEA2093TS block diagram

6.4 Board description

The board incorporates the TEA2093TS SR controller and a power MOSFET. The TEA2093TS acts as a controlled amplifier. The input is the voltage difference between the DRAIN and the SOURCE pins. The corresponding gate driver signal is the output. The amplifier regulates the source-to-drain voltage difference to 37 mV in the rectification phase.

To facilitate easy layout design for a single-sided board, resistors R1 and R2 are added. They must be between 0 Ω and 10 Ω. For the fastest turn-off time, use the lowest value. By default, the TDSON-FL MOSFET Q4 is mounted with a 0 Ω gate resistor (R1). It is also possible to mount a TO220 MOSFET Q5 with gate resistor R2. Capacitors C1 and C2 are decoupling capacitors for the V_{CC} of the TEA2093TS.

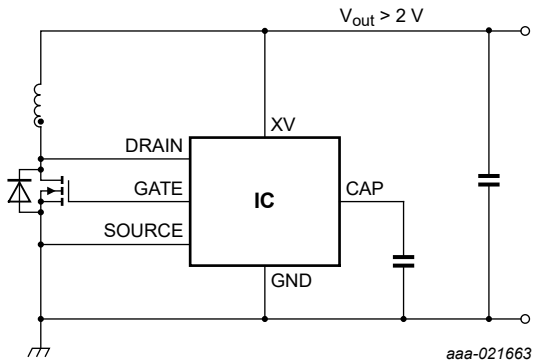
To ensure sufficient charge power during the secondary stroke to drive the external MOSFET, a value of 100 nF is used for capacitor C2. To prevent unwanted oscillation of the V_{CC} supply, capacitor C1 is added. A provision is made for snubber R3/C3. The components are not mounted. However, if high-voltage spikes occur on the drain-source connections of the MOSFETs, they can be added. To facilitate optimal configurations for either the low-side or the high-side connection, jumpers JP1 and JP2 are added (see the diagrams in Section 7).

7 Configuring the hardware

7.1 Connected at low-side SR

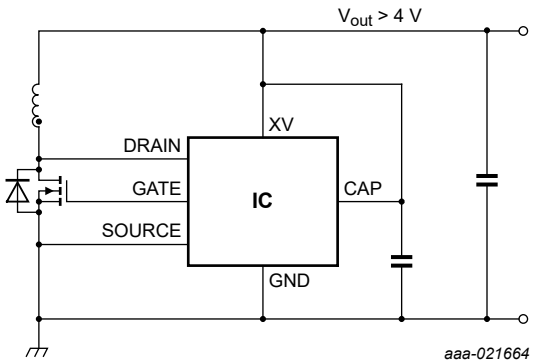
The TEA2093DB2202 evaluation board must be incorporated in an existing asymmetrical half-bridge SMPS.

Figure 4 shows the connection of the TEA2093DB2202 evaluation board to the secondary side of an asymmetrical half-bridge SMPS as low-side SR.



(1) Jumpers JP1 and JP2 are both not placed
(2) Supply via DRAIN pin (V_{out} = 2 V to 4.7 V)
(3) Supply via V_{out} (> 4.7 V)

a. Constant current (CC)/constant voltage (CV) mode



(1) Jumper JP1 is placed; jumper JP2 is not placed
(2) Supply via V_{out} (> 4 V)

b. Constant voltage (CV) mode

Figure 4. TEA2093DB2202 evaluation board configuration with low-side rectification

Figure 4(a) shows the configuration for SR low-side applications, which include CC mode (for example, USB BC specification for an operation between 2 V and 5 V). When V_{out} ≥ 4.7 V, the TEA2093TS uses the voltage on the XV pin as supply. The resulting voltage on the CAP pin is typically 0.7 V below the voltage on the XV pin. It is used as supply voltage for the gate drive output to the external MOSFET.

When V_{out} < 4.7 V (CC mode), the TEA2093TS uses the pulsed voltage on the drain input to generate the voltage for the CAP pin. When 0 V < V_{out} < 4.7 V, the regulated voltage on the CAP pin is 4.0 V (typical).

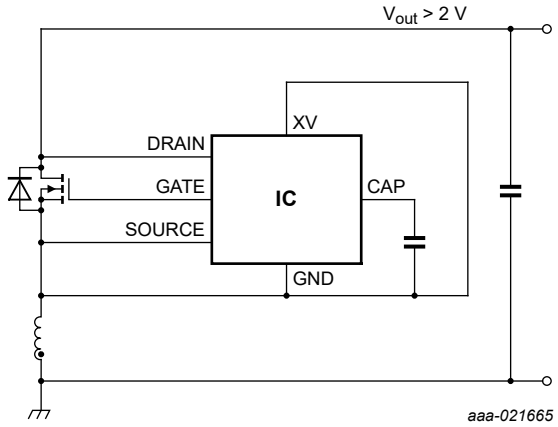
Figure 4(b) shows the configuration for SR low-side application for CV mode only. V_{out} must be ≥ 4 V. In this case, the CAP pin can be connected directly to the XV pin. The result of connecting the CAP pin directly to the XV pin is 0.7 V additional gate drive voltage compared to the configuration in Figure 4(a). To achieve the best efficiency, the additional gate drive voltage drives the external MOSFET to a lower R_{DSon}. The maximum gate drive voltage is 12 V.

Maximum voltage ratings for TEA2093TS pins:

- Pins XV and CAP: 38 V
- Pin DRAIN: 120 V

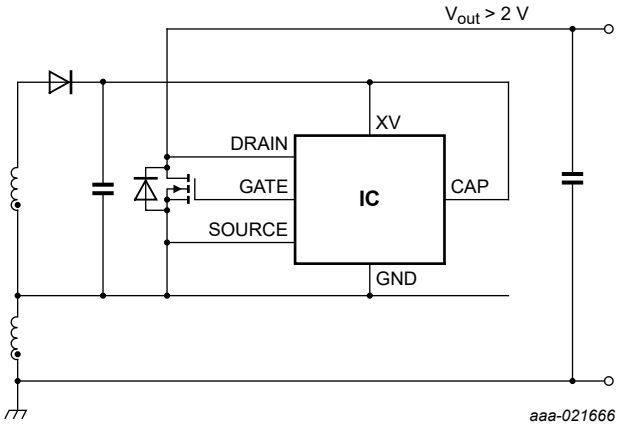
7.2 Connected at high-side SR

Figure 5 shows the connection of the TEA2093DB2202 evaluation board to the secondary side of an asymmetrical half-bridge SMPS as high-side SR.



(1) Jumper JP1 is not placed; jumper JP2 is placed

a. Supply via the DRAIN input (> 2 V)



(1) Jumper JP1 is placed; jumper JP2 is not placed

b. Supply via auxiliary winding

Figure 5. TEA2093DB2202 evaluation board configuration with high-side rectification

Figure 5(a) shows the configuration for SR high-side applications with self-supply. In this case, the TEA2093TS retrieves its supply from the pulsed voltage on the DRAIN input. The regulator inside the TEA2093TS converts these pulses to regulated DC voltage of approximately 9 V. If the XV pin is connected to the IC ground, the TEA2093TS generates 9 V. This voltage is present on the CAP pin. It is the reference voltage for the gate drive of the external MOSFET.

Figure 5(b) shows the configuration for SR high-side application which is supplied by an additional auxiliary winding. This configuration can deliver the best possible efficiency for high-side application.

If the auxiliary voltage drops to below 4 V for the lower output voltages in a multiple-outputs application, the TEA2093TS generates its own supply voltage. It maintains a minimum supply of 4 V on the CAP pin. The auxiliary voltage can then be optimized for the higher output voltages. In this way, maximum efficiency at maximum power is achieved.

Maximum voltage ratings for TEA2093TS pins:

- Pins XV and CAP: 38 V
- Pin DRAIN: 120 V

8 Schematic, board layout and bill of materials

8.1 Schematic

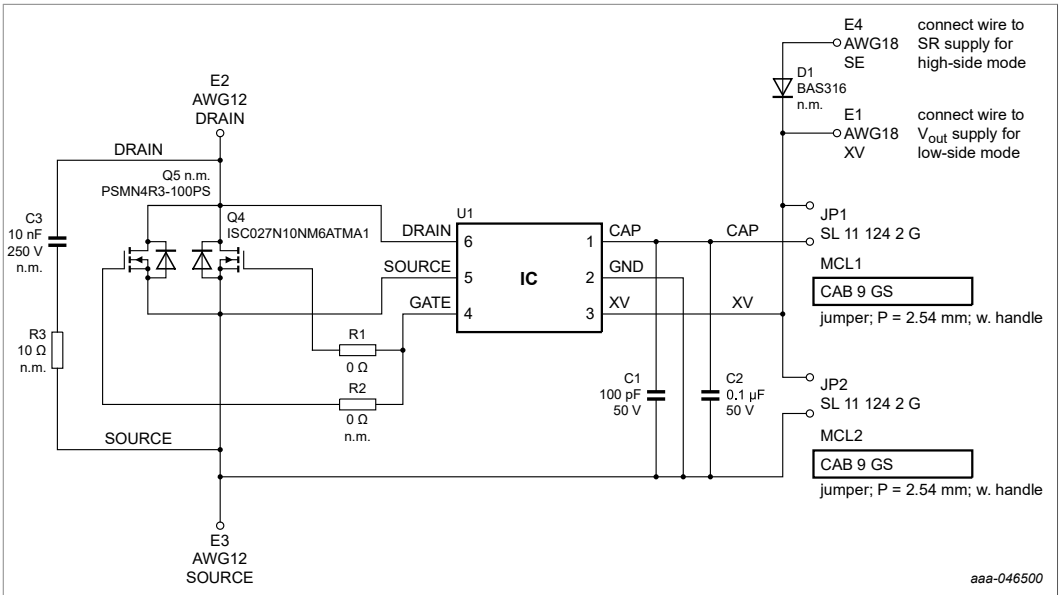


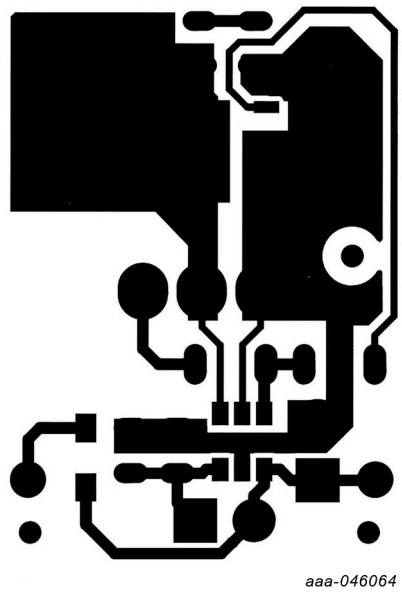
Figure 6. TEA2093DB2202 evaluation board schematic diagram

8.2 Bill of materials (BOM)

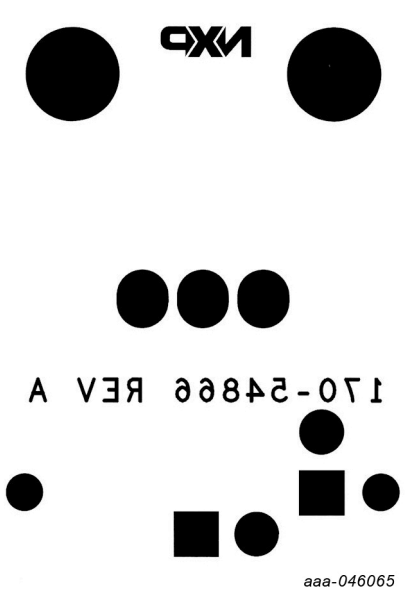
Table 1.

Reference	Description and values	Part number	Manufacturer
C1	capacitor; 100 pF; 50 V; 0805	08055A101KAT2A	AVX
C2	capacitor; 0.1 µF; 50 V; 0805	X7R0805HTTD104K	Koa Speer
C3	capacitor; not mounted; 10 nF; 250 V; 0805	CGA4J3X7R2E103K125AA	TDK
D1	diode; not mounted; SOD323	BAS316	Nexperia
JP1; JP2	header; straight; 1 × 2-way	SL 11 124 2 G	Fischer
MCL1; MCL2	jumper; with handle; P = 2.54 mm	CAB 9 GS	Fischer
R1	resistor; 0 Ω; 1206	CRCW12060000Z0EA	Vishay
R2	resistor; not mounted; 0 Ω; 1206	CRCW12060000Z0EA	Vishay
R3	resistor; not mounted; 10 Ω; 0805	CR0805-JW-100ELF	Bourns
Q4	MOSFET; TDSON-FL	ISC027N10NM6ATMA1	Infineon
Q5	MOSFET; not mounted; TO220AB	PSMN4R3-100PS	Nexperia
U1	SR controller; TSOP6	TEA2093TS	NXP Semiconductors

8.3 Layout



a. Top



b. Bottom

Figure 7. TEA2093DB2202 evaluation board layout

Below are several important guidelines for a good layout:

- Keep the trace from the DRAIN pin to the MOSFET drain as short as possible.
- Keep the trace from the SOURCE pin to the MOSFET source as short as possible.
- Keep the area of the loop from the DRAIN pin to the MOSFET drain, to the MOSFET source, and to the SOURCE pin as small as possible. Ensure that the overlap of this loop over the power drain track or the power source track is as small as possible. The two loops must not cross each other.
- Keep the track from the GATE pin to the gate of the MOSFET as short as possible.
- Use separate clean tracks for the XV and the GND pins. If possible, use a small ground plane underneath the IC, which improves the heat dispersion.
- Place capacitors C1 and C2 close to the IC

9 Abbreviations

Table 2. Abbreviations

Acronym	Description
CC	constant current
CV	constant voltage
MOSFET	metal-oxide-semiconductor field-effect transistor
SMPS	switch-mode power supply
SR	synchronous rectifier

10 References

[1] **TEA2093TS data sheet** — GreenChip synchronous rectifier controller; 2022, NXP Semiconductors

11 Legal information

11.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

11.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

11.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

GreenChip — is a trademark of NXP B.V.

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 June 2022
Document identifier: UM11772