



FQD17P06 / FQU17P06 P-Channel QFET® MOSFET

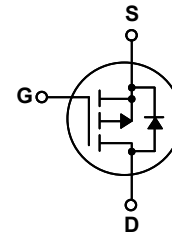
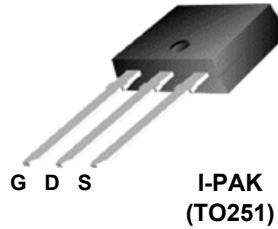
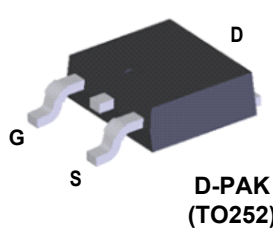
- 60 V, - 12 A, 135 mΩ

Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- -12 A, -60 V, $R_{DS(on)} = 135 \text{ m}\Omega$ (Max.) @ $V_{GS} = -10 \text{ V}$
- Low Gate Charge (Typ. 21 nC)
- Low C_{rss} (Typ. 80 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQD17P06 / FQU17P06	Unit
V_{DSS}	Drain-Source Voltage	-60	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	-12
		- Continuous ($T_C = 100^\circ\text{C}$)	-7.6
I_{DM}	Drain Current - Pulsed (Note 1)	-48	A
V_{GSS}	Gate-Source Voltage	± 25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	300	mJ
I_{AR}	Avalanche Current (Note 1)	-12	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-7.0	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	44	W
	- Derate above 25°C	0.35	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQD17P06 / FQU17P06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.85	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *, Typ.	50	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	110	

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-60	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C	--	-0.06	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	μA
		$V_{DS} = -48\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -6.0\text{ A}$	--	0.11	0.135	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -30\text{ V}, I_D = -6.0\text{ A}$	--	8.7	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	690	900	pF
C_{oss}	Output Capacitance		--	325	420	pF
C_{rss}	Reverse Transfer Capacitance		--	80	105	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -30\text{ V}, I_D = -8.5\text{ A},$ $R_G = 25\ \Omega$	--	13	35	ns
t_r	Turn-On Rise Time		--	100	210	ns
$t_{d(off)}$	Turn-Off Delay Time		--	22	55	ns
t_f	Turn-Off Fall Time		(Note 4)	--	60	130
Q_g	Total Gate Charge	$V_{DS} = -48\text{ V}, I_D = -17\text{ A},$ $V_{GS} = -10\text{ V}$	--	21	27	nC
Q_{gs}	Gate-Source Charge		--	4.2	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4)	--	10	--
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-12	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-48	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -12\text{ A}$	--	--	-4.0	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -17\text{ A},$	--	92	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$	--	0.32	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 2.4\text{ mH}, I_{AS} = -12\text{ A}, V_{DD} = -25\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq -17\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

Typical Characteristics

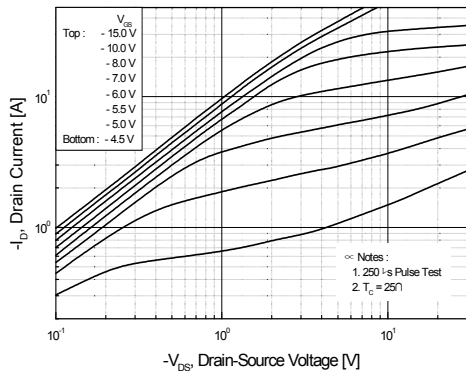


Figure 1. On-Region Characteristics

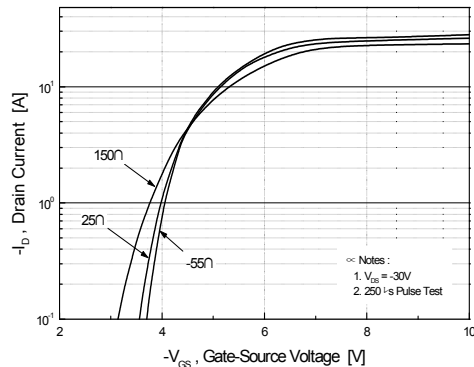


Figure 2. Transfer Characteristics

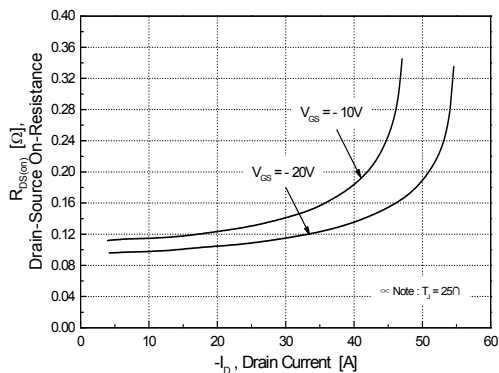


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

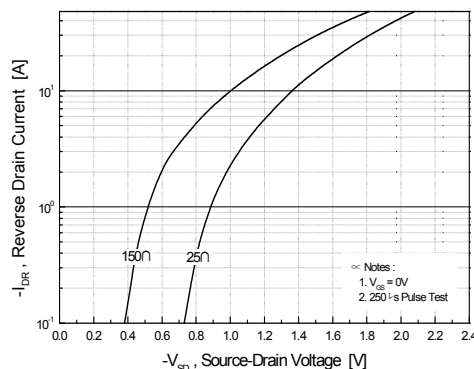


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

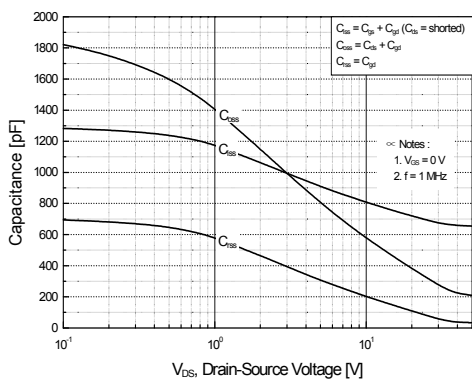


Figure 5. Capacitance Characteristics

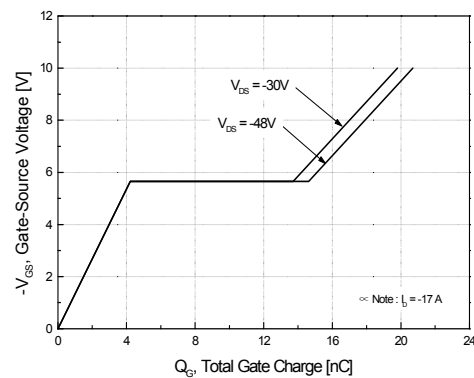


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

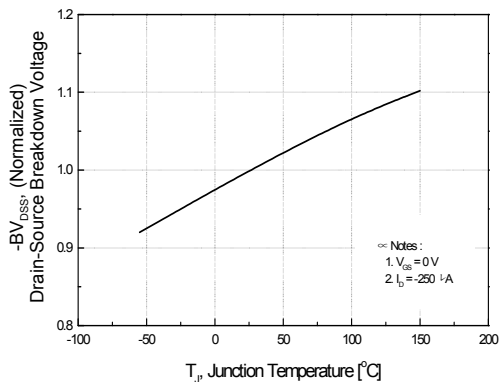


Figure 7. Breakdown Voltage Variation vs. Temperature

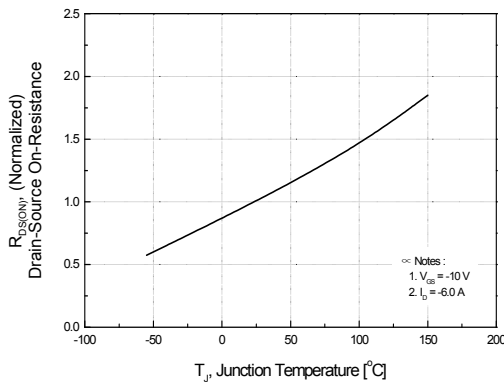


Figure 8. On-Resistance Variation vs. Temperature

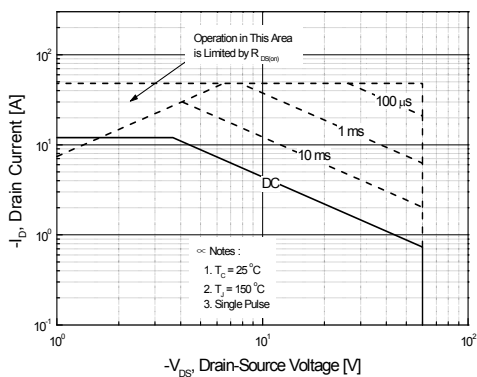


Figure 9. Maximum Safe Operating Area

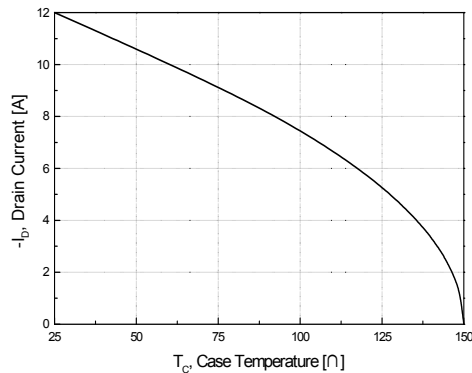


Figure 10. Maximum Drain Current vs. Case Temperature

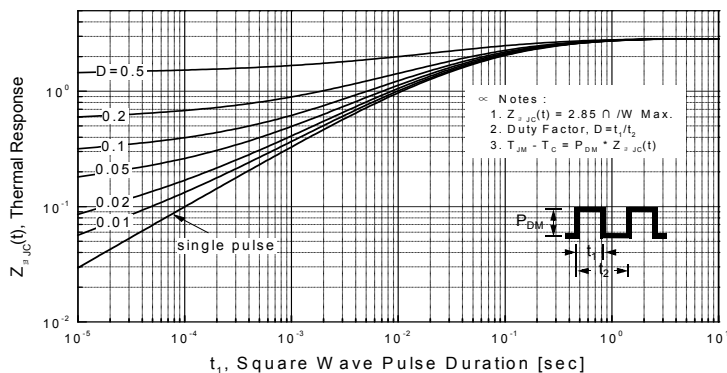
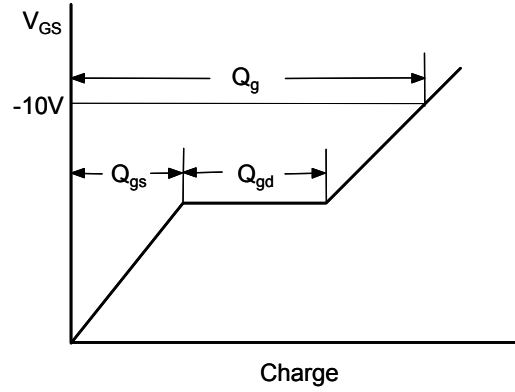
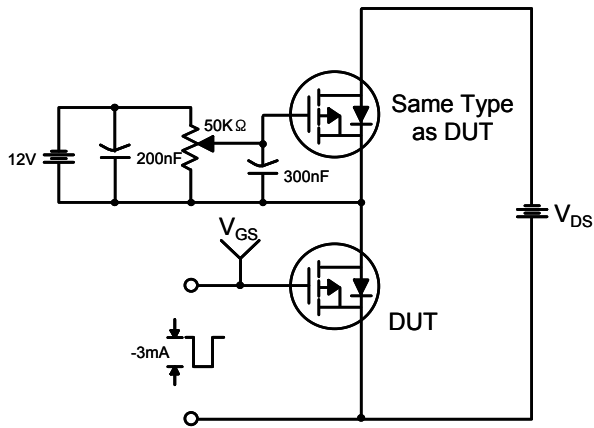
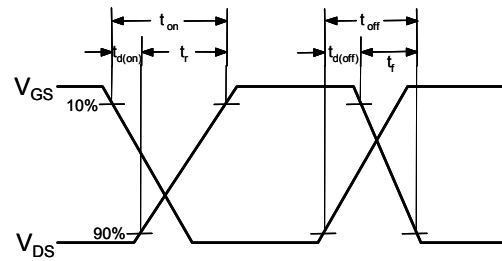
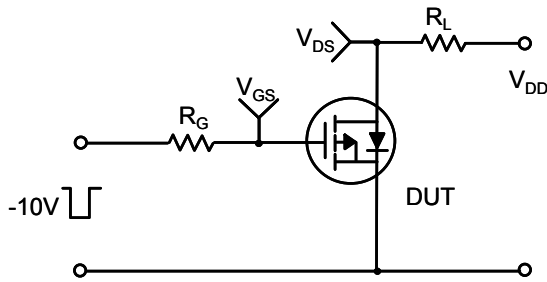


Figure 11. Transient Thermal Response Curve

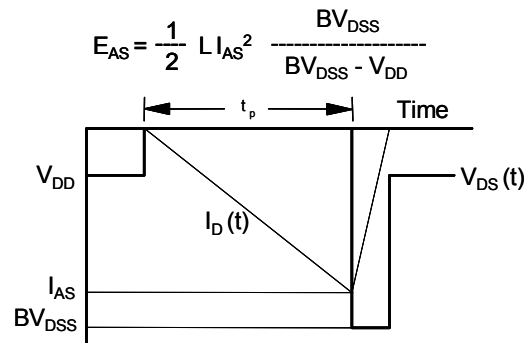
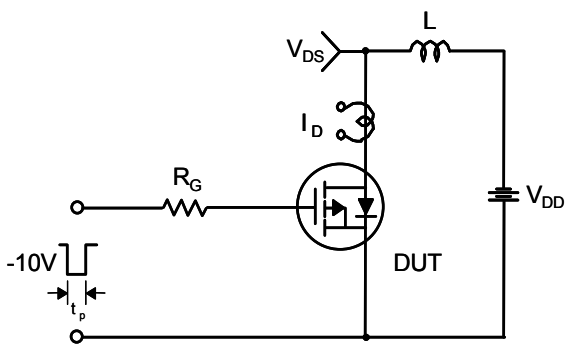
Gate Charge Test Circuit & Waveform



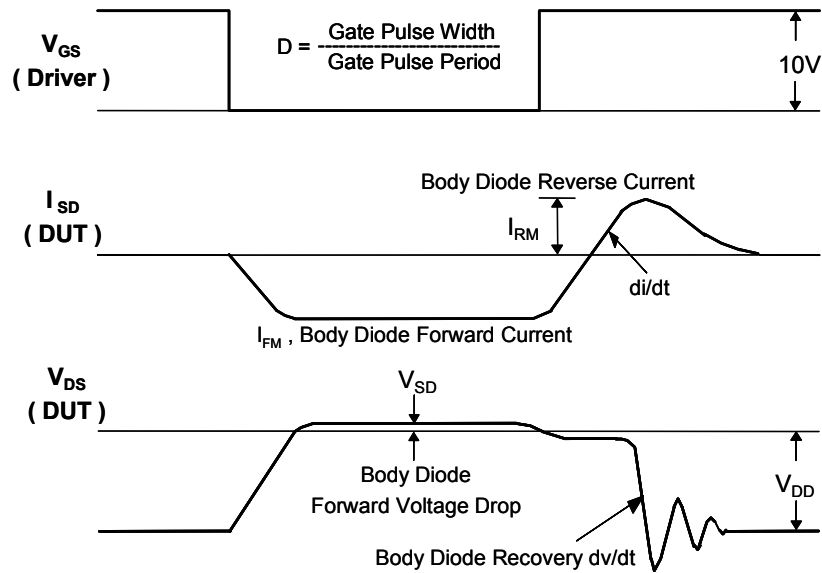
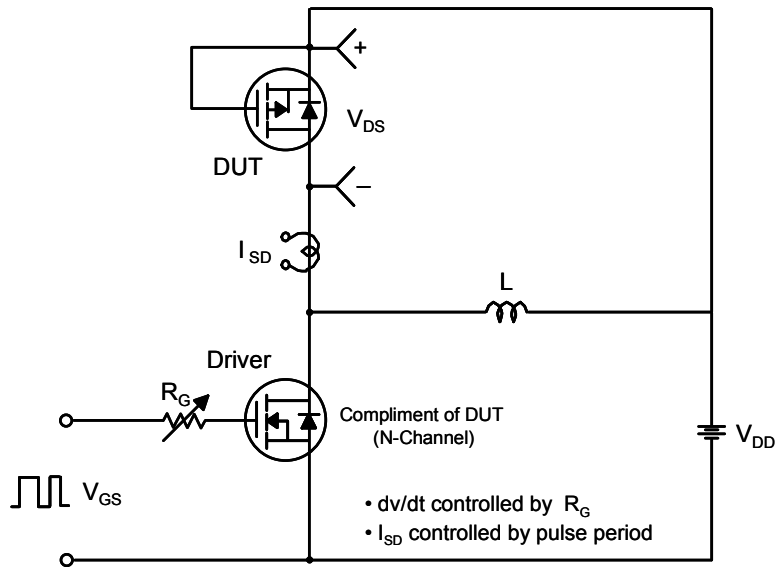
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

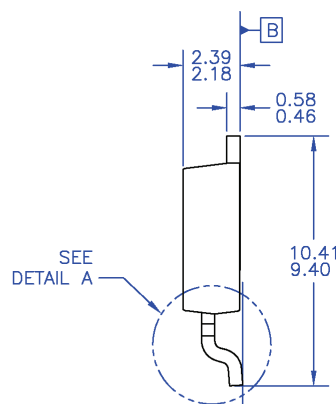
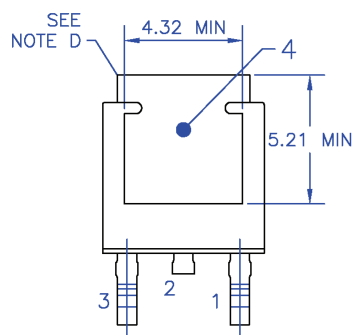
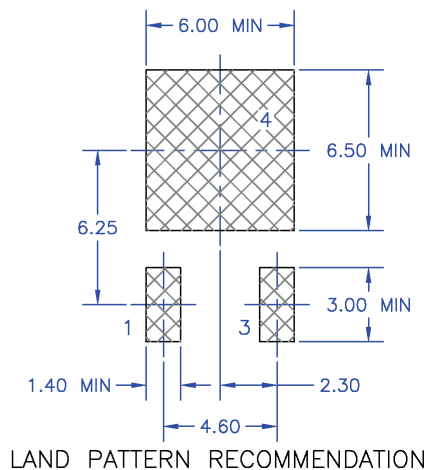
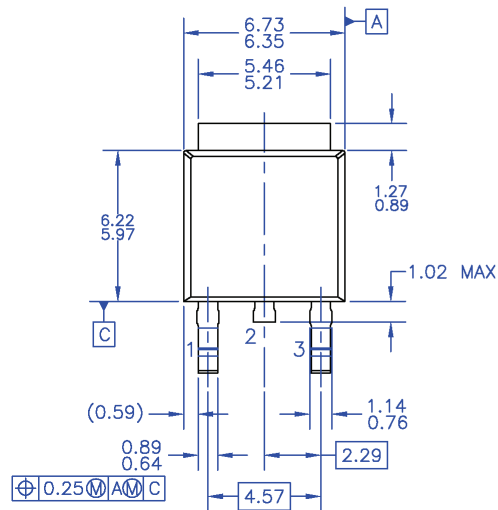


Peak Diode Recovery dv/dt Test Circuit & Waveforms

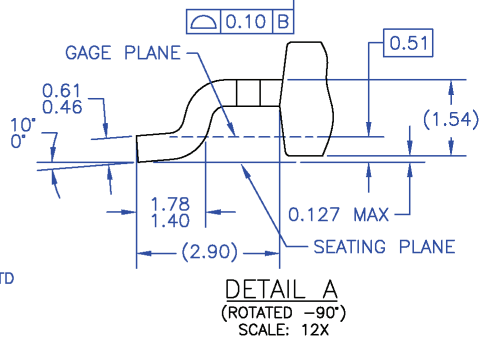


Mechanical Dimensions

D-PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8



TO-252 (DPAK) MOLDED, 3 LEAD, OPTION AA

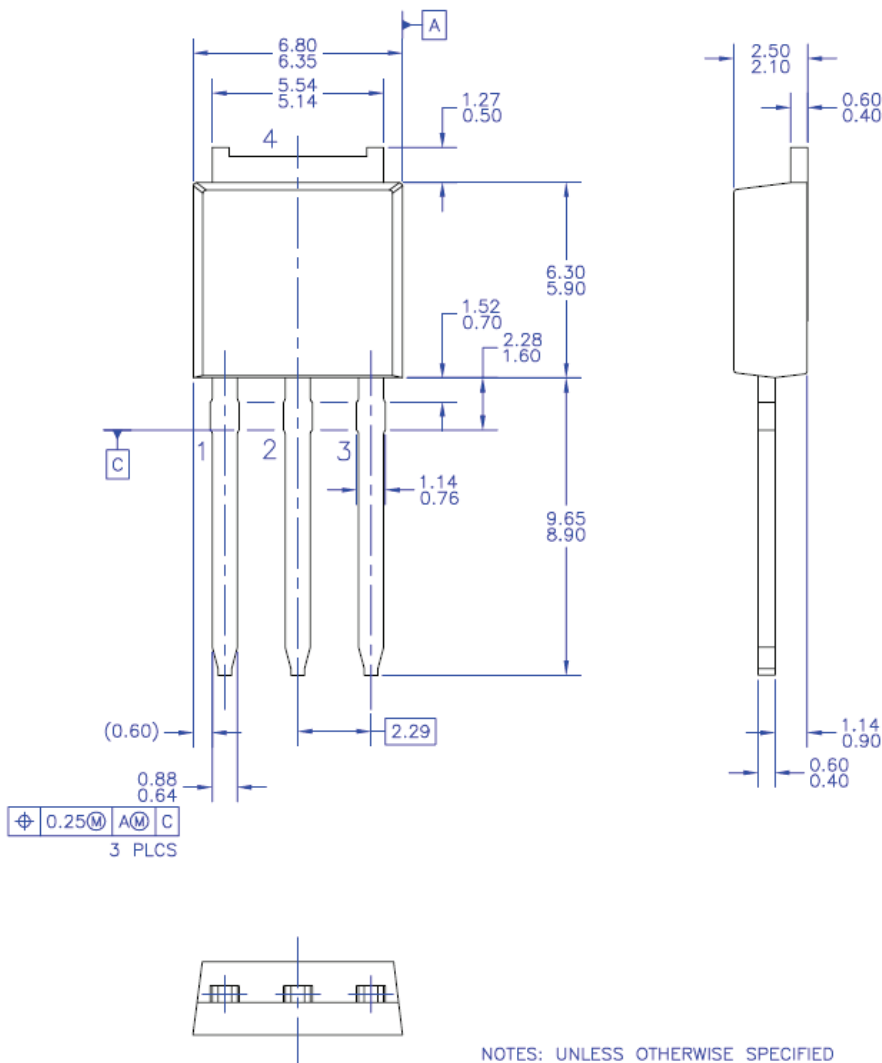
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Dimensions in Millimeters

Mechanical Dimensions

I-PAK



NOTES: UNLESS OTHERWISE SPECIFIED

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- B) THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

TO-251 (IPAK) MOLDED, 3LEAD, OPTION AA

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Dimensions in Millimeters



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| BitSiC™ | Global Power Resource SM | QFET® | TinyBuck™ |
| Build it Now™ | Green Bridge™ | QS™ | TinyCalc™ |
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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