OptiMOS®-P Small-Signal-Transistor

Features

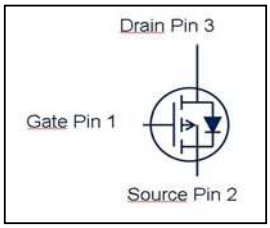
- P-Channel
- Enhancement mode
- Super Logic level (2.5 V rated)
- 150°C operating temperature
- Avalanche rated
- d*v*/d*t* rated
- Pb-free lead plating; RoHS compliant
- Qualified according to AEC Q101
- Halogen-free according to IEC61249-2-21

RoHS AEC Qualified Halogen-Free

Product Summary

V_{DS}	-20	V
$R_{DS(on),max}$	550	mΩ
I_D	-0.63	A

PG-SOT-323



Type	Package	Tape and Reel Information	Marking	Lead free	Packing
BSS 209PW	SOT-323	H6327: 1000 pcs/reel	X3s	Yes	Non Dry

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	-0.63	A
		T_C=70 °C	-0.5	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C	-2.5	
Avalanche energy, single pulse	E_{AS}	I_D= -0.63 A, R_{GS}=25 Ω	4.0	mJ
Reverse diode d*v*/d*t*	d*v*/d*t*	I_D= -0.63 A, V_{DS}=-16 V, d*i*/d*t* =-200 A/µs, $T_{j,max}$=150 °C	-6	kV/µs
Gate source voltage	V_{GS}		±12	V
Power dissipation	P_{tot}	T_A=25 °C	0.30	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
ESD class		JESD22-C101 (HBM)	0 (max 250V)	
Soldering temperature			260 °C	
IEC climatic category; DIN IEC 68-1			55/150/56	

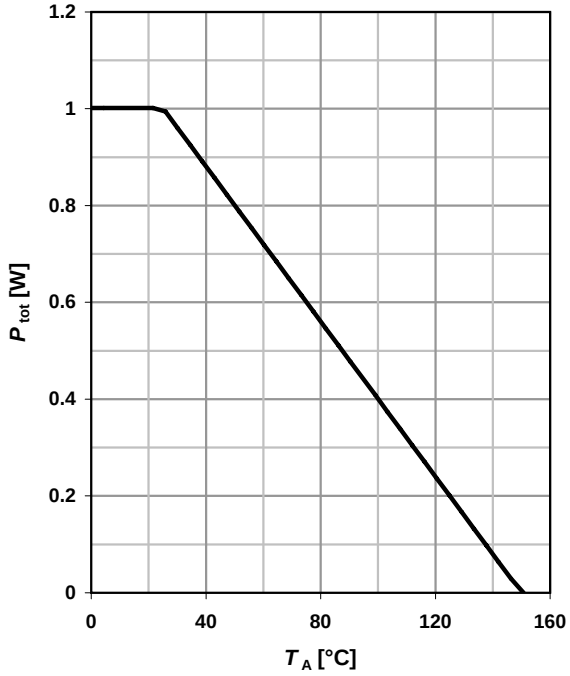
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - soldering point	R_{thJS}		-	-	120	K/W
SMD version, device on PCB:	R_{thJA}	minimal footprint	-	-	420	
		6 cm^2 cooling area[1)]	-	-	350	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=-250µA	-20	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=3.5 µA	-0.6	-0.9	-1.2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=-20 V, V_{GS}=0 V, T_j=25 °C	-	-0.1	-1	µA
		V_{DS}=-20 V, V_{GS}=0 V, T_j=150 °C	-	-10	-100	
Gate-source leakage current	I_{GSS}	V_{GS}=12 V, V_{DS}=0 V	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=2.5 V, I_D=0.46 A	-	581	900	
		V_{GS}=4.5 V, I_D=0.63 A	-	379	550	
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=0.46 A	0.87	1.74	-	S

[1)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air; t≤10 sec.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=-15 V, f=1 MHz	-	87	115	pF
Output capacitance	C_{oss}		-	35	46.7	
Reverse transfer capacitance	C_{rss}		-	30	45	
Turn-on delay time	$t_{d(on)}$	V_{DD}=-10 V, V_{GS}=-4.5 V, I_D=0.58 A, R_G=6 Ω	-	2.6	4.0	ns
Rise time	t_r		-	7	11	
Turn-off delay time	$t_{d(off)}$		-	6	9	
Fall time	t_f		-	4.6	6.9	
Gate Charge Characteristics[3)]						
Gate to source charge	Q_{gs}	V_{DD}=10 V, I_D=0.58 A, V_{GS}=0 to 4.5 V	-	-0.18	-0.24	nC
Gate to drain charge	Q_{gd}		-	-0.46	-0.7	
Gate charge total	Q_g		-	-1.0	-1.3	
Gate plateau voltage	$V_{plateau}$		-	-2.0	-	V
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	-0.7	A
Diode direct current, pulsed	I_{SM}		-	-	-4.0	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=-0.58 A, T_j=25 °C	-	-0.92	-0.88	V
Reverse recovery time	t_{rr}	V_R=10 V, I_F=$\lvert I_S \rvert$, di_F/dt=100 A/µs	-	9	11.2	ns
Reverse recovery charge	Q_{rr}		-	1.27	1.59	nC

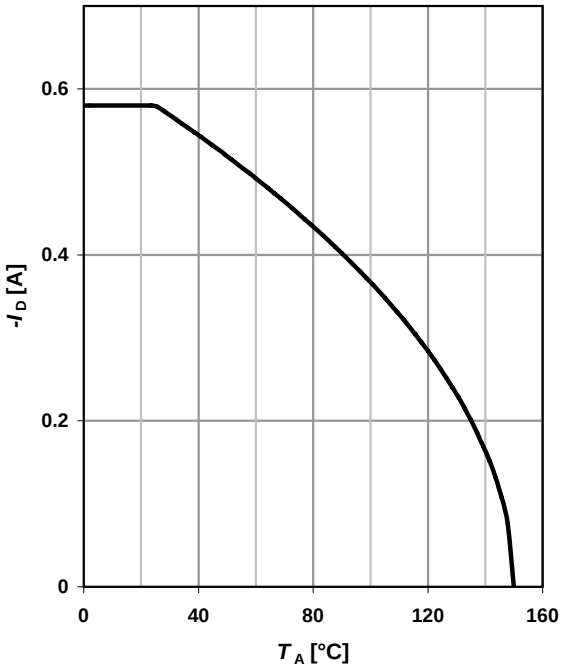
1 Power dissipation

$P_{tot}=f(T_A)$



2 Drain current

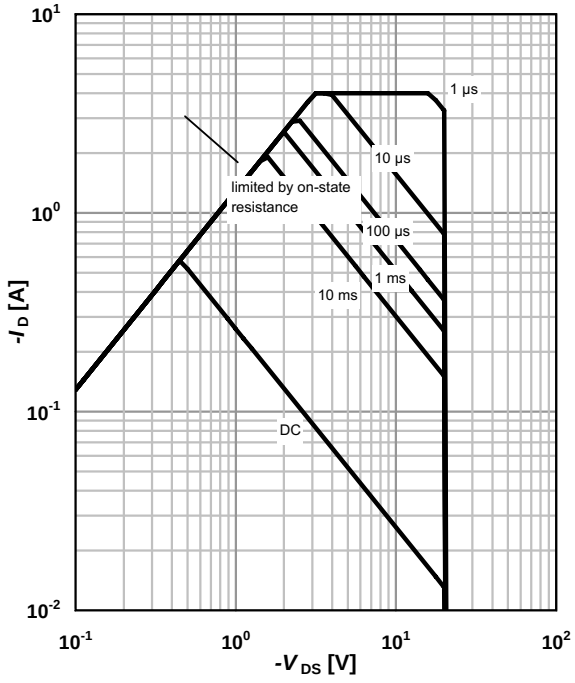
$I_D=f(T_A)$; $|V_{GS}|\geq 4.5$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_A=25$ °C[1)]; $D=0$

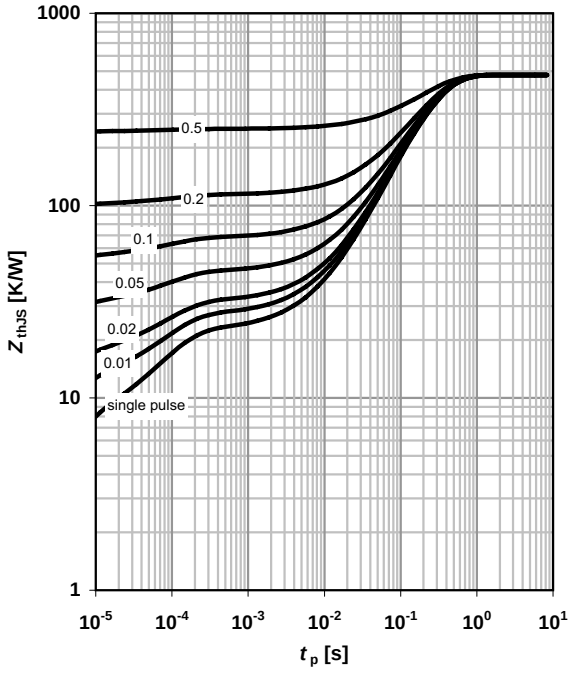
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJS}=f(t_p)$

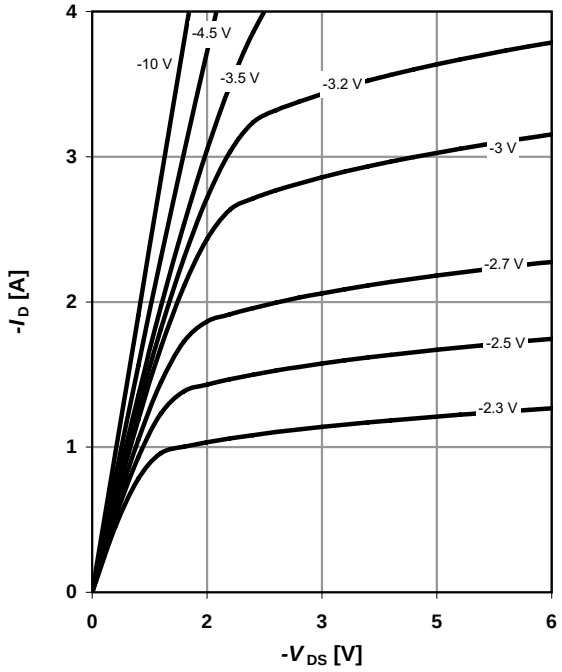
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

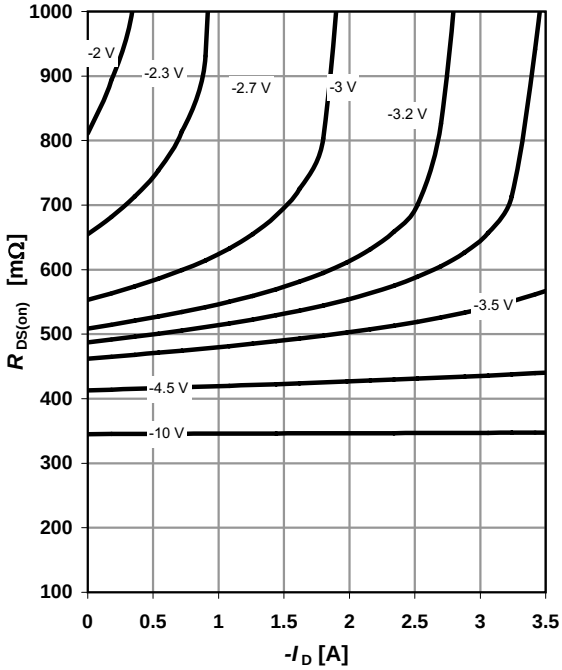
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

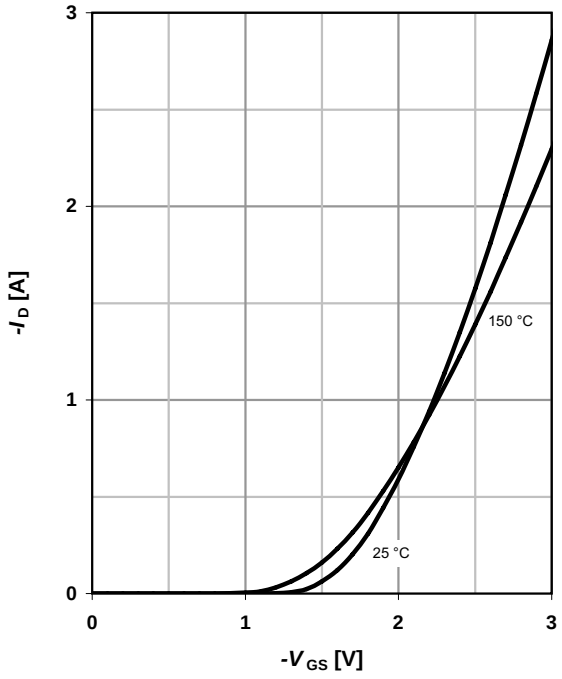
parameter: V_{GS}



7 Typ. transfer characteristics

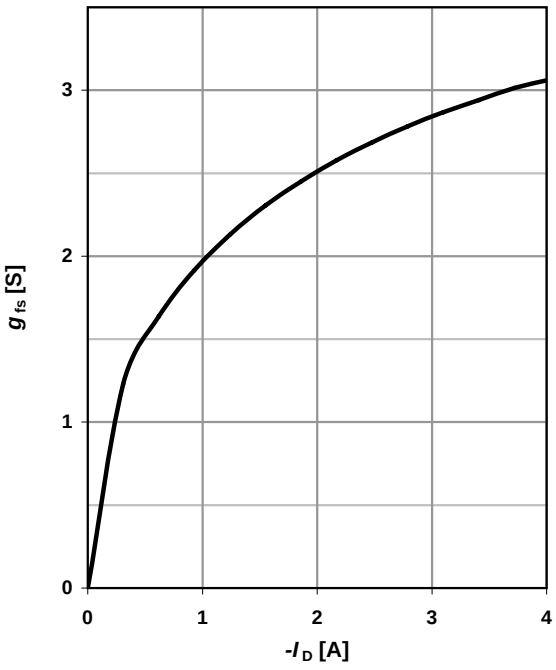
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



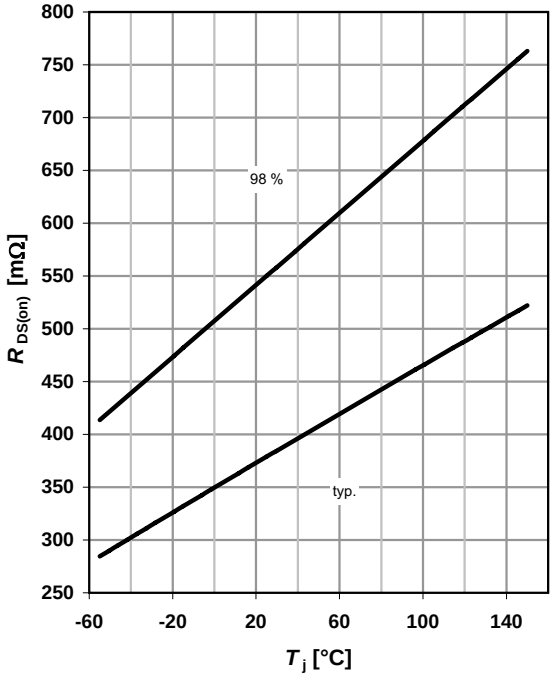
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



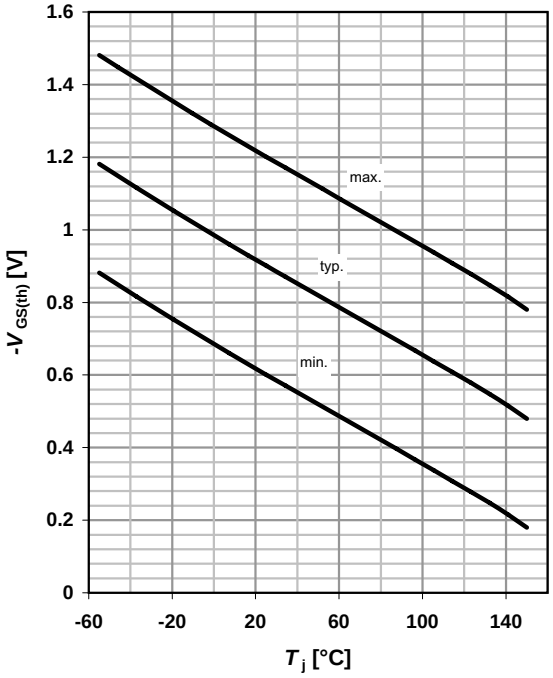
9 Drain-source on-state resistance

$R_{DS(on)}=f(T_j)$; I_D=-0.58 A; V_{GS}=-4.5 V



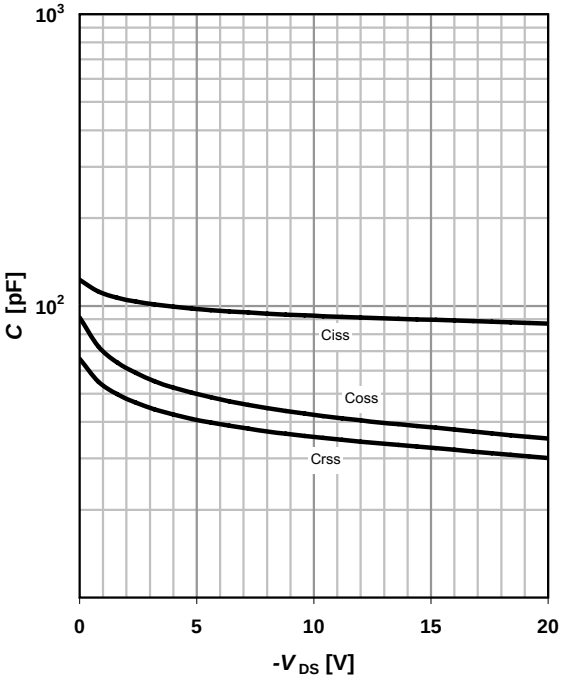
10 Typ. gate threshold voltage

$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; I_D=-3.5 µA



11 Typ. capacitances

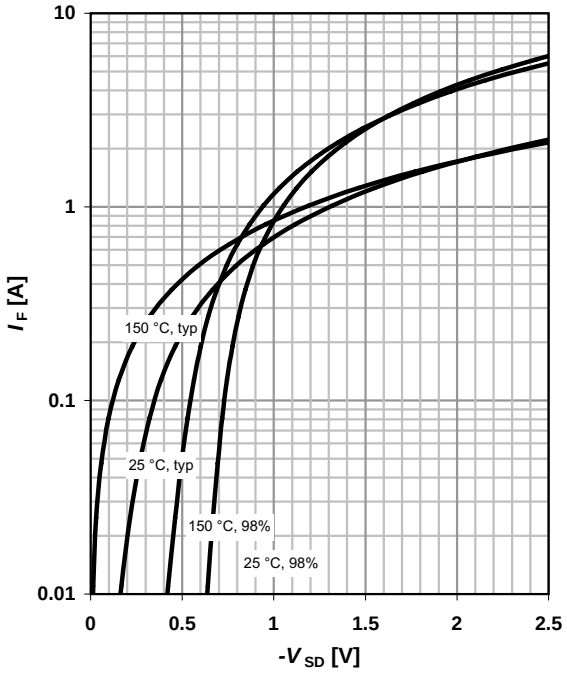
$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

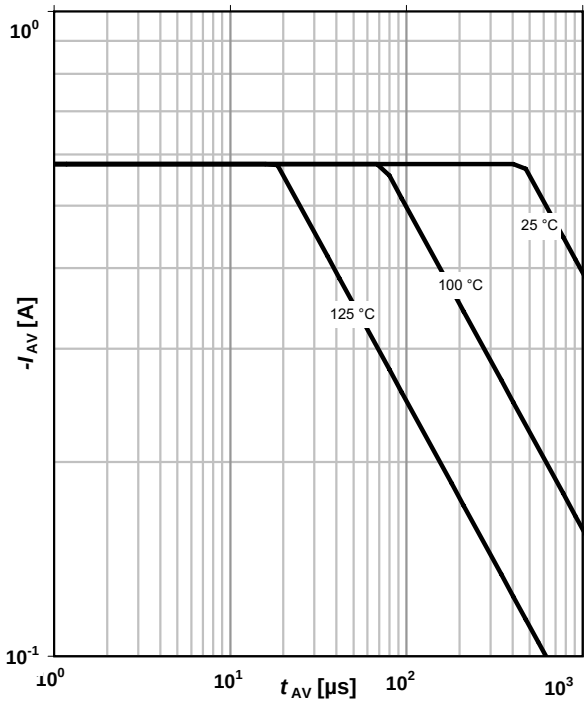
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

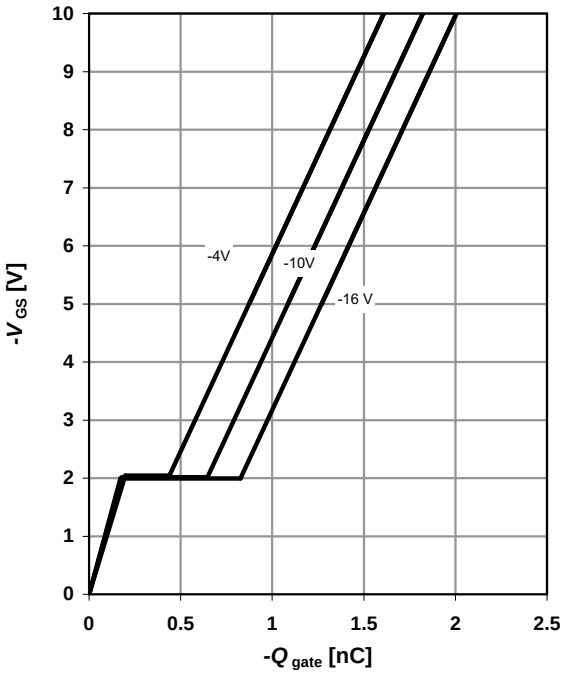
parameter: $T_{j(start)}$



14 Typ. gate charge

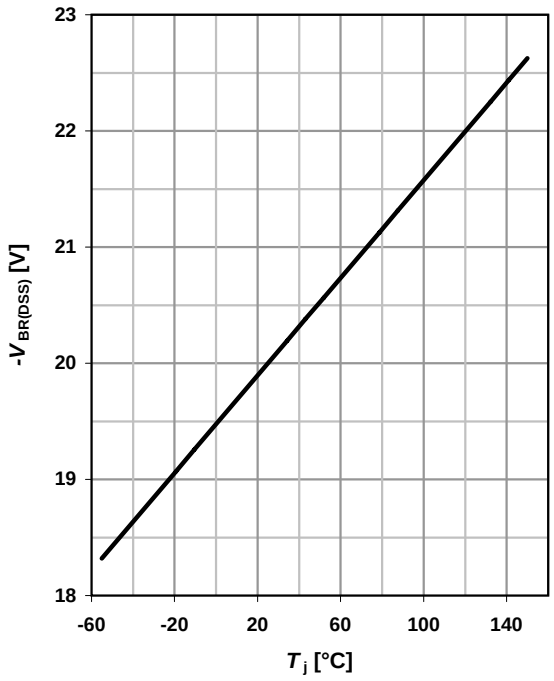
V_{GS}=f(Q_{gate}); I_D=-0.58 A pulsed

parameter: V_{DD}

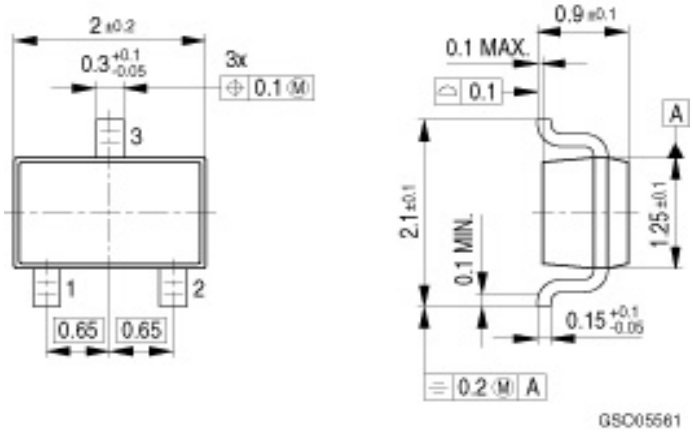


15 Drain-source breakdown voltage

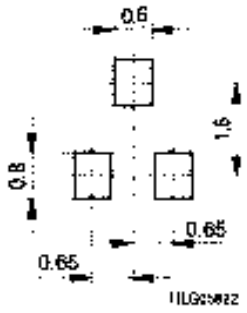
$V_{BR(DSS)}$=f(T_j); I_D=-250 µA



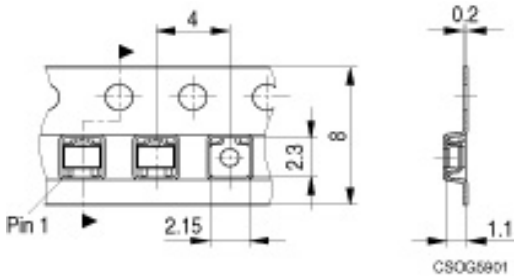
Package Outline:



Footprint:



Packaging:



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