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FDS6690A

Single N-Channel, Logic-Level, PowerTrench® MOSFET

General Description

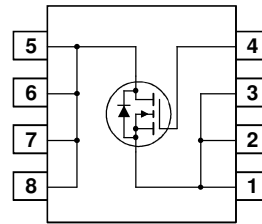
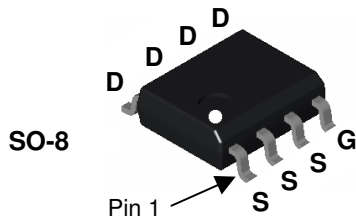
This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.



Features

- 11 A, 30 V. $R_{DS(ON)} = 12.5\text{ m}\Omega @ V_{GS} = 10\text{ V}$
 $R_{DS(ON)} = 17.0\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous (Note 1a)	11	A
	– Pulsed	50	
P_D	Power Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1.0	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	96	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Rated	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	125	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6690A	FDS6690A	13"	12mm	2500 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		25		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			10	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 11\text{ A}$		9.8	12.5	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		12.0	17.0	
		$V_{GS} = 10\text{ V}, I_D = 11\text{ A}, T_J = 125^\circ\text{C}$		13.7	22.0	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	50			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 11\text{ A}$		48		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		1205		pF
C_{oss}	Output Capacitance			290		pF
C_{rss}	Reverse Transfer Capacitance			115		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		2.4		Ω

Switching Characteristics (Note 2)

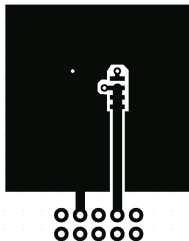
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		9	19	ns
t_r	Turn–On Rise Time			5	10	ns
$t_{d(off)}$	Turn–Off Delay Time			28	44	ns
t_f	Turn–Off Fall Time			9	19	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 11\text{ A}, V_{GS} = 5\text{ V}$		12	16	nC
Q_{gs}	Gate–Source Charge			3.4		nC
Q_{gd}	Gate–Drain Charge			4.0		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current			2.1		A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.74	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 11\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$		24		nS
Q_{rr}	Diode Reverse Recovery Charge			27		nC

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) $50^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



- b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2 Test: Pulse Width < $300\ \mu\text{s}$, Duty Cycle < 2.0%

3. Starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 8\text{ A}$, $V_{DD} = 30\text{ V}$, $V_{GS} = 10\text{ V}$

Typical Characteristics

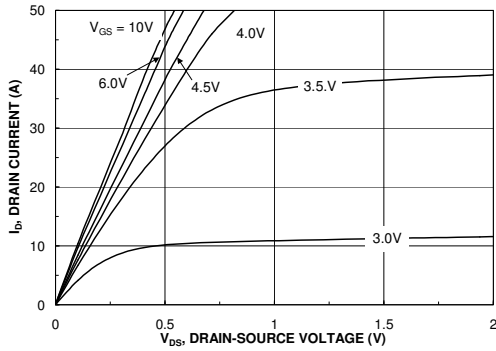


Figure 1. On-Region Characteristics.

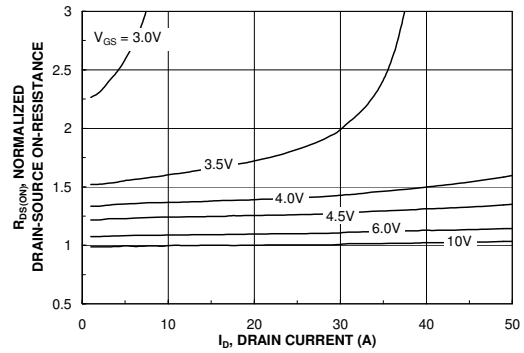


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

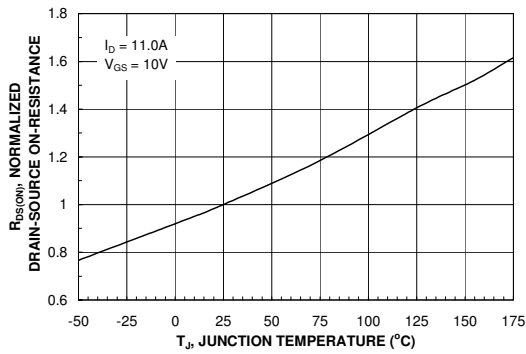


Figure 3. On-Resistance Variation with Temperature.

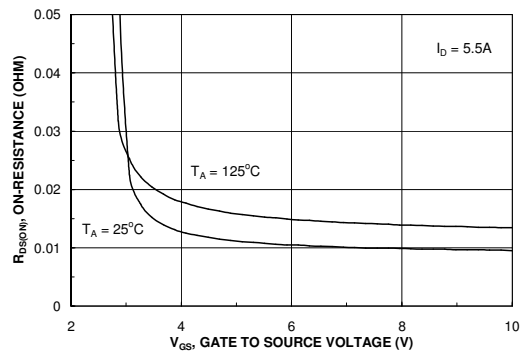


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

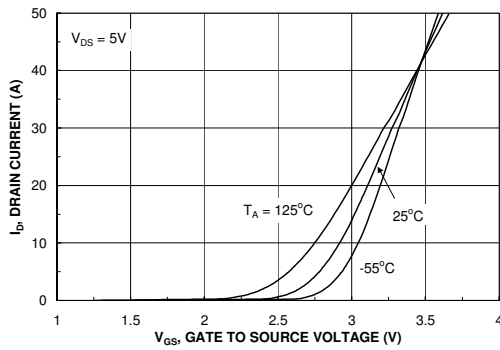


Figure 5. Transfer Characteristics.

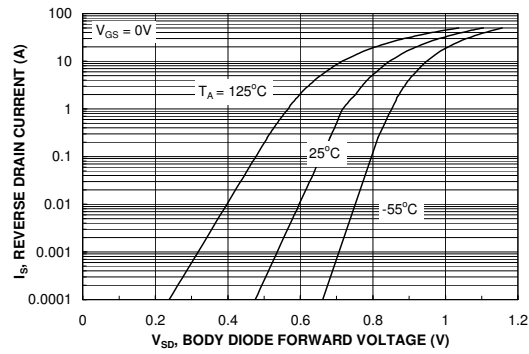


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

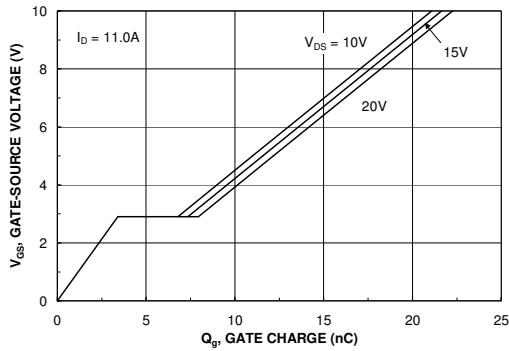


Figure 7. Gate Charge Characteristics.

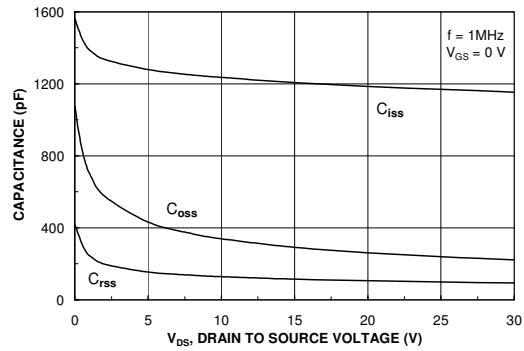


Figure 8. Capacitance Characteristics.

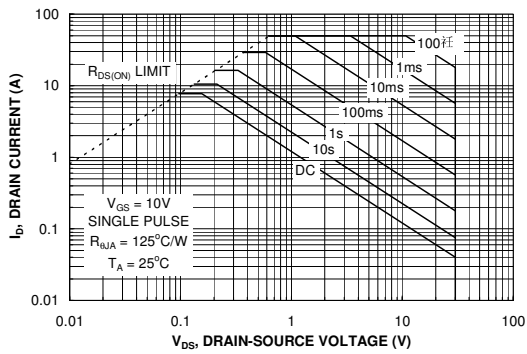


Figure 9. Maximum Safe Operating Area.

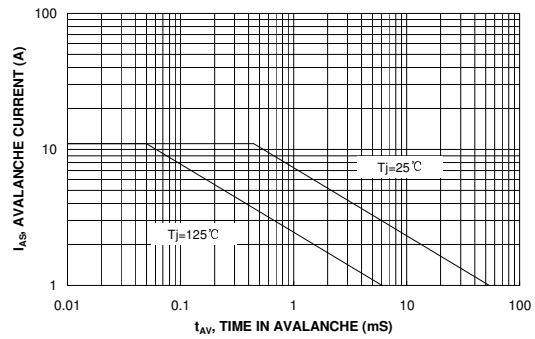


Figure 10. Unclamped Inductive Switching Capability Figure

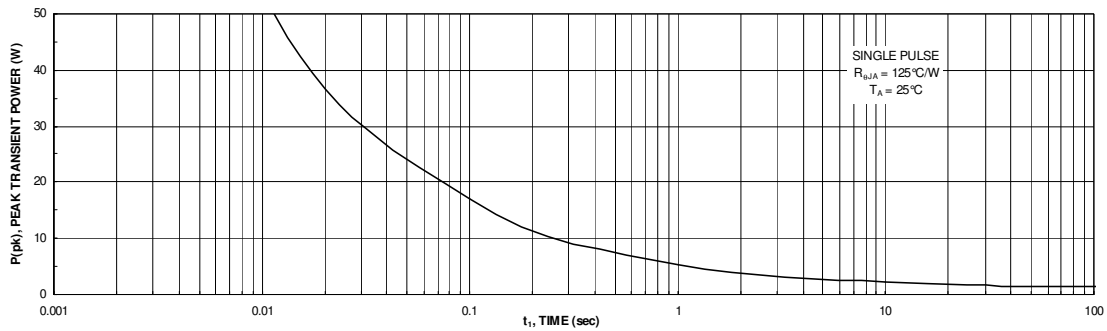


Figure 11. Single Pulse Maximum Power Dissipation.

Typical Characteristic

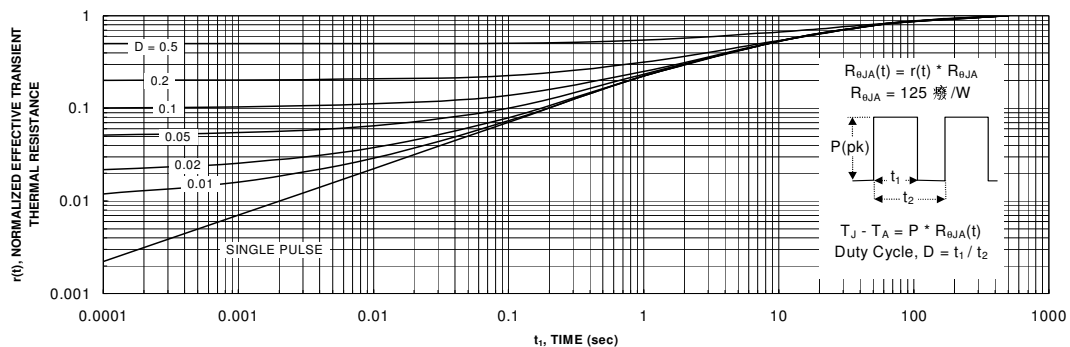


Figure 12. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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