4.5V to 18V Input, 3.0A Integrated MOSFET 1ch Synchronous Buck DC/DC Converter

BD9D321EFJ

General Description

BD9D321EFJ is a synchronous buck switching regulator with built-in low on-resistance power MOSFETs. It is capable of providing current of up to 3 A. The SLLM™ control provides excellent efficiency characteristics in light-load conditions which make the product appropriate for equipment and devices that demand minimal standby power consumption. External phase compensation circuit is not necessary for it is a constant on-time control DC/DC converter with high speed response. •

Features

- Synchronous Single DC/DC Converter
- Constant On-time Control
- SLLM™ (Simple Light Load Mode) Control
- Over Current Protection
- Short Circuit Protection
- Thermal Shutdown Protection
- Under Voltage Lockout Protection
- Adjustable Soft Start
- HTSOP-J8 Package (Backside Heat Dissipation)

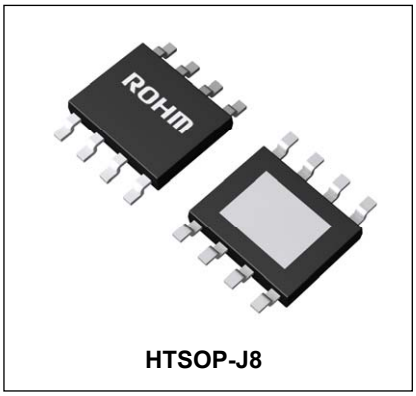
Applications

- Step-down Power Supply for DSPs, FPGAs, Microprocessors, etc.
- Set-top Box
- LCD TVs
- DVD / Blu-ray Player / Recorder
- Entertainment Devices

Key Specifications

- Input Voltage Range: 4.5V to 18.0 V
- Output Voltage Setting Range: 0.765V to 7V
  (V_{IN} × 0.07)V to (V_{IN} × 0.65)V
- Output Current: 3 A (Max)
- Switching Frequency: 700 kHz (Typ)
- High Side MOSFET On-Resistance: 100 m Ω (Typ)
- Low Side MOSFET On-Resistance: 70 m Ω (Typ)
- Standby Current: 2 μA (Typ)

Package W (Typ) x D (Typ) x H (Max)
HTSOP-J8 4.90mm x 6.00mm x 1.00mm



HTSOP-J8

Typical Application Circuit

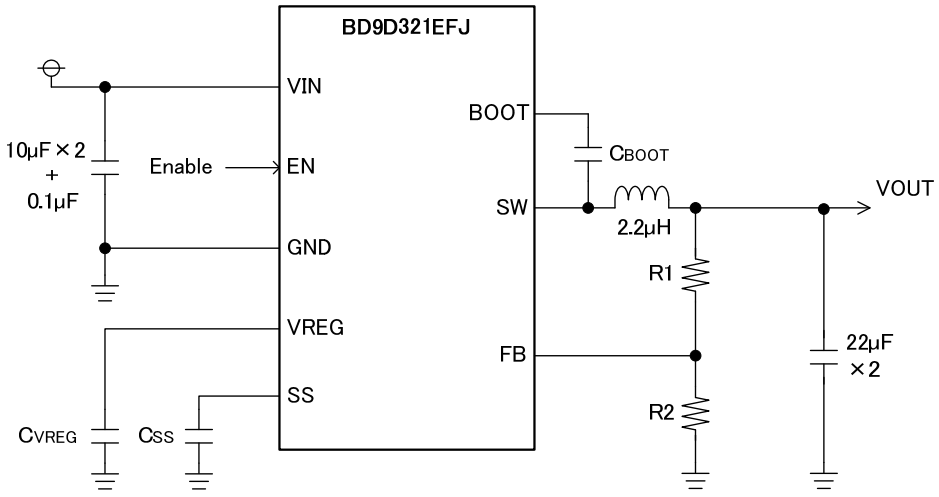


Figure 1. Typical Application Circuit

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Pin Configuration

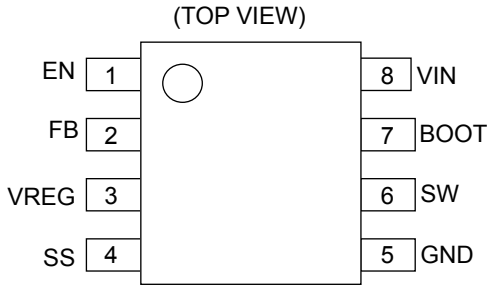

Figure 2. Pin Assignment

Pin Descriptions

Terminal No.	Symbol	Function
1	EN	Turning this terminal signal low level (0.3 V or lower) forces the device to enter the shutdown mode. Turning this terminal signal high level (2.2 V or higher) enables the device. This terminal must be terminated.
2	FB	An inverting input terminal of comparator which compares with reference voltage (V_{REF}). Refer to page.17 for how to calculate the resistance of the output voltage setting.
3	VREG	Power supply voltage terminal inside IC. Voltage of 5.25V (Typ) is outputted with more than 2.2V is impressed to EN terminal. Connect 1μF ceramic capacitor to ground.
4	SS	Terminal for setting the soft start time. The rise time of the output voltage can be specified by connecting a capacitor to this terminal. Refer to page.17 for how to calculate the capacitance.
5	GND	Ground terminal for the output stage of the switching regulator and the control circuit
6	SW	Switch node. This terminal is connected to the source of the high-side MOSFET and drain of the low-side MOSFET. Connect a bootstrap capacitor of 0.1μF between this terminal and BOOT terminal. In addition, connect an inductor considering the direct current superimposition characteristic.
7	BOOT	Connect a bootstrap capacitor of 0.1μF between this terminal and SW terminal. The voltage of this capacitor is the gate drive voltage of the high-side MOSFET.
8	VIN	Power supply terminal for the switching regulator. Connecting a 20μF(10μF × 2) and 0.1μF ceramic capacitor to ground is recommended.
-	FIN	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using multiple via provides excellent heat dissipation characteristics.

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Block Diagram

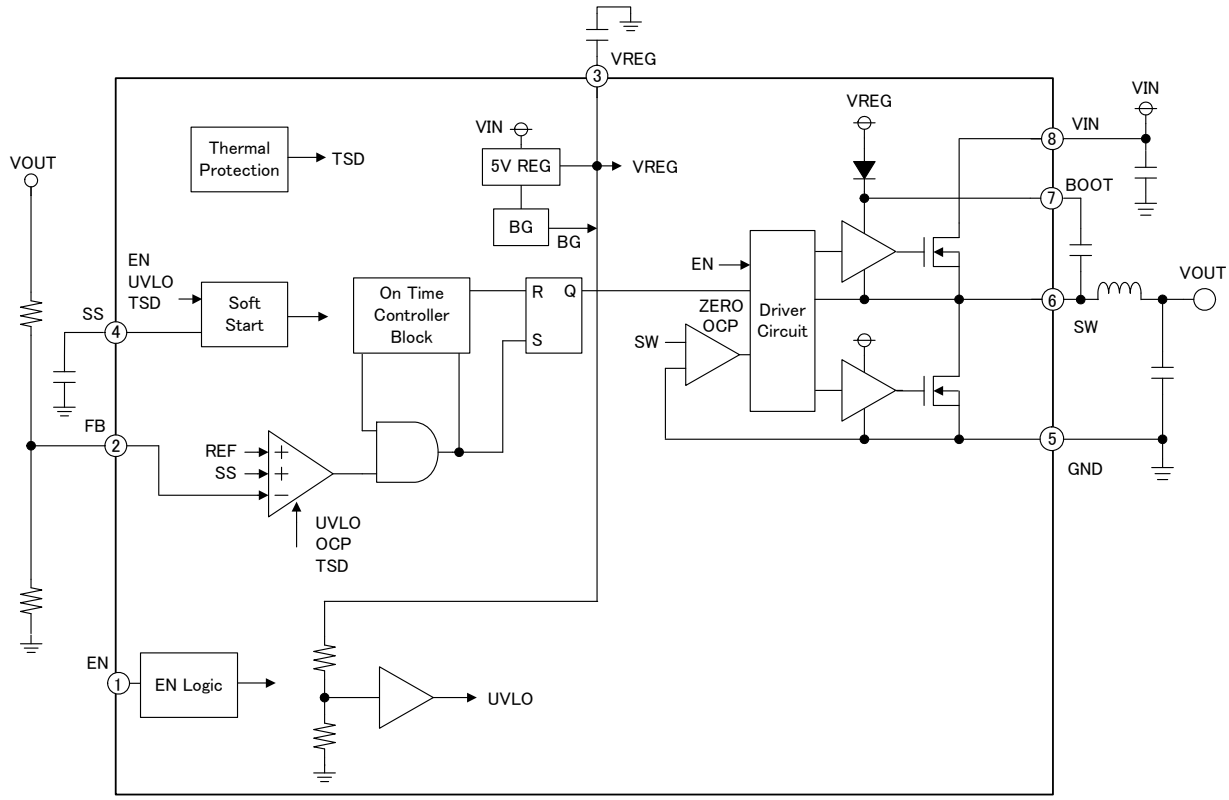

Figure 3. Block Diagram

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Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Input Voltage (Note 1)	V_{IN}	20	V
BOOT Voltage (Note 1)	V_{BOOT}	27	V
BOOT-SW Voltage (Note 1)	V_{BOOT}-V_{SW}	7	V
Output Feedback Voltage	V_{FB}	VREG	V
SW Voltage (Note 1)	V_{SW}	20	V
VREG Voltage (Note 1)	VREG	7	V
SS Voltage (Note 1)	V_{SS}	7	V
Logic Input Voltage (Note 1)	V_{EN}	20	V
Power dissipation (Note 2)	Pd	3.75	W
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	+150	°C

(Note 1) No need to exceed Pd.

(Note 2) Derating in done 30.08 mW/°C for operating above Ta ≥ 25°C (Mount on 4-layer 70.0mm × 70.0mm × 1.6mm board)

Caution1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution2: The operating temperature range is intended to guarantee functional operation and does not guarantee the life of the LSI within this range. The life of the LSI is subject to derating depending on usage environment such as the voltage applied, ambient temperature and humidity. Consider derating in the design of equipment and devices.

Recommended Operating Conditions

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Input voltage	V_{IN}	4.5	12	18	V
BOOT voltage	V_{BOOT}	4.5	-	24	V
SW Voltage	V_{SW}	-0.7	-	+18	V
BOOT-SW voltage	V_{BOOT}-V_{SW}	4.5	-	5.5	V
Logic Input Voltage	V_{EN}	0	-	18	V
Output Current	I_{OUT}	-	-	3	A
Output Voltage Range	V_{RANGE}	0.765 (Note 3)	-	7 (Note 4)	V

(Note 3) Please use under the condition of VOUT ≥ VIN × 0.07 [V].

(Note 4) Please use under the condition of VOUT ≤ VIN × 0.65 [V].

(Refer to the page 17 for how to calculate the output voltage setting.)

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Electrical Characteristics
(Ta = 25°C, V_{IN} = 12V, V_{EN} = 3V unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
<VIN Pin Block >						
Standby Circuit Current	I_{STB}	-	2	15	μA	V_{EN}=GND
Operating Circuit Current	I_{VIN}	-	0.7	2	mA	V_{EN}=3V, I_{OUT}=0mA when no switching
<Enable Block >						
EN Low Voltage	V_{ENL}	-	-	0.3	V	
EN High Voltage	V_{ENH}	2.2	-	VIN	V	
EN Bias Current	I_{EN}	-	1.5	5	μA	V_{EN}=3V
<5V Linear Regulator Block >						
VREG Standby Voltage	V_{VREG_STB}	-	-	0.1	V	V_{EN}=GND
VREG Output Voltage	V_{VREG}	5	5.25	5.5	V	
Maximum Current	I_{REG}	-	10	-	mA	
< Under-Voltage Lock-Out Block >						
UVLO Threshold Voltage	V_{VREG_UVLO}	3.4	3.8	4.2	V	VREG: Sweep up
UVLO Hysteresis Voltage	dV_{VREG_UVLO}	200	300	400	mV	VREG: Sweep down
< Reference Voltage Block >						
FB Threshold Voltage1	V_{REF1}	0.753	0.765	0.777	V	V_{IN}=12V, V_{OUT}=1.8V PWM Mode Operation
FB Threshold Voltage2	V_{REF2}	0.741	0.757	0.773	V	V_{IN}=12V, V_{OUT}=5.0V PWM Mode Operation
FB Input Current	I_{FB}	-	-	1	μA	
SS Charge Current	I_{SSC}	1.4	2.0	2.6	μA	
SS Discharge Current	I_{SSD}	0.1	0.2	-	mA	VREG=5.25V, V_{SS}=0.5V
< On Time Control Block >						
On Time	Ton	-	215	-	nsec	V_{IN}=12V, V_{OUT}=1.8V
Minimum Off Time	Toffmin	100	200	-	nsec	
<SW Block >						
High Side FET ON Resistance	R_{ONH}	-	100	200	mΩ	
Low Side FET ON Resistance	R_{ONL}	-	70	140	mΩ	
< Over Current Protection Block >						
Over Current Protection Current Limit	Iocp	-	5	-	A	(Note 5)

(Note 5) No tested on outgoing inspection.

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Typical Performance Curves

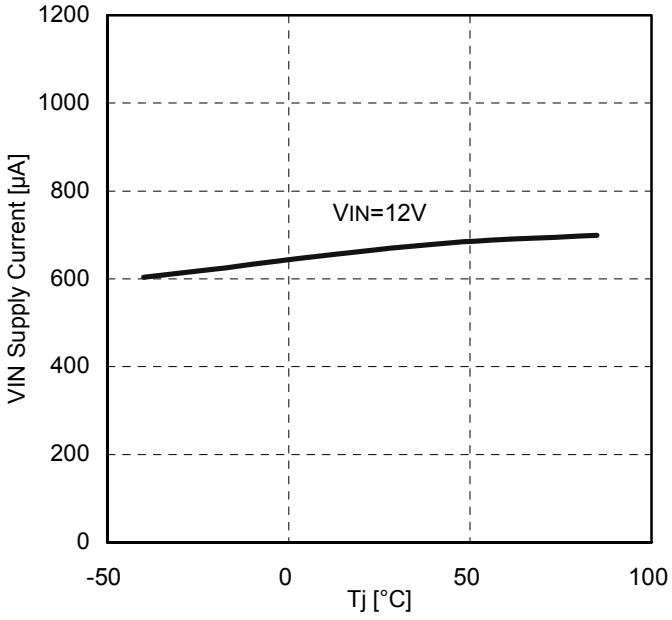

Figure 4. VIN Current vs Junction Temperature

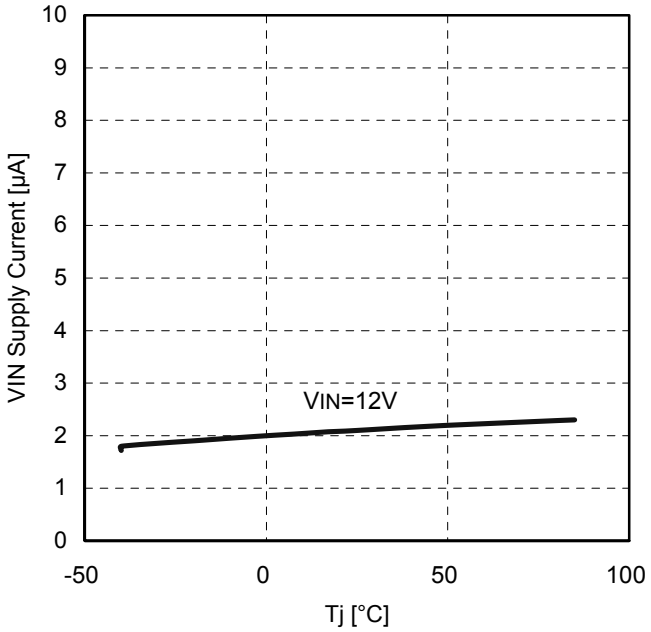

Figure 5. VIN Shutdown Current vs Junction Temperature

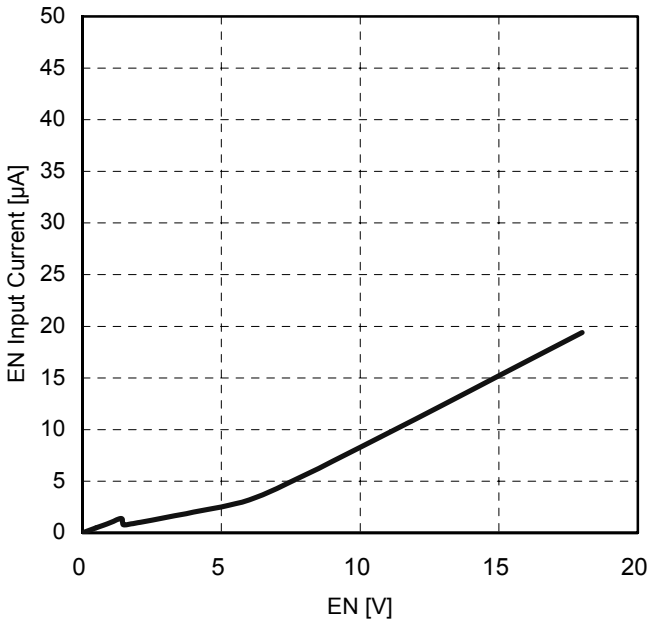

Figure 6. EN Current vs EN Voltage

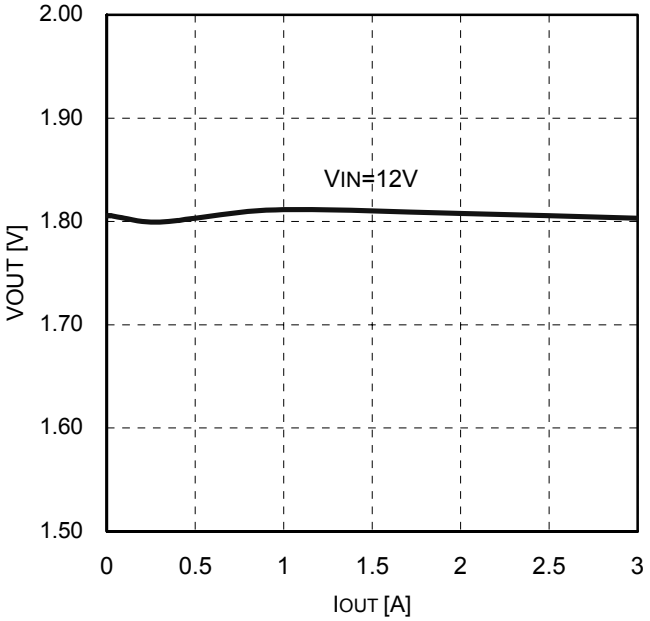

Figure 7. Output Voltage vs Output Current

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Typical Performance Curves (Continued)

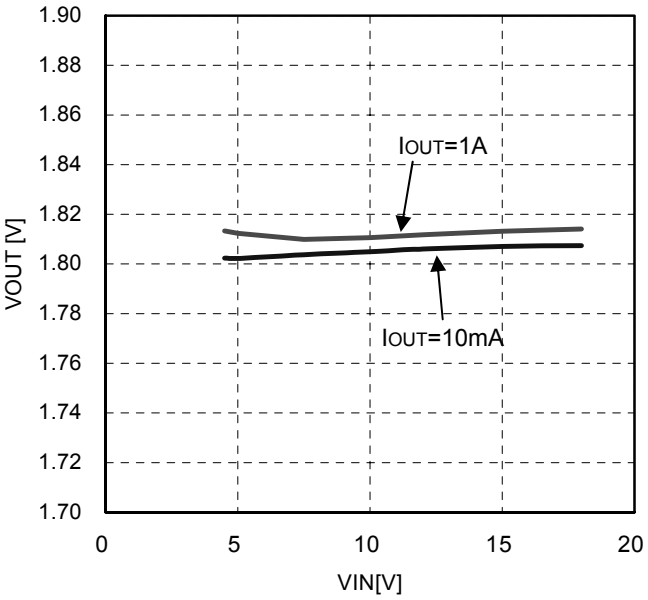

Figure 8. Output Voltage vs Input Voltage

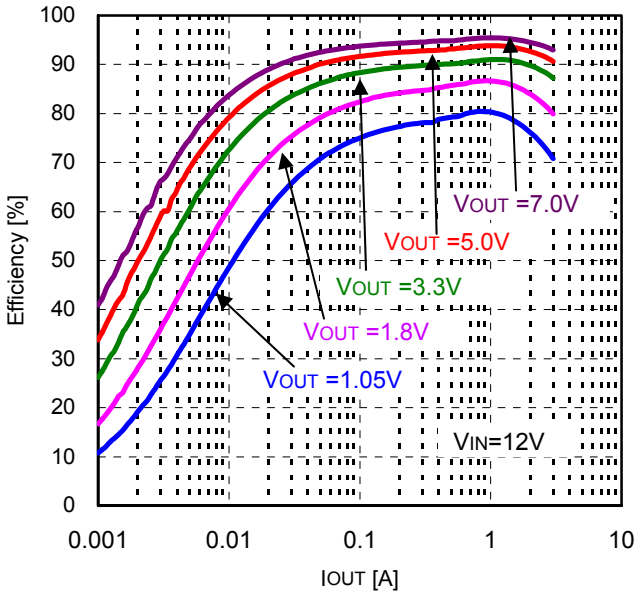

Figure 9. Efficiency vs Output Current

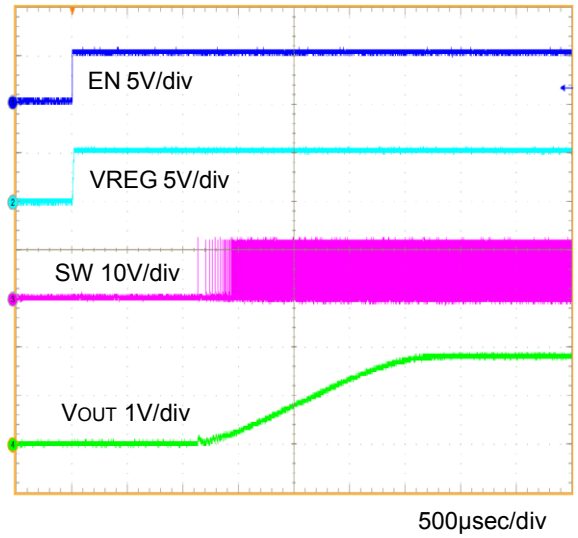

Figure 10. Start-up Waveform（EN=0V→5V）
(VIN=12V, VOUT=1.8V, IOUT=3A, Css=3300pF)

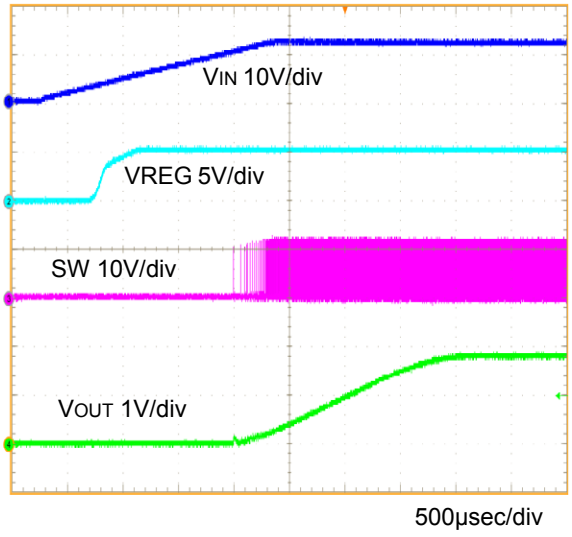

Figure 11. Start-up Waveform（VIN=EN）
(VIN=12V, VOUT=1.8V, IOUT=3A, Css=3300pF)

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Typical Performance Curves (Continued)

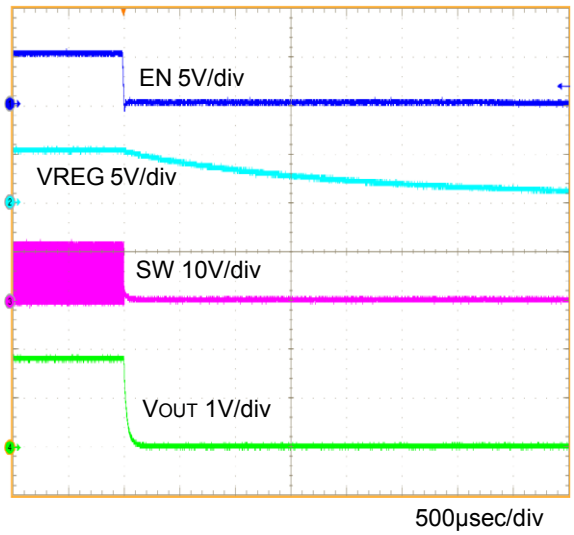

Figure 12. Shutdown Waveform（EN=5V→0V）
(VIN=12V, VOUT=1.8V, IOUT=3A, Css=3300pF)

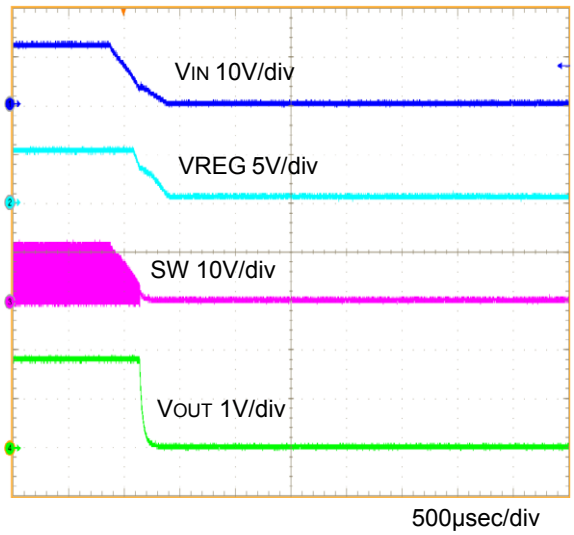

Figure 13. Shutdown Waveform（VIN=EN）
(VIN=12V, VOUT=1.8V, IOUT=3A, Css=3300pF)

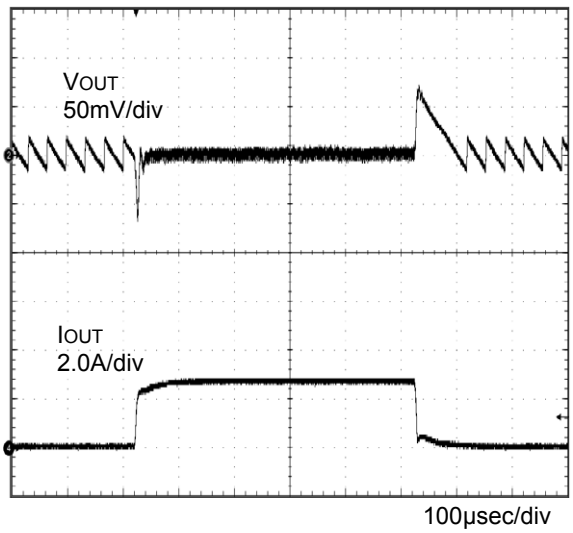

Figure 14. Load Transient Response
(VIN=12V, VOUT=1.8V, IOUT=50mA to 3A)

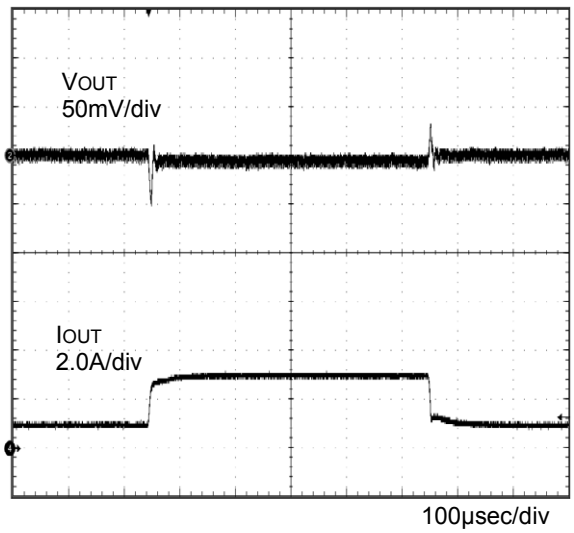

Figure 15. Load Transient Response
(VIN=12V, VOUT=1.8V, IOUT=1A to 3A)

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Typical Performance Curves (Continued)

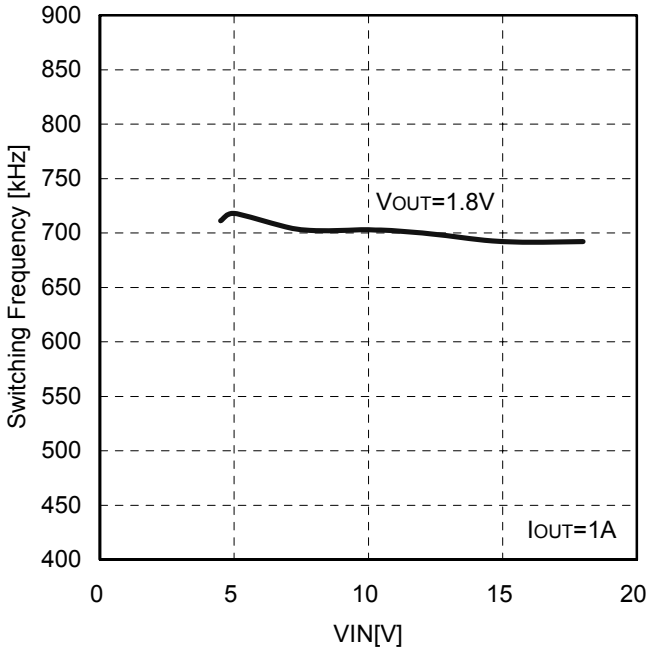

Figure 16. Switching Frequency vs Input Voltage

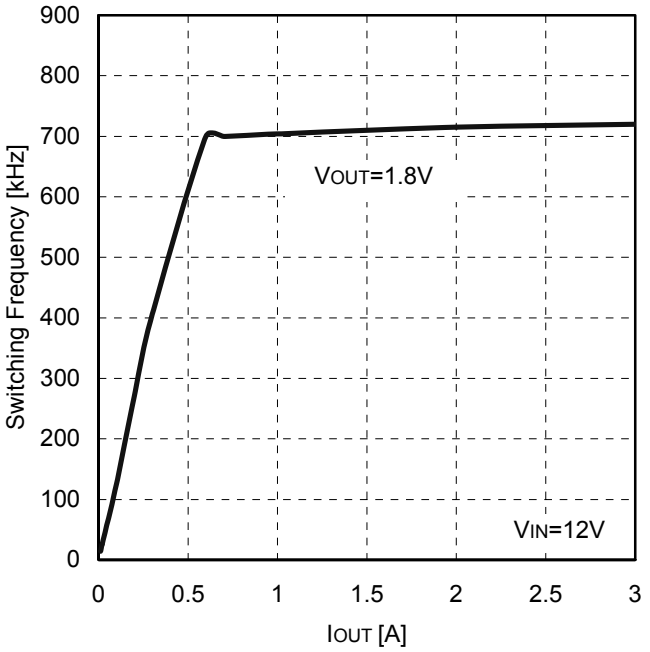

Figure 17. Switching Frequency vs Output Current

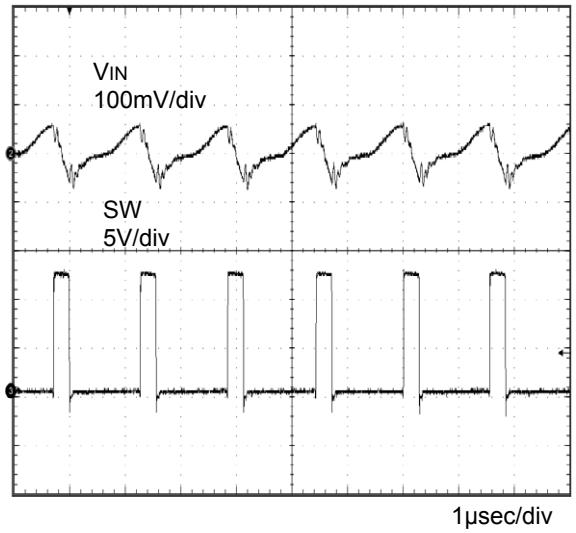

Figure 18. Voltage Ripple at Input
(VIN=12V, VOUT=1.8V, IOUT=3A, L=2.2µH, CIN=10µF x 2)

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Typical Performance Curves (Continued)

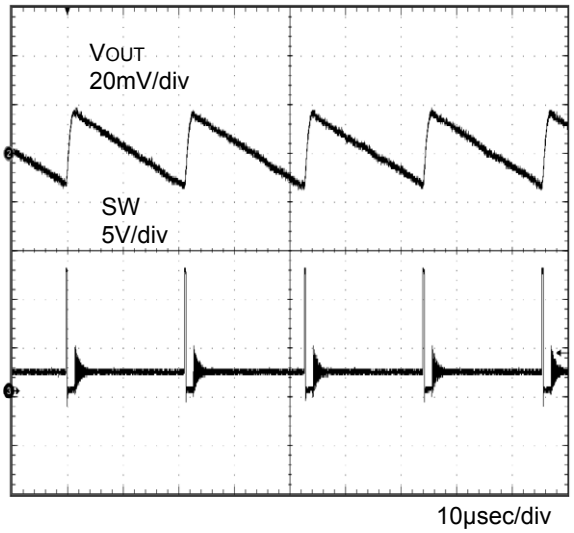

Figure 19. Voltage Ripple at Output
(VIN=12V, VOUT=1.8V, IOUT=30mA, L=2.2µH, COUT=22µF x 2)

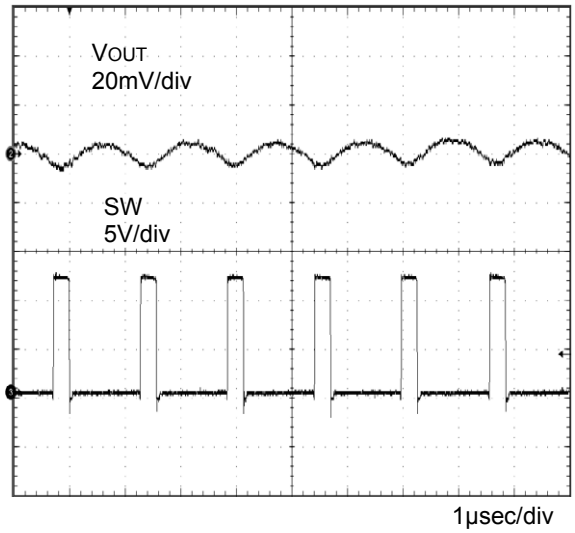

Figure 20. Voltage Ripple at Output
(VIN=12V, VOUT=1.8V, IOUT=3A, L=2.2µH, COUT=22µF x 2)

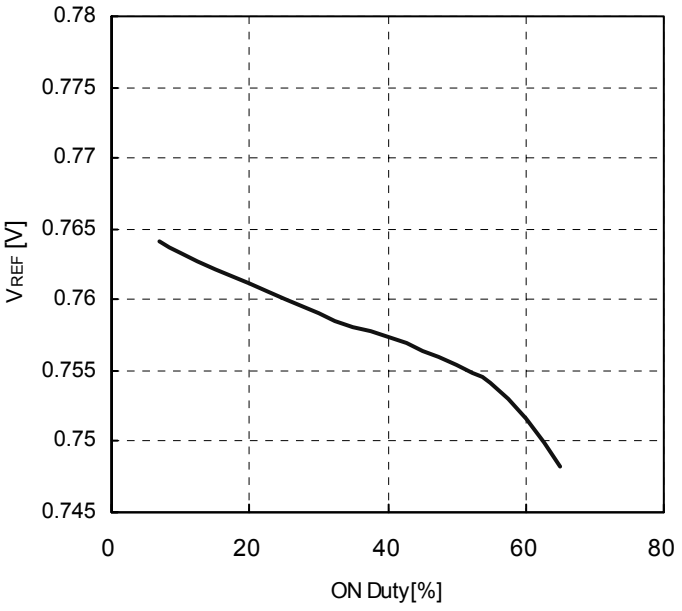

Figure 21. Reference Voltage vs ON Duty
(PWM operation)

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Function Explanations

1 Basic Operation

1-1 Constant On Time Control

BD9D321EFJ is a single synchronous buck switching regulator employing a constant on-time control system.
It controls the on-time by using the duty ratio of VOUT /VIN inside IC so that a switching frequency becomes 700 kHz.
Therefore it runs with the frequency of 700 kHz under the constant on-time decided with VOUT / VIN.

1-2 SLLM™ Control

BD9D321EFJ utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM (Simple Light Load Mode) control for lighter load to improve efficiency.

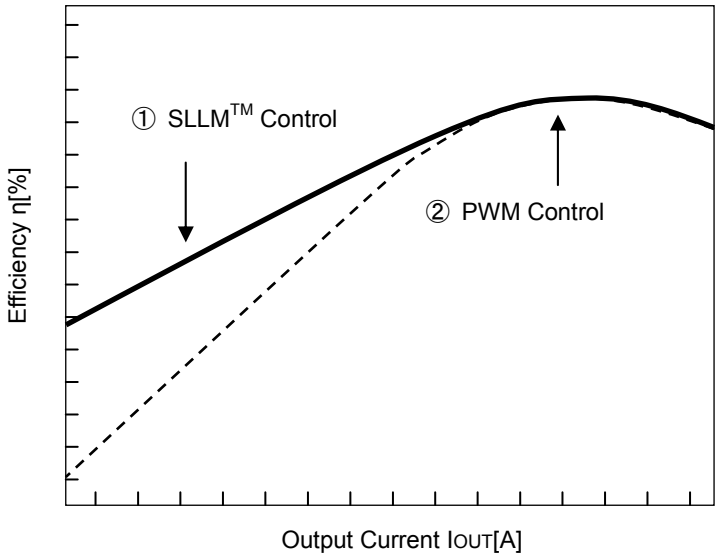

Figure 22. Efficiency (SLLM™ Control and PWM Control)

①SLLM™ Control

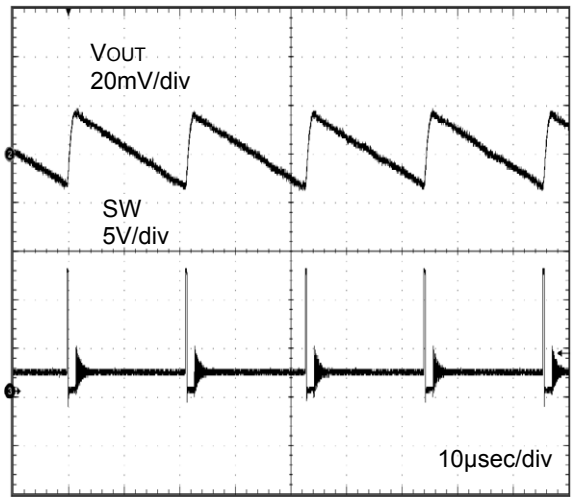

Figure 23. SW Waveform (①SLLM™ control)
(VIN = 12V, VOUT = 1.8V, IOUT = 30mA)

②PWM Control

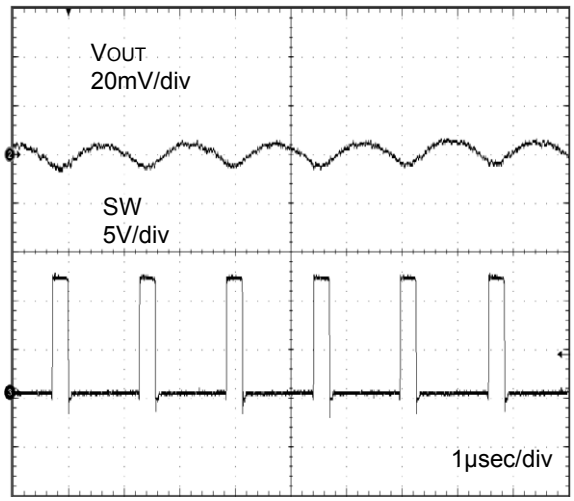

Figure 24. SW Waveform (②PWM control)
(VIN = 12V, VOUT = 1.8V, IOUT = 3A)

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1-3 Enable Control

The IC shutdown can be controlled by the voltage applied to the EN terminal. When V_{EN} reaches 2.2 V (Typ), the internal circuit is activated and the IC starts up.

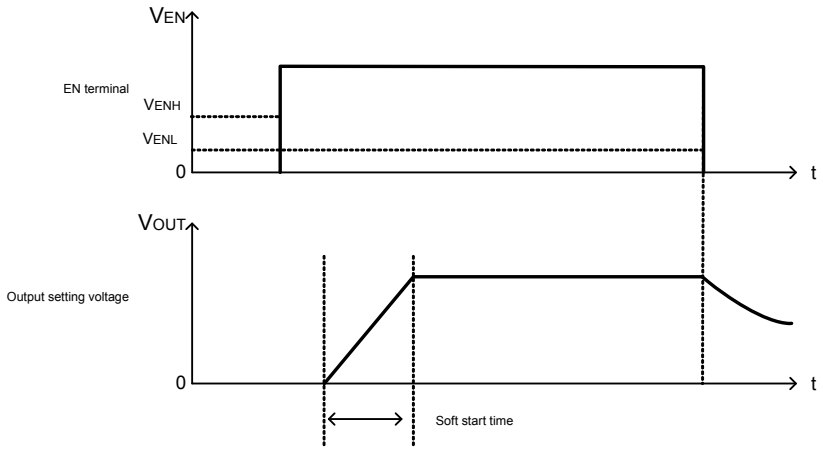

Figure 25. Start-up with EN pin

1-4 Soft Start Function

By turning EN terminal to High, the soft start function operates and it gradually starts output voltage by controlling the current at start-up. Also soft start function prevents sudden current and over shoot of output voltage. Rising time can be set by connecting capacitor to SS terminal. For setting the rising time, please refer to page.17.

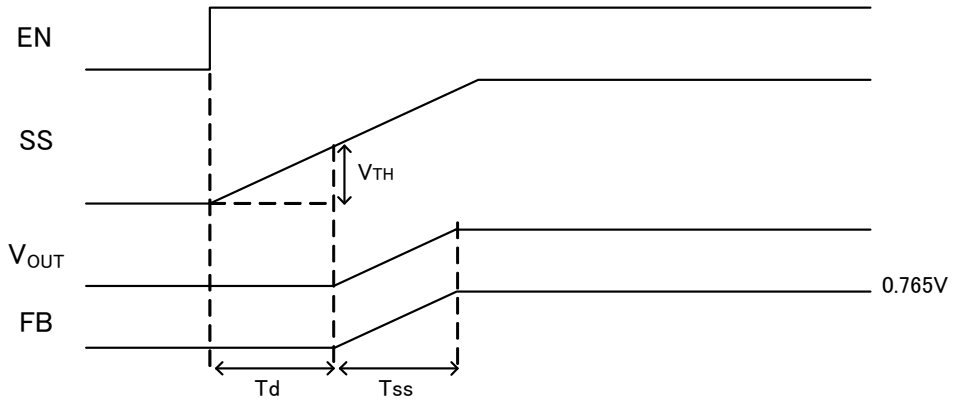

Figure 26. Soft Start Timing chart

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2 Protective Functions

The protective circuits are intended for prevention of damage caused by unexpected accidents. Do not use them for continuous protective operation.

2-1 Over Current Protection (OCP)

Over current protection function is effective by controlling current which flows in low side MOSFET by 1 cycle each of switching period. With inductor current exceeding the current restriction setting value I_{OCP} when LG is ON, the HG pulse cannot be hit even with FB voltage under REF voltage and LG continues to be ON until it is below I_{OCP}. It hits HG when it goes below I_{OCP}. As a result both frequency and duty fluctuates and output voltage may decrease.
In a case where output is decreased because of OCP, output may rise after OCP is released due to the action at high speed load response. This is non-latch protection and after over current situation is released the output voltage will recover.

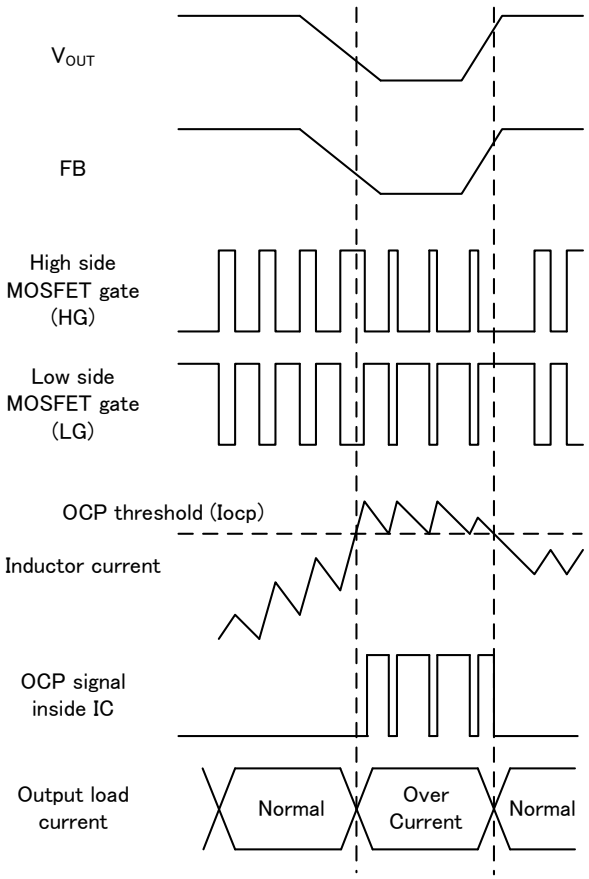

Figure 27. Over current protection timing chart

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2-2 Under Voltage Lockout Protection (UVLO)

The Under Voltage Lockout Protection circuit monitors the VREG terminal voltage.
The operation enters standby when the VREG terminal voltage is 3.5 V (Typ) or lower.
The operation starts when the VREG terminal voltage is 3.8 V (Typ) or higher.

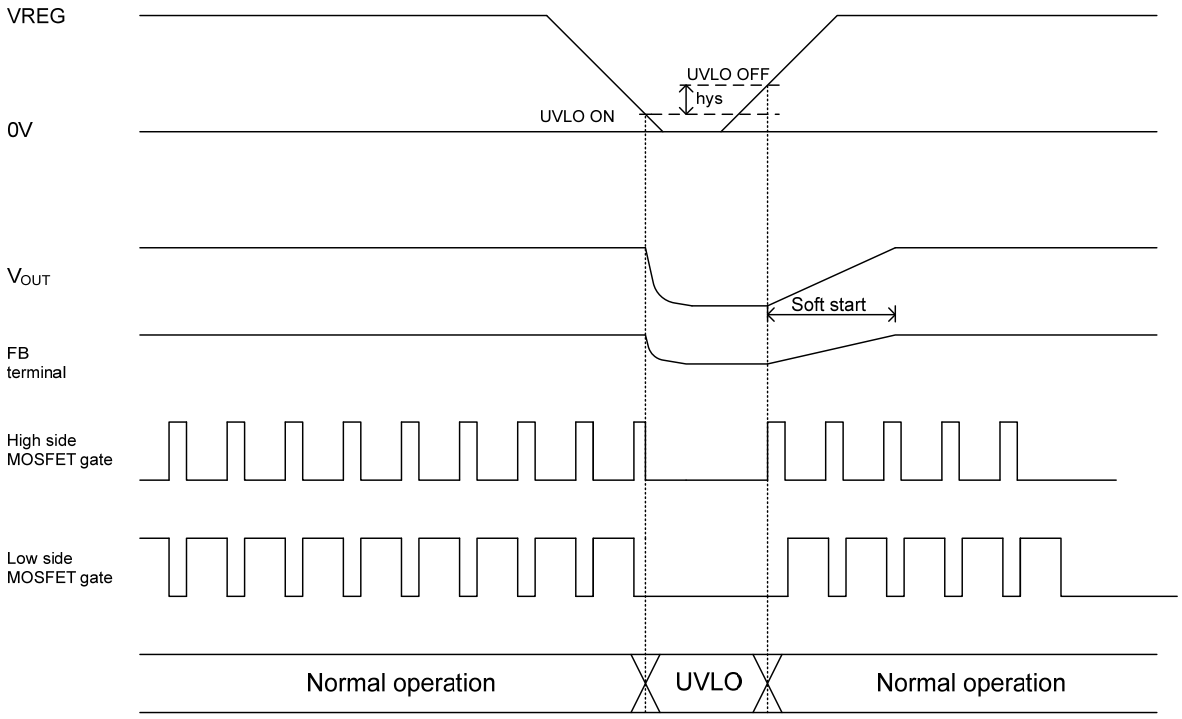

Figure 28. UVLO Timing Chart

※Load at Startup

Ensure that the respective output has light load at startup of this IC. Also, restrain the power supply line noise at startup and voltage drop generated by operating current within the hysteresis width of UVLO. Noise exceeding the hysteresis noise width may cause the IC to malfunction.

2-3 Thermal Shutdown Function

When the chip temperature exceeds Tj = 175°C, the DC/DC converter is stopped. The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding Tjmax = 150°C. Do not use this function for application protection design. This is non-latch protection.

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Application Example

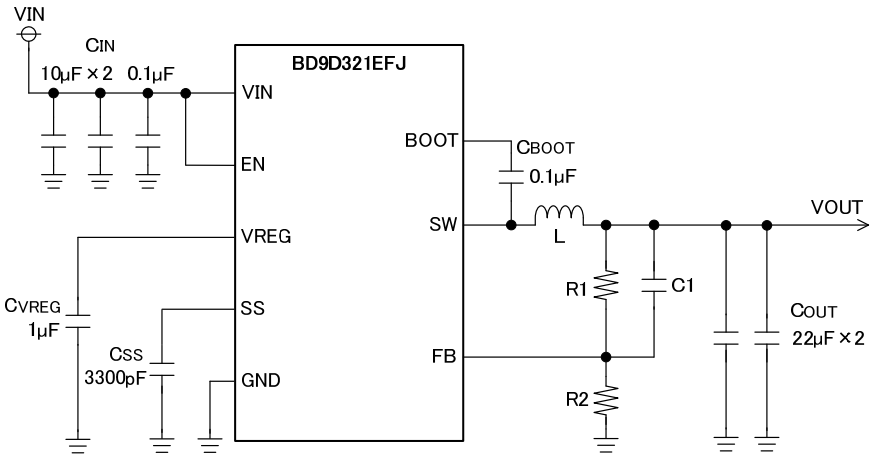

Figure 29. Application Circuit

Table 1. Recommended Component values

V_{IN} [V]	V_{OUT} [V]	R1 [kΩ]	R2 [kΩ]	C1 [pF]	L [μH] (Note 7)
12	1.0	6.8	22	- (Note 6)	1.5
12	1.05	8.2	22	- (Note 6)	1.5
12	1.2	12+0.51	22	- (Note 6)	1.5
12	1.8	30	22	- (Note 6)	2.2
12	3.3	68+5.6	22	- (Note 6)	2.2
12	5.0	120+3.3	22	- (Note 6)	3.3
12	7.0	180+3.3	22	- (Note 6)	3.3

(Note 6) C1 is a feed forward capacitor.
Additional phase boost can be achieved by adding the 5pF to 100pF capacitor (C1) in parallel with R1.

(Note 7) Recommended Inductor ・ALPS GLMC series
・TDK SPM6530 series

Selection of Components Externally Connected

(1) Output LC Filter Constant

The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. Selecting an inductor with a large inductance causes the ripple current ΔI_L that flows into the inductor to be small. However, decreasing the ripple voltage generated in the output is not advantageous in terms of the load transient response characteristic. An inductor with a small inductance improves the transient response characteristic but causes the inductor ripple current to be large which increases the ripple voltage in the output voltage, showing a trade-off relationship. The recommended inductor values are shown in Table 1.

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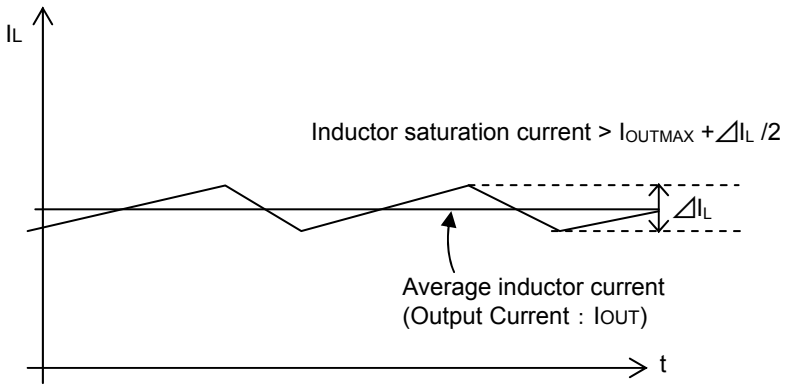

Figure 30. Waveform of current through inductor

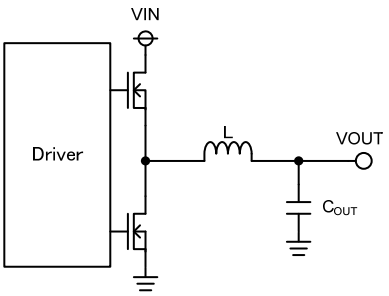

Figure 31. Output LC filter circuit

The inductor peak to peak ripple current ⊿IL is calculated using the following equation.

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times L} \text{ [A]}$$

For example, with VIN = 12 V, VOUT = 1.8 V, L = 2.2μH and the switching frequency F_{OSC} = 700 kHz, the calculated peak current ⊿IL is 1.0A.
Then, the inductor saturation current must be larger than the sum of the maximum output current (IOUTMAX) and 1/2 of the inductor ripple current (ΔIL / 2).

The output capacitor C_{OUT} affects the output ripple voltage characteristics. The output capacitor C_{OUT} must satisfy the required ripple voltage characteristics.

The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}}) \text{[V]}$$

R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor.

※The capacitor rating must allow a sufficient margin with respect to the output voltage.
The output ripple voltage can be decreased with a smaller ESR.
A ceramic capacitor of about 22 μF to 100 μF is recommended.

※Pay attention to total capacitance value, when additional capacitor CLOAD is connected in addition to output capacitor COUT. Then, please determine CLOAD and soft start time Tss (Refer to (3) Soft Start Setting) as satisfying the following equation.

$$C_{OUT} + C_{LOAD} \leq \frac{(I_{OCP} - I_{OUT}) \times T_{SS}}{V_{OUT}} \text{ [μF]}$$

IOCP is Over Current Protection Current limit value.

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(2) Output Voltage Setting

The output voltage value can be set by the feedback resistance ratio.

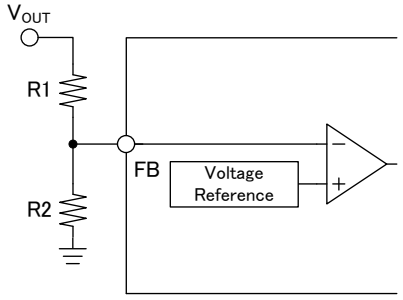

Figure 32. Feedback Resistor Circuit

$$V_{OUT} = \frac{R_1 + R_2}{R_2} \times V_{REF} \ [\mathrm{V}]$$

The VREF can be represented by the following equation defining VOUT_T as the target output voltage.

$$\text{In case } 0.07 \le \frac{V_{OUT\_T}}{V_{IN}} \le 0.5,\ V_{REF} = -0.02 \times \frac{V_{OUT\_T}}{V_{IN}} + 0.765 \ [\mathrm{V}]$$

$$\text{In case } 0.5 < \frac{V_{OUT\_T}}{V_{IN}} \le 0.65,\ V_{REF} = -0.22 \times \left(\frac{V_{OUT\_T}}{V_{IN}}\right)^2 + 0.2 \times \frac{V_{OUT\_T}}{V_{IN}} + 0.7105 \ [\mathrm{V}]$$

BD9D321EFJ can operate under the condition which satisfies the following equation.

$$0.07 \le \frac{V_{OUT}}{V_{IN}} \le 0.65$$

3) Soft Start Setting

Turning the EN terminal signal High activates the soft start function. This causes the output voltage to rise gradually while the current at startup is placed under control. This allows the prevention of output voltage overshoot and inrush current. The rise time depends on the value of the capacitor connected to the SS terminal.

$$T_d = (C_{SS} \times V_{TH}) / I_{SS}$$
$$T_{SS} = (C_{SS} \times V_{FB} \times 1.15) / I_{SS}$$

where

T_d is Soft Start Delay Time

T_{SS} is Soft Start Time

C_{SS} is Capacitor connected to Soft Start Time Terminal

V_{FB} is FB Terminal Voltage(0.765V Typ)

V_{TH} is Internal MOS threshold voltage(0.7V Typ)

I_{SS} is Soft Start Terminal Source Current(2.0μA Typ)

with C_{SS} = 3300pF,

$$T_d = (3300\,[\mathrm{pF}] \times 0.7\,[\mathrm{V}]) / 2.0\,[\mu\mathrm{A}]$$
$$= 1.16\,[\mathrm{msec}]$$
$$T_{SS} = (3300\,[\mathrm{pF}] \times 0.765\,[\mathrm{V}] \times 1.15) / 2.0\,[\mu\mathrm{A}]$$
$$= 1.45\,[\mathrm{msec}]$$

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PCB Layout Design

In the step-down DC/DC converter, a large pulse current flows into two loops. The first loop is the one into which the current flows when the high side FET is turned ON. The flow starts from the input capacitor C_{IN}, runs through the FET, inductor L and output capacitor C_{OUT} and back to ground of C_{IN} via ground of C_{OUT}. The second loop is the one into which the current flows when the low side FET is turned on. The flow starts from the low side FET, runs through the inductor L and output capacitor C_{OUT} and back to ground of the low side FET via ground of C_{OUT}. Route these two loops as thick and as short as possible to allow noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors directly to the ground plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

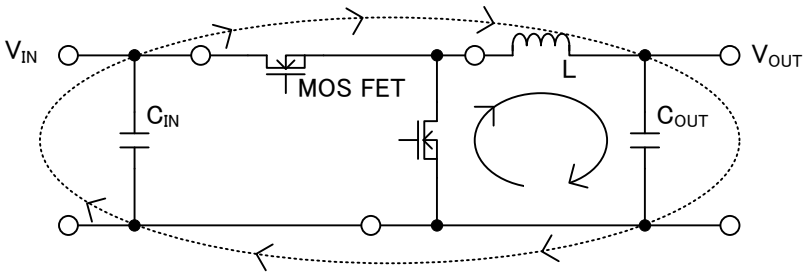

Figure 33. Current Loop of Buck Converter

Accordingly, design the PCB layout considering the following points.

- Connect an input capacitor as close as possible to the IC VIN terminal on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the ground node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the coil pattern as thick and as short as possible.
- Provide lines connected to FB and SS far from the SW nodes.
- Place the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.

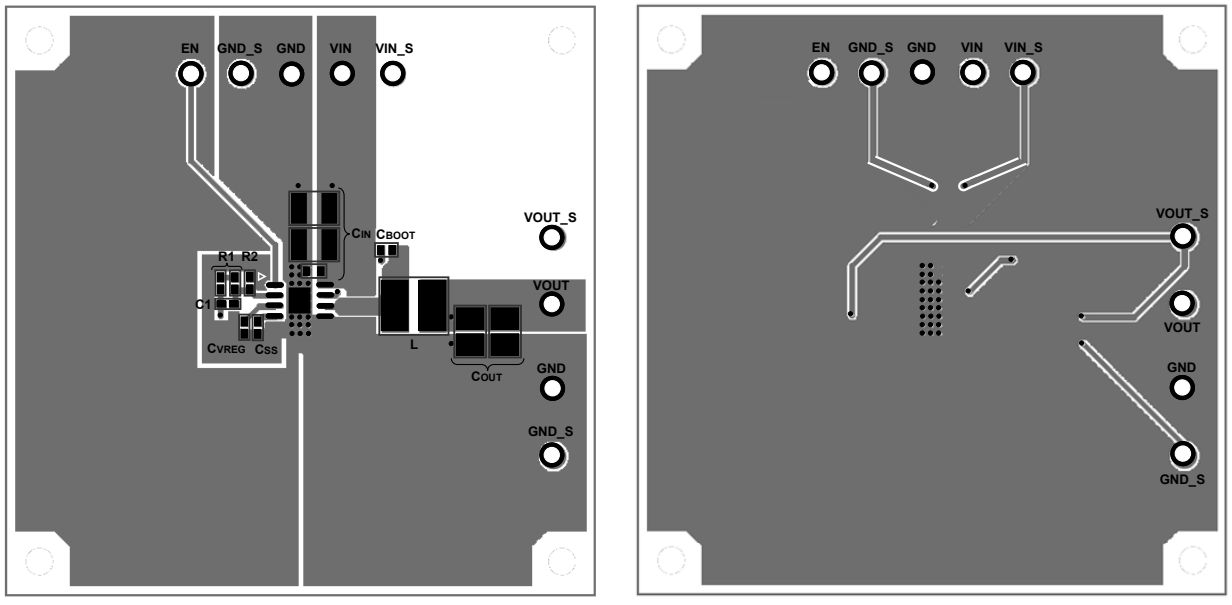

Figure 34. Example of PCB layout

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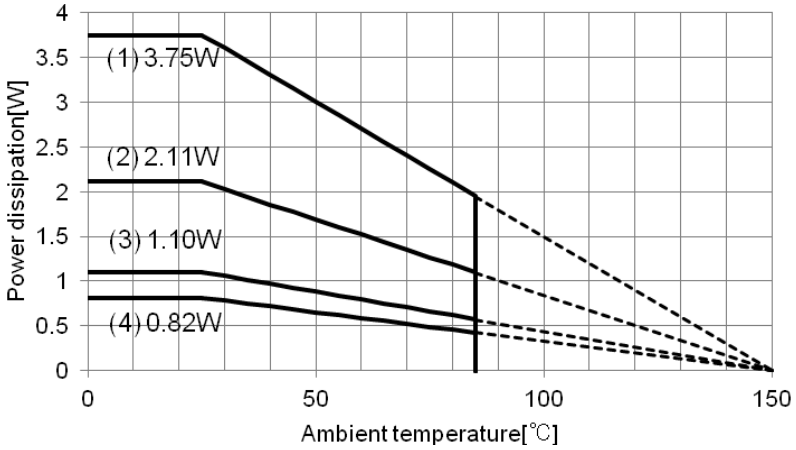
Power Dissipation

When designing the PCB layout and peripheral circuitry, sufficient consideration must be given to ensure that the power dissipation is within the allowable dissipation curve.



HTSOP-J8 Package
70 × 70 × 1.6 mm assembled glass epoxide board
(1) 4-layer board (Copper foil area 70 mm × 70 mm)
(2) 2-layer board (Copper foil area 70 mm × 70 mm)
(3) 2-layer board (Copper foil area 15 mm × 15 mm)
(4) 1-layer board (Copper foil area 0 mm× 0 mm)

Figure 35. Power dissipation (HTSOP-J8)

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I/O Equivalent Circuit

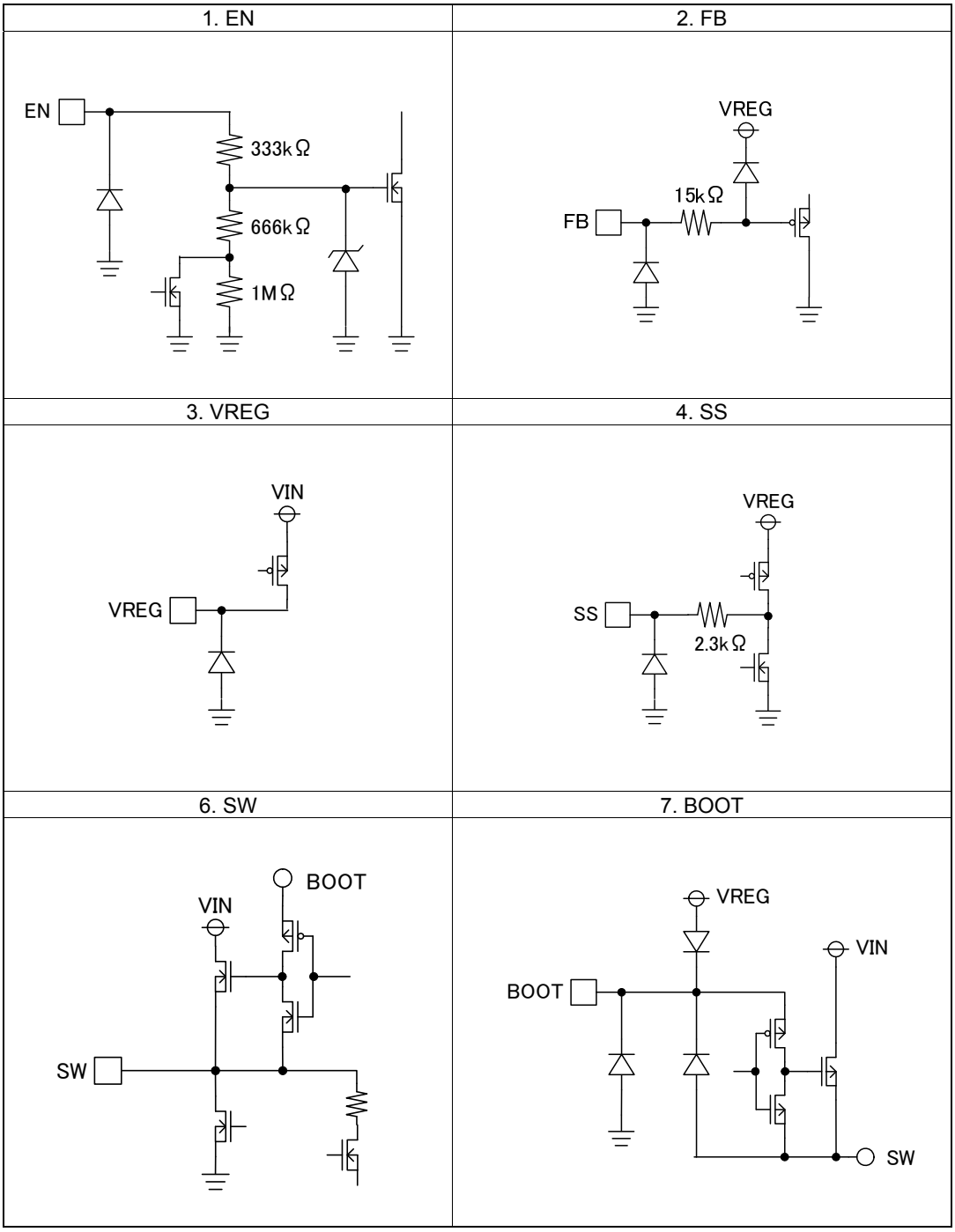

Figure 36. I/O equivalence circuit

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on 4 - layer 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

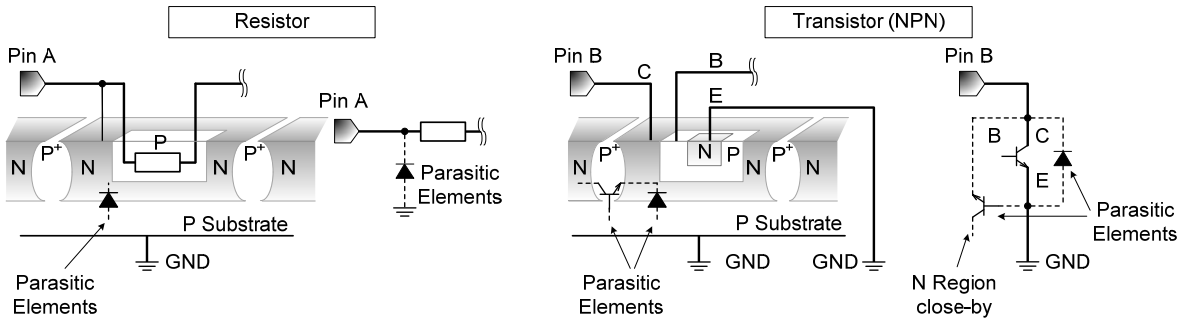

Figure 37. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information

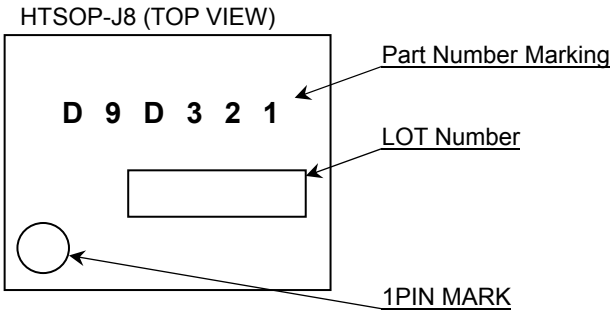
B D 9 D 3 2 1 E F J	-	E 2

Part Number

Package
EFJ: HTSOP-J8

Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



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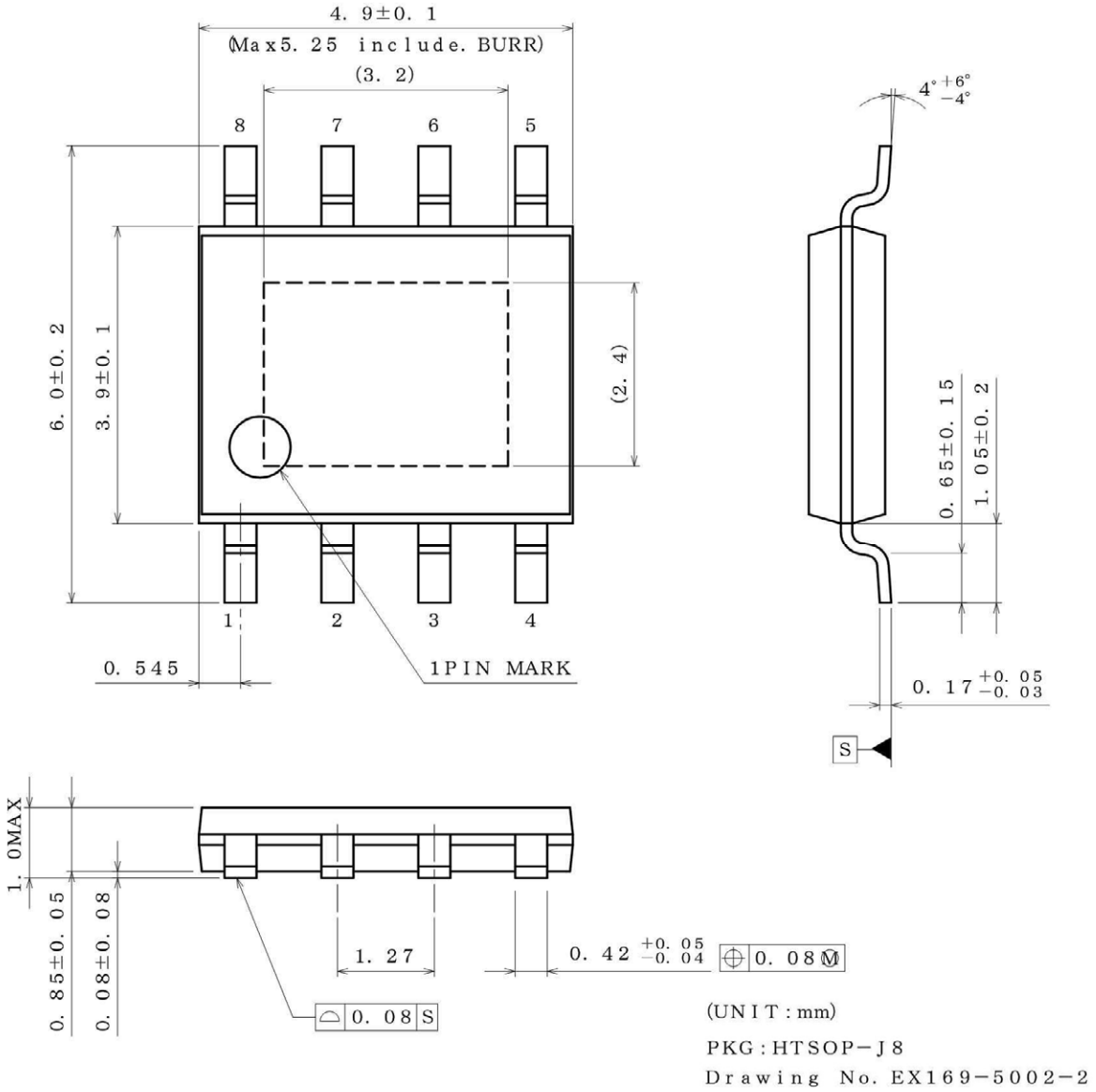
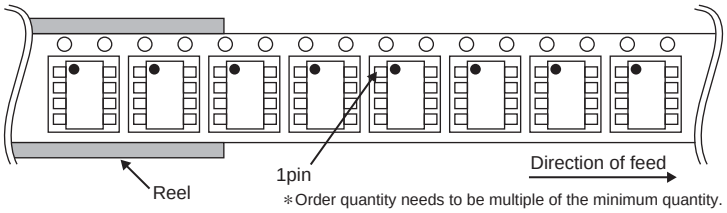
Physical Dimension, Tape and Reel Information

Package Name	HTSOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
07.Aug.2013	001	Created
29.Jan.2015	002	Revised the Electrical Characteristics and Table1. Added Figure 21.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

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8. Confirm that operation temperature is within the specified range described in the product specification.

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For details, please refer to ROHM Mounting specification

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   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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