TEXAS INSTRUMENTS

ISO1540, ISO1541

SLLSEB6C – JULY 2012 – REVISED JUNE 2015

ISO154x Low-Power Bidirectional I²C Isolators

1 Features

- Isolated Bidirectional, I²C Compatible, Communication
- Supports up to 1-MHz Operation
- 3-V to 5.5-V Supply Range
- Open-Drain Outputs With 3.5-mA Side 1 and 35-mA Side 2 Sink Current Capability
- –40°C to +125°C Operating Temperature
- ±50-kV/µs Transient Immunity (Typical)
- HBM ESD Protection of 4 kV on All Pins; 8 kV on Bus Pins
- Safety and Regulatory Approvals
  - 4242-V_{PK} Isolation per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
  - 2500-V_{RMS} Isolation for 1 Minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards
  - CQC Basic Insulation per GB4943.1-2011

2 Applications

- Isolated I²C Buses
- SMBus and PMBus Interfaces
- Open-Drain Networks
- Motor Control Systems
- Battery Management
- I²C Level Shifting

3 Description

The ISO1540 and ISO1541 devices are low-power, bidirectional isolators that are compatible with I²C interfaces. These devices have their logic input and output buffers separated by TI's Capacitive Isolation technology using a silicon dioxide (SiO_2) barrier. When used with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

This isolation technology provides for function, performance, size, and power consumption advantages when compared to optocouplers. The ISO1540 and ISO1541 devices enable a complete isolated I²C interface to be implemented within a small form factor.

The ISO1540 has two isolated bidirectional channels for clock and data lines while the ISO1541 has a bidirectional data and a unidirectional clock channel. The ISO1541 is useful in applications that have a single Master while the ISO1540 is ideally fit for multi-master applications.

Isolated bidirectional communications is accomplished within these devices by offsetting the Side 1 Low-Level Output Voltage to a value greater than the Side 1 High-Level Input Voltage, thus preventing an internal logic latch that otherwise would occur with standard digital isolators.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO1540 ISO1541	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

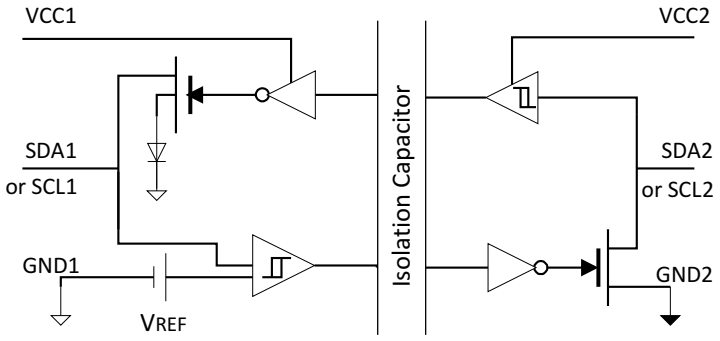


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2013) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- VDE Standard changed to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 ... 1

Changes from Revision A (October 2012) to Revision B — **Page**

- Change Safety Feature From: (VDE 0884 Part 2) (Pending) To: (VDE 0884 Part 2) (Approved) ... 1
- Changed, VDE column From: File number: 40016131 (pending) To: File number: 40016131 ... 16

Changes from Original (July 2012) to Revision A — **Page**

- Changed From: CSA Component Acceptance Notice 5A (Pending) To: CSA Component Acceptance Notice 5A (Approved) ... 1
- Changed From: IEC 60950-1 and IEC 61010-1 End Equipment Standards (Pending) To: IEC 60950-1 and IEC 61010-1 End Equipment Standards (Approved) ... 1
- Changed *Regulatory Information*, CSA column From: File number: 220991 (pending) To: File number: 220991 ... 16

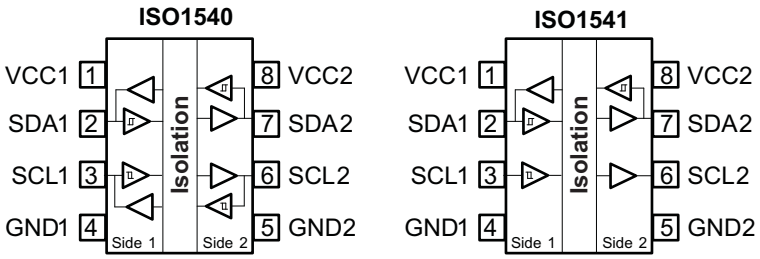
5 Device Comparison Table

PRODUCT	RATED ISOLATION	PACKAGE	CHANNEL DIRECTION
ISO1540	4242-V_{PK} and 2500-V_{RMS} (1)	D-8	Both SDA and SCL are bidirectional
ISO1541			SDA is bidirectional SCL is unidirectional

(1) See *Regulatory Information* for detailed Isolation specifications.

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O		DESCRIPTION	
NAME	NO.	ISO1540	ISO1541	ISO1540	ISO1541
GND1	4	—	—	Ground, Side 1	Ground, Side 1
GND2	5	—	—	Ground, Side 2	Ground, Side 2
SCL1	3	I/O	I	Serial Clock Input/Output, Side 1	Serial Clock Input, Side 1
SCL2	6	I/O	O	Serial Clock Input/Output, Side 2	Serial Clock Output, Side 2
SDA1	2	I/O	I/O	Serial Data, Side 1 Input/Output	Serial Data, Side 1 Input/Output
SDA2	7	I/O	I/O	Serial Data Input/Output, Side 2	Serial Data Input/Output, Side 2
VCC1	1	—	—	Supply Voltage, Side 1	Supply Voltage, Side 1
VCC2	8	—	—	Supply Voltage, Side 2	Supply Voltage, Side 2

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V	Voltage	VCC1, VCC2	–0.5	6	V
		SDA1, SCL1	–0.5	VCC1 + 0.5(3)	
		SDA2, SCL2	–0.5	VCC2 + 0.5(3)	
I_O	Output current	SDA1, SCL1	–20	20	mA
		SDA2, SCL2	–100	100	
$T_{J(MAX)}$	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values here within are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	Bus pins	±8000	V
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)		±1500	
		Machine Model JEDEC JESD22-A115-A, all pins		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
VCC1, VCC2	Supply Voltage	3	5.5	V
V_{SDA1}, V_{SCL1}	Input and Output Signal Voltages, Side 1	0	VCC1	V
V_{SDA2}, V_{SCL2}	Input and Output Signal Voltages, Side 2	0	VCC2	V
V_{IL1}	Low-Level Input Voltage, Side 1	0	0.5	V
V_{IH1}	High-Level Input Voltage, Side 1	0.7 × VCC1	VCC1	V
V_{IL2}	Low-Level Input Voltage, Side 2	0	0.3 x VCC2	V
V_{IH2}	High-Level Input Voltage, Side 2	0.7 × VCC2	VCC2	V
I_{OL1}	Output Current, Side 1	0.5	3.5	mA
I_{OL2}	Output Current, Side 2	0.5	35	mA
C_{b1}	Maximum Capacitive Load, Side 1		40	pF
C_{b2}	Maximum Capacitive Load, Side 2		400	pF
f_{MAX}	Maximum Operating Frequency (1)		1	MHz
T_A	Ambient Temperature	–40	125	°C
T_J	Junction Temperature	–40	136	°C
T_{SD}	Thermal Shutdown	139	171	°C

(1) This represents the maximum frequency with the maximum bus load (C_b) and the maximum current sink (I_O). If the system has less bus capacitance, then higher frequencies can be achieved.

7.4 Thermal Information

THERMAL METRIC (1)		ISO1540, ISO1541 D [SOIC] 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating conditions, unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT (3 V ≤ VCC1, VCC2 ≤ 3.6 V)								
I_{CC1}	Supply Current, Side 1	ISO1540	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2	See Figure 18; R_1,R_2 = Open, C_1,C_2 = Open		2.4	3.6	mA
		ISO1541				2.1	3.3	mA
I_{CC2}	Supply Current, Side 2	ISO1540 and ISO1541				1.7	2.7	mA
I_{CC1}	Supply Current, Side 1	ISO1540	V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2			2.5	3.8	mA
		ISO1541				2.3	3.6	mA
I_{CC2}	Supply Current, Side 2	ISO1540 and ISO1541				1.9	3.1	mA
SUPPLY CURRENT (4.5 V ≤ VCC1, VCC2 ≤ 5.5 V)								
I_{CC1}	Supply Current, Side 1	ISO1540	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2	See Figure 18; R_1,R_2 = Open, C_1,C_2 = Open		3.1	4.7	mA
		ISO1541				2.8	4.4	
I_{CC2}	Supply Current, Side 2	ISO1540 and ISO1541				2.3	3.7	mA
I_{CC1}	Supply Current, Side 1	ISO1540	V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2			3.1	4.7	mA
		ISO1541				2.9	4.5	
I_{CC2}	Supply Current, Side 2	ISO1540 and ISO1541				2.5	4	mA
SIDE 1 (ONLY)								
V_{ILT1}	Voltage Input Threshold “Low”, Side 1 (SDA1, SCL1)				500	550	660	mV
V_{IHT1}	Voltage Input Threshold “High”, Side 1 (SDA1, SCL1)				540	610	700	mV
V_{HYST1}	Voltage Input Hysteresis, Side 1 V_{IHT1}- V_{ILT1}				40	60		mV
V_{OL1} (1)	Low-Level Output Voltage, Side 1 (SDA1,SCL1)		0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA		650		800	mV
ΔV_{OIT1} (1)(2)	Low-Level Output Voltage to High-Level Input Voltage Threshold Difference, Side 1 (SDA1, SCL1)				50			mV
SIDE 2 (ONLY)								
V_{ILT2}	Voltage Input Threshold “Low”, Side 2 (SDA2, SCL2)				0.3 x VCC2		0.4 x VCC2	V
V_{IHT2}	Voltage Input Threshold “High”, Side 2 (SDA2, SCL2)				0.4 x VCC2		0.5 x VCC2	V
V_{HYST2}	Voltage Input Hysteresis, Side 2 V_{IHT2} - V_{ILT2}				0.05 x VCC2			V
V_{OL2}	Low-Level Output Voltage, Side 2 (SDA2, SCL2)		0.5 mA ≤ (I_{SDA2} and I_{SCL2}) ≤ 35 mA				0.4	V
BOTH SIDES								
$\|I_I\|$	Input Leakage Currents (SDA1, SCL1, SDA2, SCL2)		V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2			0.01	10	µA
C_I	Input Capacitance to Local Ground (SDA1, SCL1, SDA2, SCL2)		V_I = 0.4 x sin(2E6πt) + 2.5 V			7		pF
CMTI	Common-Mode Transient Immunity		See Figure 20		25	50		kV/µs
V_{CCUV} (3)	VCC Undervoltage Lockout Threshold (Side 1 and Side 2)				2.1	2.5	2.8	V

(1) This parameter does not apply to the ISO1541 SCL1 line as it is unidirectional.
(2) $\Delta V_{OIT1} = V_{OL1} – V_{IHT1}$. This represents the minimum difference between a Low-Level Output Voltage and a High-Level Input Voltage Threshold to prevent a permanent latch condition that would otherwise exist with bidirectional communication.
(3) Any VCC voltages, on either side, less than the minimum will ensure device lockout. Both VCC voltages greater than the maximum will prevent device lockout.

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
t_{SP}	Input Noise Filter		5	12		ns
t_{UVLO}	Time to recover from *Undervoltage Lock-out*	See Figure 21 2.7 V to 0.9 V	30	50	110	µs

7.7 Switching Characteristics

over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
3 V ≤ VCC1, VCC2 ≤ 3.6 V							
t_{f1}	Output Signal Fall Time (SDA1, SCL1)	See Figure 18 R_1 = 953 Ω, C_1 = 40 pF	0.7 × VCC1 to 0.3 × VCC1	8	17	29	ns
			0.9 × VCC1 to 900 mV	16	29	48	
t_{f2}	Output Signal Fall Time (SDA2, SCL2)	See Figure 18 R_2 = 95.3 Ω, C_2 = 400 pF	0.7 × VCC2 to 0.3 × VCC2	14	23	47	ns
			0.9 × VCC2 to 400 mV	35	50	100	
t_{pLH1-2}	Low-to-High Propagation Delay, Side 1 to Side 2	See Figure 18 R_1 = 953 Ω, R_2 = 95.3 Ω, C_1, C_2 = 10 pF	0.55 V to 0.7 × VCC2		33	65	ns
t_{PHL1-2}	High-to-Low Propagation Delay, Side 1 to Side 2		0.7 V to 0.4 V		90	181	ns
PWD_{1-2}	Pulse Width Distortion $\lvert t_{pHL1-2} - t_{pLH1-2} \rvert$				55	123	ns
t_{PLH2-1} (1)	Low-to-High Propagation Delay, Side 2 to Side 1		0.4 × VCC2 to 0.7 × VCC1		47	68	ns
t_{PHL2-1} (1)	High-to-Low Propagation Delay, Side 2 to Side 1		0.4 × VCC2 to 0.9 V		67	109	ns
PWD_{2-1} (1)	Pulse Width Distortion $\lvert t_{pHL2-1} - t_{pLH2-1} \rvert$				20	49	ns
t_{LOOP1} (1)	Round-trip propagation delay on Side 1	See Figure 19; R_1 = 953 Ω, C_1 = 40 pF R_2 = 95.3 Ω, C_2 = 400 pF	0.4 V to 0.3 × VCC1		100	165	ns
4.5 V ≤ VCC1, VCC2 ≤ 5.5 V							
t_{f1}	Output Signal Fall Time (SDA1, SCL1)	See Figure 18 R_1 = 1430 Ω, C_1 = 40 pF	0.7 × VCC1 to 0.3 × VCC1	6	11	20	ns
			0.9 × VCC1 to 900 mV	13	21	39	
t_{f2}	Output Signal Fall Time (SDA2, SCL2)	See Figure 18 R_2 = 143 Ω, C_2 = 400 pF	0.7 × VCC2 to 0.3 × VCC2	10	18	35	ns
			0.9 × VCC2 to 400 mV	28	41	76	
t_{pLH1-2}	Low-to-High Propagation Delay, Side 1 to Side 2	See Figure 18 R_1 = 1430 Ω, R_2 = 143 Ω, $C_{1,\ 2}$ = 10 pF	0.55 V to 0.7 × VCC2		31	62	ns
t_{PHL1-2}	High-to-Low Propagation Delay, Side 1 to Side 2		0.7 V to 0.4 V		70	139	ns
PWD_{1-2}	Pulse Width Distortion $\lvert t_{pHL1-2} - t_{pLH1-2} \rvert$				38	80	ns
t_{PLH2-1} (1)	Low-to-High Propagation Delay, Side 2 to Side 1		0.4 × VCC2 to 0.7 × VCC1		55	80	ns
t_{PHL2-1} (1)	High-to-Low Propagation Delay, Side 2 to Side 1		0.4 × VCC2 to 0.9 V		47	85	ns
PWD_{2-1} (1)	Pulse Width Distortion $\lvert t_{pHL2-1} - t_{pLH2-1} \rvert$				8	21	ns
t_{LOOP1} (1)	Round-trip propagation delay on Side 1	See Figure 19; R_1 = 1430 Ω, C1 = 40 pF R_2 = 143 Ω, C2 = 400 pF	0.4 V to 0.3 × VCC1		110	180	ns

(1) This parameter does not apply to the ISO1541 SCL1 line as it is unidirectional.

7.8 Typical Characteristics

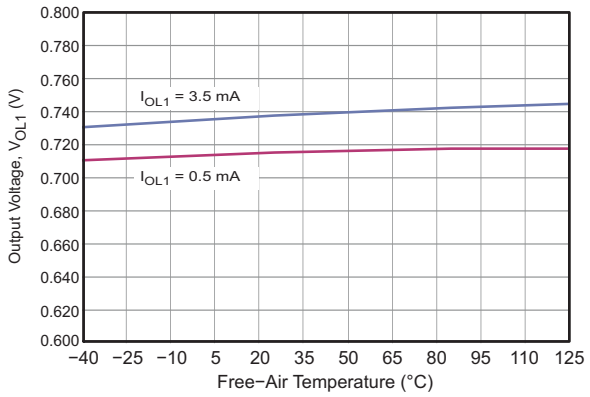


Figure 1. Side 1: Output Low Voltage vs Free-Air Temperature

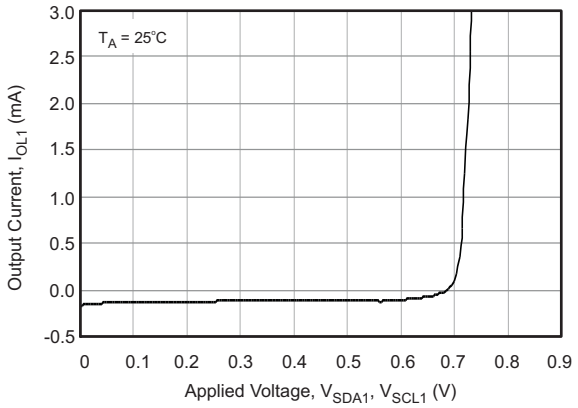


Figure 2. Side 1: Output Low Current vs S_{DA1} or S_{CL1} Applied Voltage

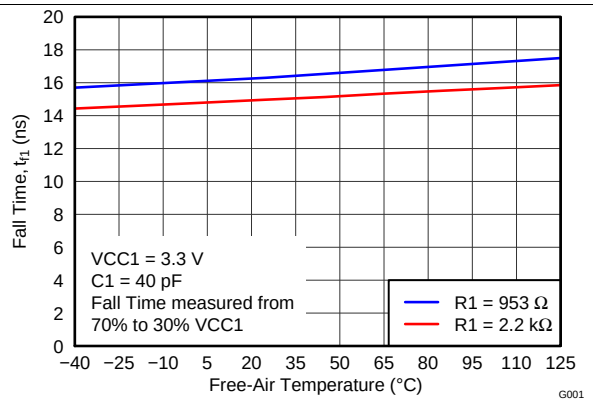


Figure 3. Side 1: Output Fall Time vs Free-Air Temperature

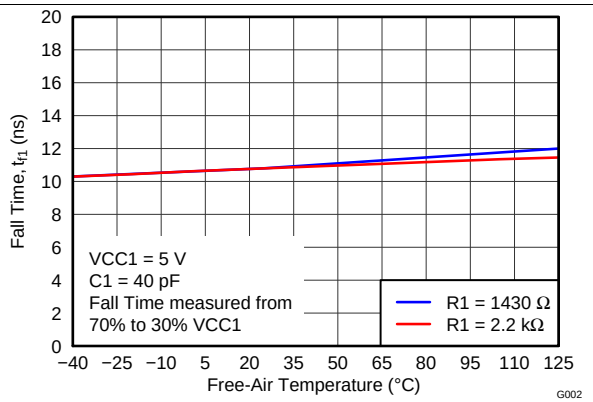


Figure 4. Side 1: Output Fall Time vs Free-air Temperature

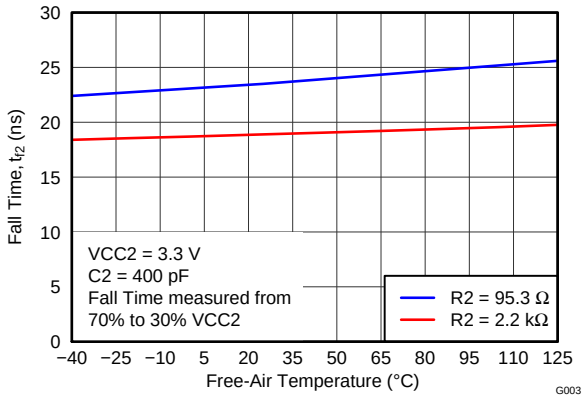


Figure 5. Side 2: Output Fall Time vs Free-Air Temperature

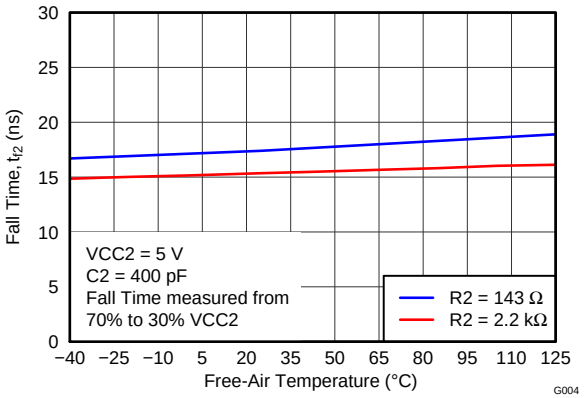


Figure 6. Side 2: Output Fall Time vs Free-Air Temperature

Typical Characteristics (continued)

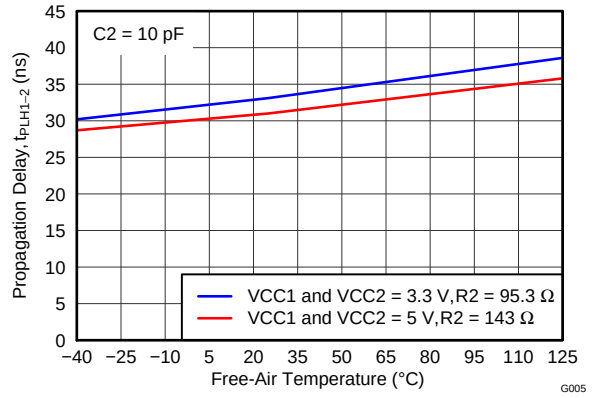


Figure 7. t_{PLH1-2} Propagation Delay vs Free-Air Temperature

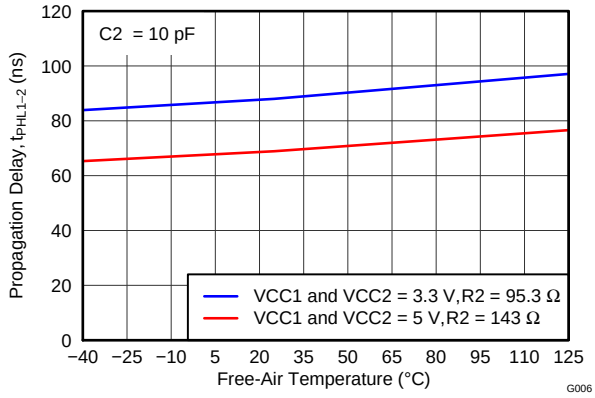


Figure 8. t_{PHL1-2} Propagation Delay vs Free-Air Temperature

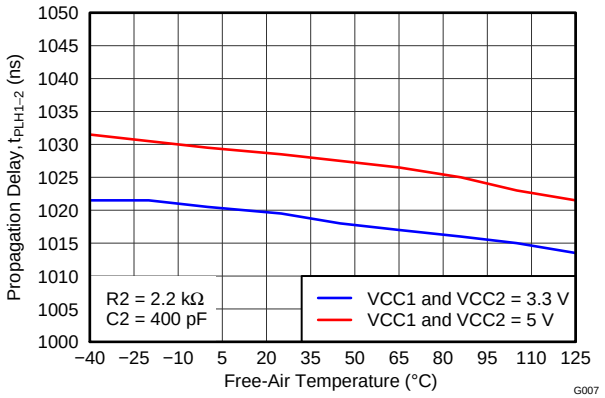


Figure 9. t_{PLH1-2} Propagation Delay vs Free-Air Temperature

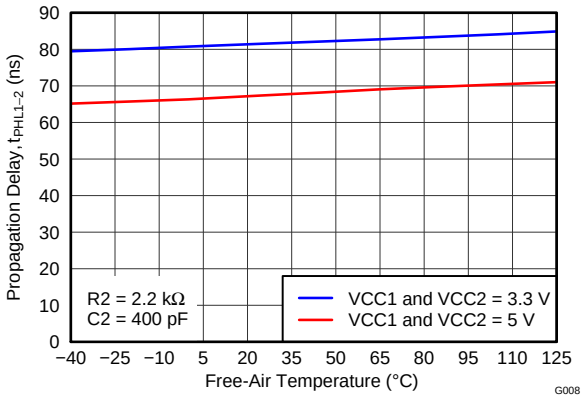


Figure 10. t_{PHL1-2} Propagation Delay vs Free-Air Temperature

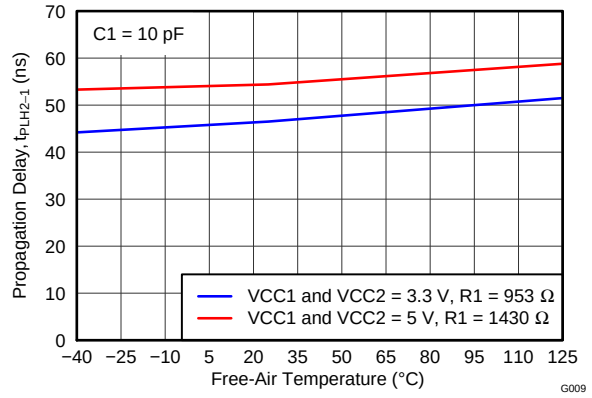


Figure 11. t_{PLH2-1} Propagation Delay vs Free-Air Temperature

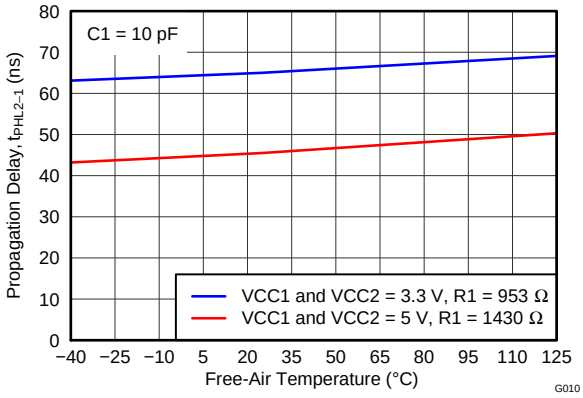


Figure 12. t_{PHL2-1} Propagation Delay vs Free-Air Temperature

Typical Characteristics (continued)

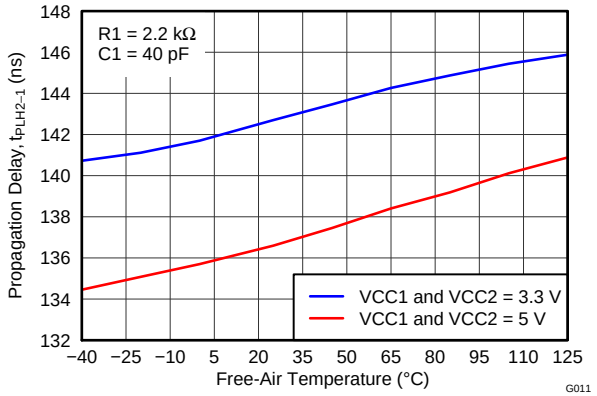


Figure 13. t_{PLH2-1} Propagation Delay vs Free-Air Temperature

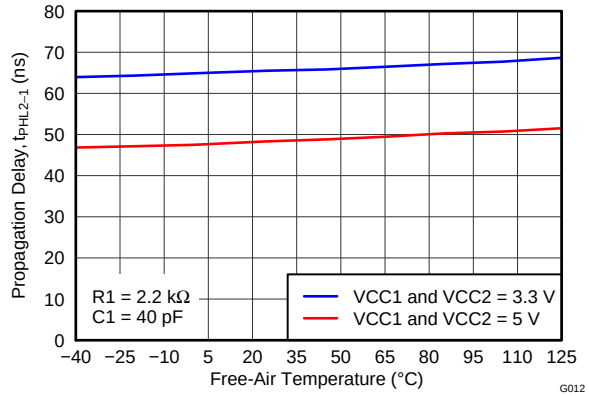


Figure 14. t_{PHL2-1} Propagation Delay vs Free-Air Temperature

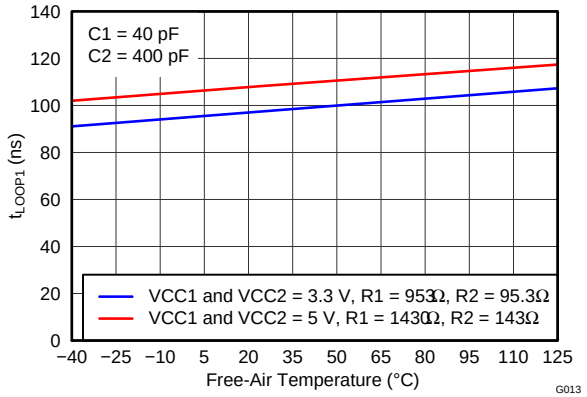


Figure 15. t_{LOOP1} vs Free-Air Temperature

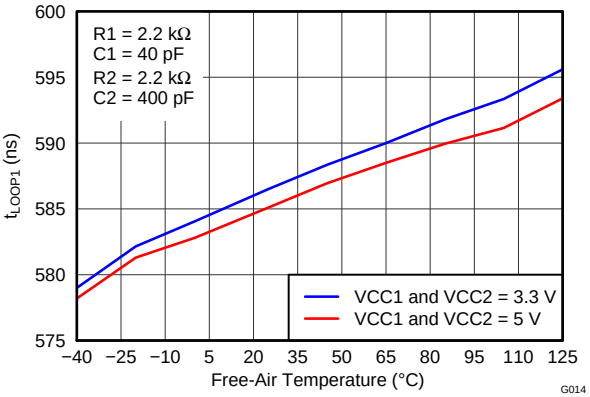


Figure 16. t_{LOOP1} vs Free-Air Temperature

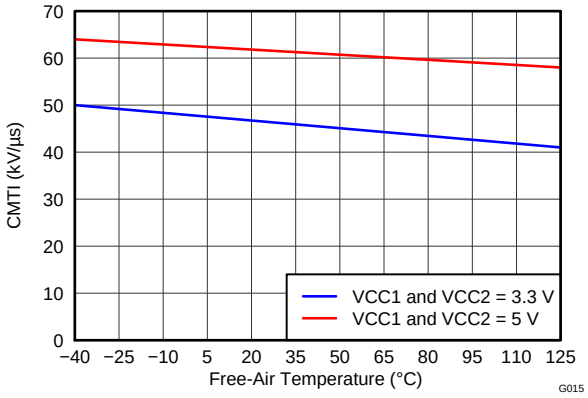


Figure 17. CMTI vs Free-Air Temperature

8 Parameter Measurement Information

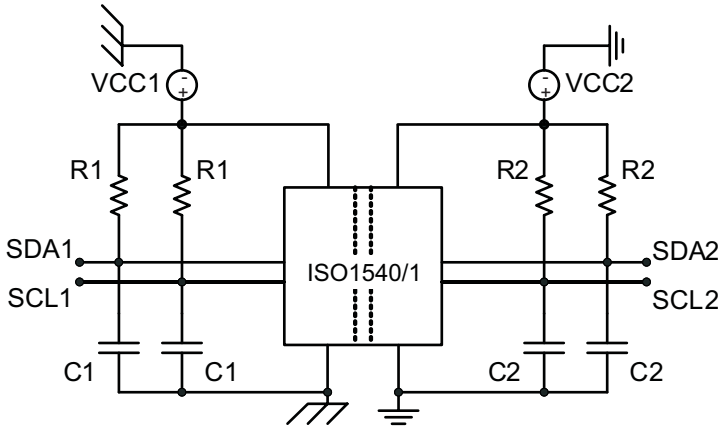


Figure 18. Test Diagram

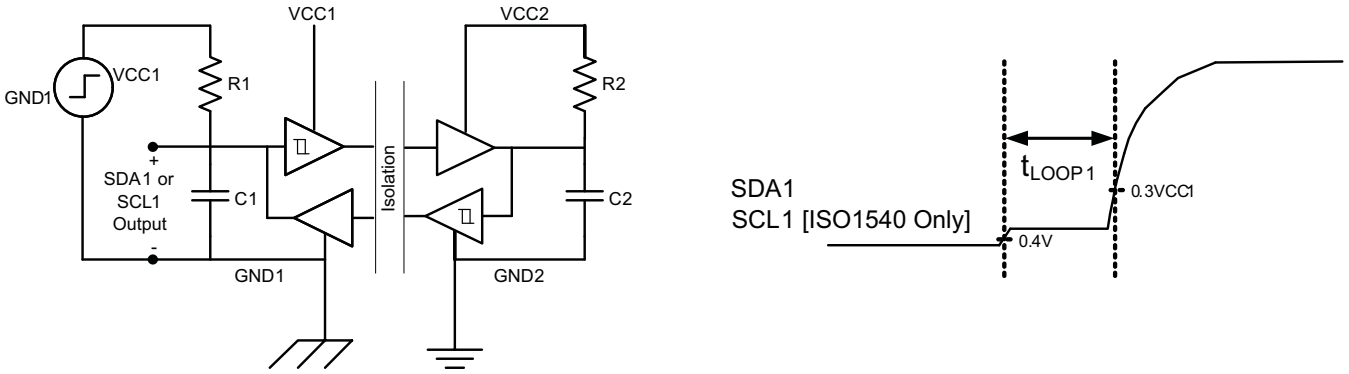


Figure 19. t_{Loop1} Setup and Timing Diagram

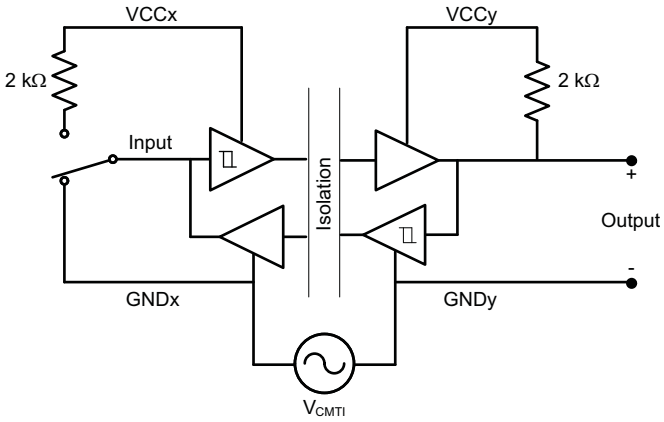
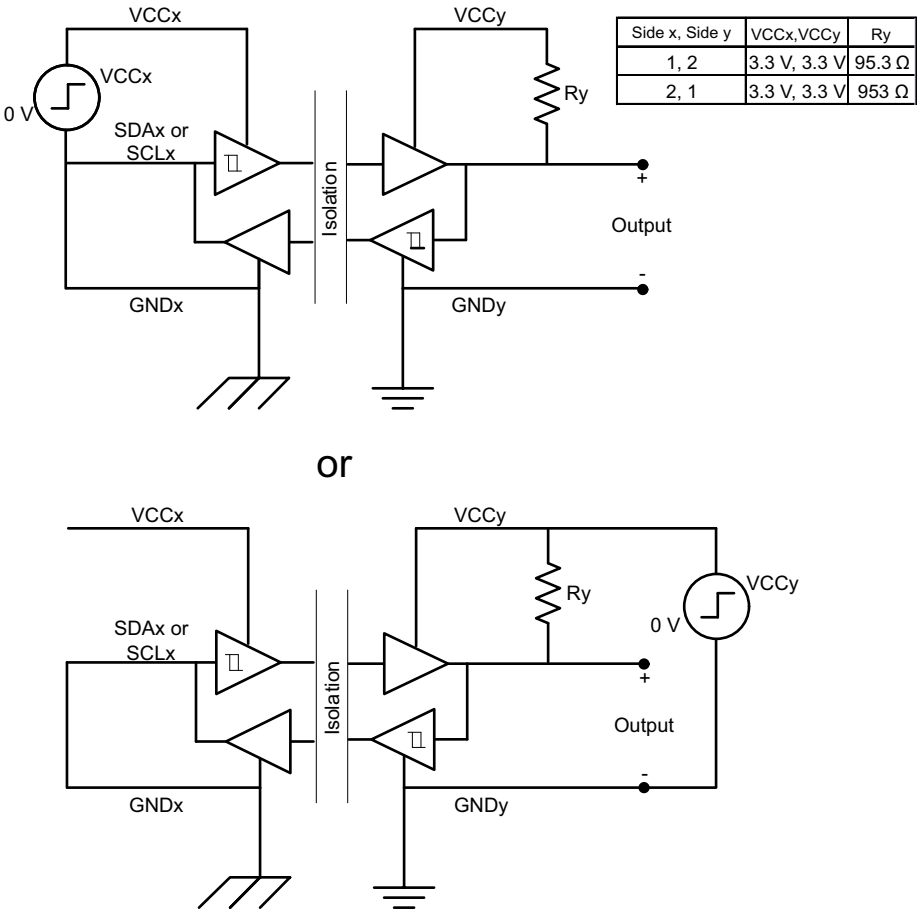


Figure 20. Common-Mode Transient Immunity Test Circuit

Parameter Measurement Information (continued)



Side x, Side y	VCCx,VCCy	Ry
1, 2	3.3 V, 3.3 V	95.3 Ω
2, 1	3.3 V, 3.3 V	953 Ω

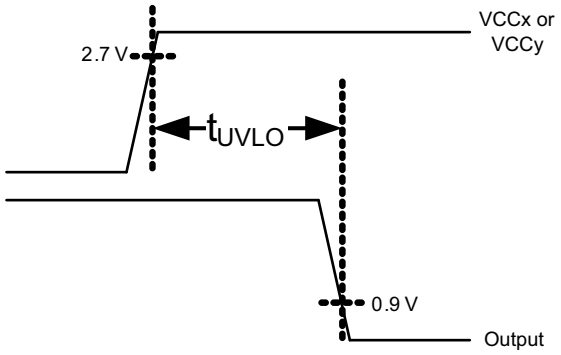


Figure 21. t_{UVLO} Test Circuit and Timing Diagrams

9 Detailed Description

9.1 Overview

The I^2C bus is used in a wide range of applications because it is simple to use. The bus consists of a two-wire communication bus that supports bidirectional data transfer between a master and several slaves. The master or processor controls the bus – in particular, the serial clock (SCL) line. Data is transferred between the master and slave through a serial data (SDA) line. This data can be transferred in four speeds: standard mode (0 to 100 kbps), fast mode (0 to 400 kbps), fast-mode plus (0 to 1 Mbps), and high-speed mode (0 to 3.4 Mbps). The most common speeds are the standard and fast modes.

The I^2C Bus operates in bidirectional, half-duplex mode, while standard digital isolators are unidirectional devices. To make efficient use of one technology supporting the other, external circuitry is required that separates the bidirectional bus into two unidirectional signal paths without introducing significant propagation delay. These devices have their logic input and output buffers separated by TI's capacitive isolation technology using a silicon dioxide (SiO_2) barrier. When used in conjunction with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

9.2 Functional Block Diagrams

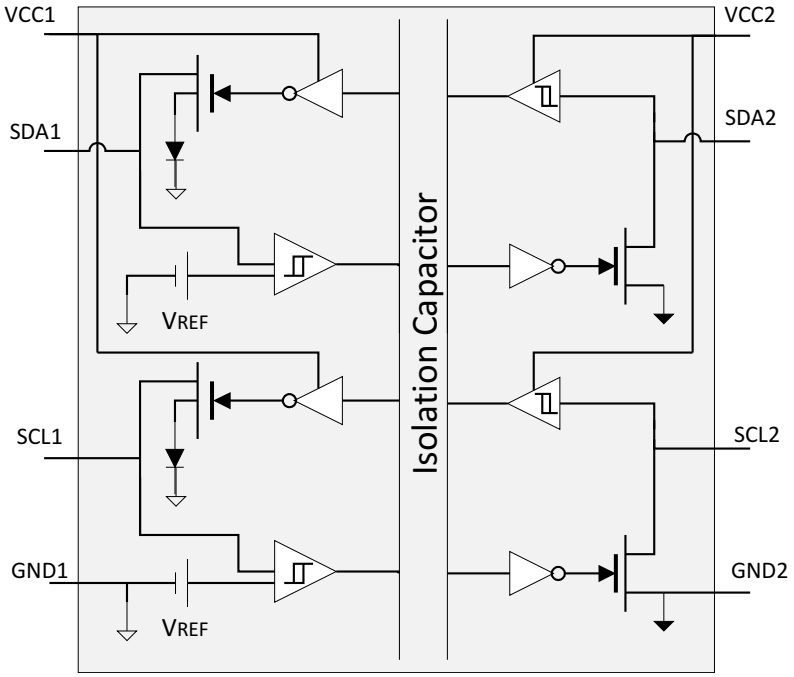


Figure 22. ISO1540 Block Diagram

Functional Block Diagrams (continued)

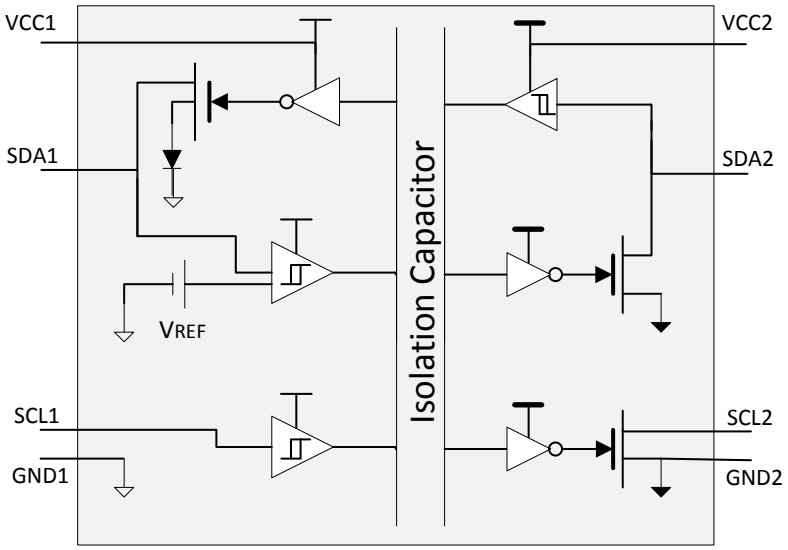


Figure 23. ISO1541 Block Diagram

9.3 Feature Description

The ISO device enables a complete isolated I²C interface to be implemented within a small form factor having following features:

Table 1. Features List

FEATURES DESCRIPTION	ISO1540	ISO1541
UL 1577 Isolation Voltage (Single) (Vrms)	2500	2500
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Transient Overvoltage Rating (Vpk)	4242	4242
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Working Voltage Rating (Vpk)	566	566
CSA Isolation Rating (Vrms)	2800	2800
CSA 60950-1 Basic Working (Vrms)	390	390
CSA 61010-1 Basic Working (Vrms)	300	300
CSA 61010-1 Reinforced Working (Vrms)	150	150
Data Rate (Mbps)	1	1
Number of Channels	2	2
Serial Clock	Bidirectional	Unidirectional
Serial Data	Bidirectional	Bidirectional
Operating Temperature (°C)	–40 to 125	–40 to 125
Pin/Package	SOIC (8)	SOIC (8)

9.3.1 Insulation and Safety-Related Specification for D-8 Package

over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	4.8			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	4.3			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	>400			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ T_A max		$>10^{11}$		Ω
C_{IO}	Barrier capacitance, input to output(1)	V_{IO} = 0.4 x sin(2E6πt)		1		pF
C_I	Input capacitance(2)		See *Electrical Characteristics*			pF

(1) All pins on each side of the barrier tied together creating a 2-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific application isolation standards. Care should be taken to maintain these distances on a board design to ensure that the mounting pads for the isolator do not reduce this distance.

Creepage and clearance on the printed-circuit-board (PCB) become equal in certain cases. Techniques such as inserting grooves and/or ribs on the PCB are used to help increase these specifications.

9.3.2 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Insulation Characteristics(3)

over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		566	V_{PEAK}
V_{PR}	Input-to-Output test voltage	Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, Partial Discharge < 5 pC	906	V_{PEAK}
		Method b1, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.875$, t = 1 s (100% production), Partial Discharge < 5 pC	1062	
		After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial Discharge < 5 pC	680	
V_{IOTM}	Transient overvoltage	$V_{TEST} = V_{OITM}$ t = 60 s (qualification) t = 1 s (100% production)	4242	V_{PEAK}
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(3) Climatic Classification 40/125/21

9.3.3 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–III
	Rated mains voltage ≤ 400 V_{RMS}	I–II

9.3.4 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current-limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	D-8	$R_{\theta JA}$ = 114.6°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			198	mA
			$R_{\theta JA}$ = 114.6°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			303	
T_S	Maximum case temperature					150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in *Absolute Maximum Ratings*. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in *Thermal Information* is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

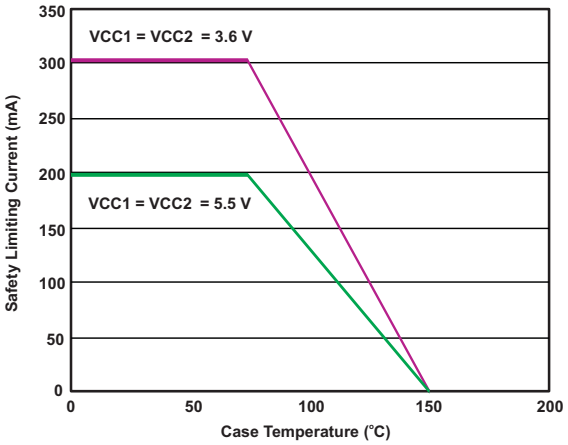


Figure 24. ISO154x Thermal Derating Curve

9.3.5 Regulatory Information

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1	Certified according to CSA Component Acceptance Notice 5A, CSA/IEC 60950-1 and CSA/IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK} Maximum Working Voltage, 566 V_{PK}	Basic insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed), 390 V_{RMS} maximum working voltage Basic insulation per CSA 61010-1-04 and IEC 61010-1 (2nd Ed), 300 V_{RMS} maximum working voltage Reinforced insulation per CSA 61010-1-04 and IEC 61010-1 (2nd Ed), 150 V_{RMS} maximum working voltage	Single Protection Isolation Voltage, 2500 V_{RMS} (1)	Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Master contract number: 220991	File number: E181974	Certificate number : CQC14001109540

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

9.4 Device Functional Modes

ISO154x functional modes are shown in Table 2.

Table 2. Function Table (1)

POWER STATE	INPUT	OUTPUT
VCC1 or VCC2 < 2.1 V	X	Z
VCC1 and VCC2 > 2.8 V	L	L
VCC1 and VCC2 > 2.8 V	H	Z
VCC1 and VCC2 > 2.8 V	Z (2)	?

(1) H = High Level; L = Low Level; Z = High Impedance or Float; X = Irrelevant; ? = Indeterminate
(2) Invalid input condition as an I^2C system requires that a pullup resistor to VCC is connected.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 I^2C Bus Overview

The Inter-Integrated Circuit (I^2C) bus is a single-ended, multi-master, 2-wire bus for efficient inter-IC communication in half-duplex mode.

I^2C uses open-drain technology, requiring two lines, Serial Data (SDA) and Serial Clock (SCL), to be connected to VDD by resistors (see Figure 25). Pulling the line to ground is considered a logic Zero while letting the line float is a logic One. This is used as a channel access method. Transitions of logic states must occur while SCL is Low, transitions while SCL is high indicate START and STOP conditions. Typical supply voltages are 3.3 V and 5 V, although systems with higher or lower voltages are permitted.

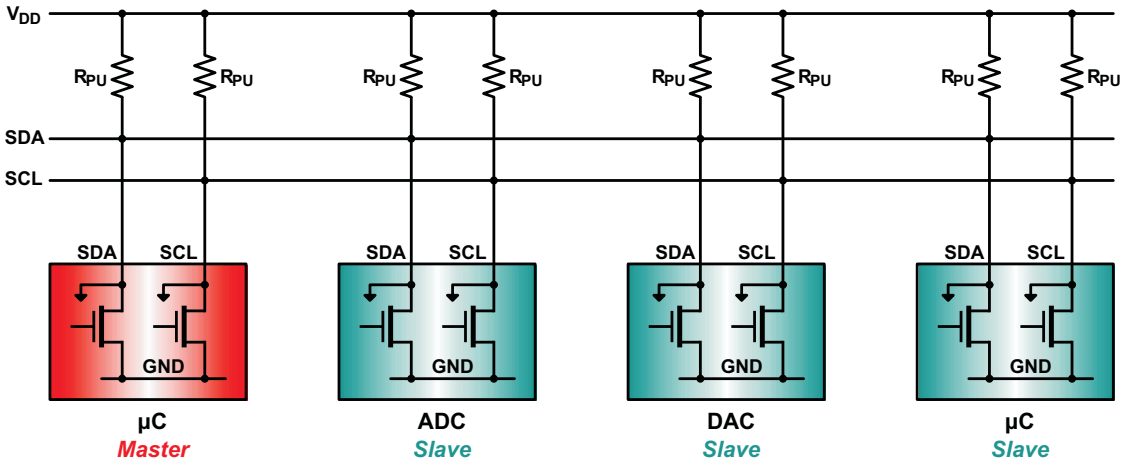


Figure 25. I^2C Bus

I^2C communication uses a 7-bit address space with 16 reserved addresses, so a theoretical maximum of 112 nodes can communicate on the same bus. In praxis, however, the number of nodes is limited by the specified, total bus capacitance of 400 pF, which restricts communication distances to a few meters.

The specified signaling rates for the ISO1540 and ISO1541 are 100 kbps (Standard mode), 400 kbps (Fast mode), 1 Mbps (Fast mode plus).

The bus has two roles for nodes: master and slave. A master node issues the clock, slave addresses, and also initiates and ends data transactions. A slave node receives the clock and addresses and responds to requests from the master. Figure 26 shows a typical data transfer between master and slave.

Application Information (continued)

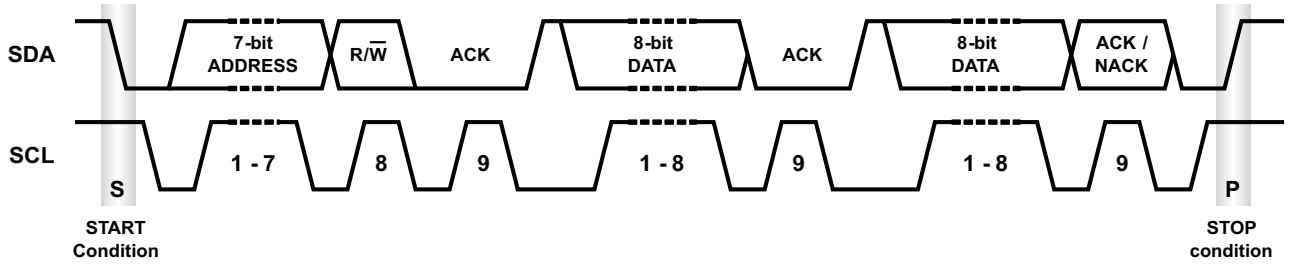


Figure 26. Timing Diagram of a Complete Data Transfer

The master initiates a transaction by creating a START condition, following by the 7-bit address of the slave it wishes to communicate with. This is followed by a single Read/Write bit, representing whether the master wishes to write to (0), or to read from (1) the slave. The master then releases the SDA line to allow the slave to acknowledge the receipt of data.

The slave responds with an acknowledge bit (ACK) by pulling SDA low during the entire high time of the 9th clock pulse on SCL, after which the master continues in either transmit or receive mode (according to the R/W bit sent), while the slave continues in the complementary mode (receive or transmit, respectively).

The address and the 8-bit data bytes are sent most significant bit (MSB) first. The START bit is indicated by a high-to-low transition of SDA while SCL is high. The STOP condition is created by a low-to-high transition of SDA while SCL is high.

If the master writes to a slave, it repeatedly sends a byte with the slave sending an ACK bit. In this case, the master is in master-transmit mode and the slave is in slave-receive mode.

If the master reads from a slave, it repeatedly receives a byte from the slave, while acknowledging (ACK) the receipt of every byte but the last one (see Figure 27). In this situation, the master is in master-receive mode and the slave is in slave-transmit mode.

The master ends the transmission with a STOP bit, or may send another START bit to maintain bus control for further transfers.

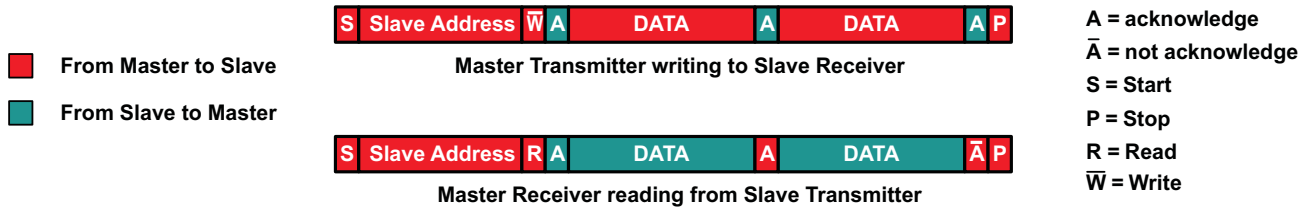


Figure 27. Transmit or Receive Mode Changes During a Data Transfer

When writing to a slave, a master mainly operates in transmit-mode and only changes to receive-mode when receiving acknowledgment from the slave.

When reading from a slave, the master starts in transmit-mode and then changes to receive-mode after sending a READ request (R/W bit = 1) to the slave. The slave continues in the complementary mode until the end of a transaction.

Note, that the master ends a reading sequence by not acknowledging (NACK) the last byte received. This procedure resets the slave state machine and allows the master to send the STOP command.

Application Information (continued)

10.1.2 Isolator Functional Principle

To isolate a bidirectional signal path (SDA or SCL), the ISO1540 internally splits a bidirectional line into two unidirectional signal lines, each of which is isolated through a single-channel digital isolator. Each channel output is made open-drain to comply with the open-drain technology of I^2C. Side 1 of the ISO1540 connects to a low-capacitance I^2C node, while Side 2 is designed for connecting to a fully loaded I^2C bus with up to 400 pF capacitance.

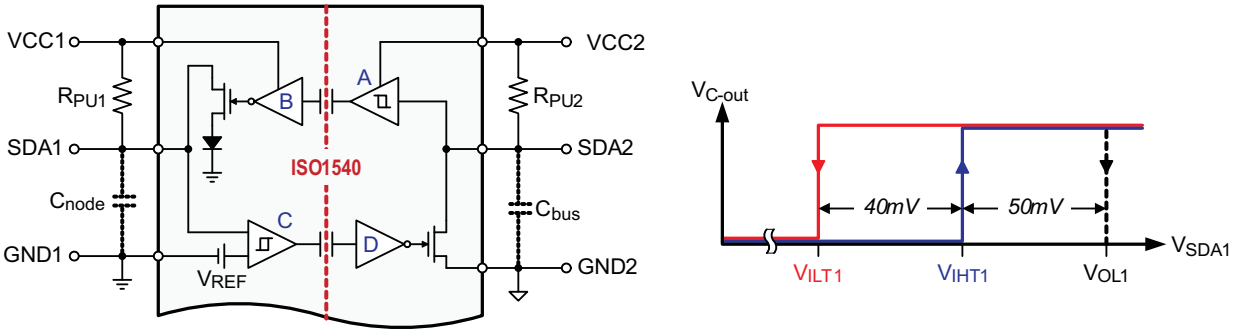


Figure 28. SDA Channel Design and Voltage Levels at SDA1

At first sight, the arrangement of the internal buffers suggests a closed signal loop that is prone to latch-up. However, this loop is broken by implementing an output buffer (B) whose output low-level is raised by a diode drop to approximately 0.75 V, and the input buffer (C) that consists of a comparator with defined hysteresis. The comparator's upper and lower input thresholds then distinguish between the proper low-potential of 0.4 V maximum driven directly by SDA1 and the buffered output low-level of B.

Figure 29 demonstrate the switching behavior of the I^2C isolator, ISO1540, between a master node at SDA1 and a heavy loaded bus at SDA2.

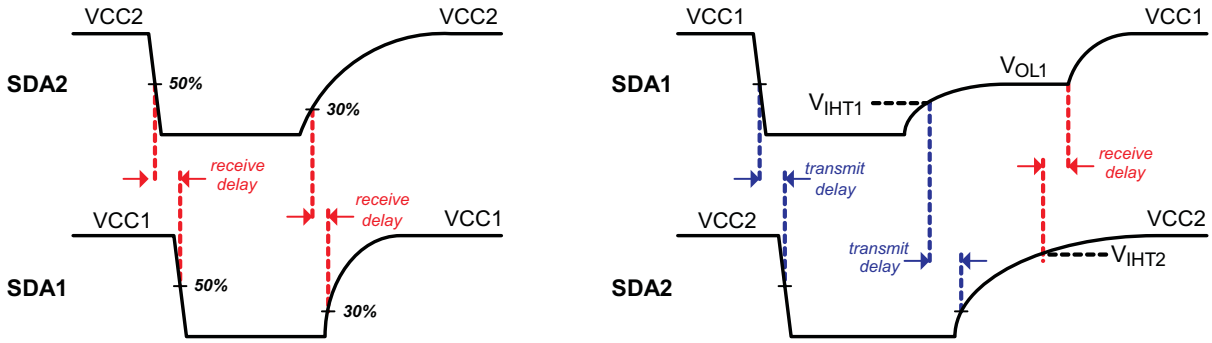


Figure 29. SDA Channel Timing in Receive and Transmit Directions

10.1.2.1 Receive Direction (Left Diagram of Figure 29)

When the I^2C bus drives SDA2 low, SDA1 follows after a certain delay in the receive path. Its output low will be the buffered output of V_{OL1} = 0.75 V, which is sufficiently low to be detected by Schmitt-trigger inputs with a minimum input-low voltage of V_{IL} = 0.9 V at 3 V supply levels.

Once SDA2 is released, its voltage potential increases towards VCC2 following the time-constant formed by R_{PU2} and C_{bus}. After the receive delay, SDA1 is released and also rises towards VCC1, following the time-constant $R_{PU1} \times C_{node}$. Because of the significant lower time-constant, SDA1 may reach VCC1 before SDA2 reaches VCC2 potential.

Application Information (continued)

10.1.2.2 Transmit Direction (Right Diagram of Figure 29)

When a master drives SDA1 low, SDA2 follows after a certain delay in the transmit direction. When SDA2 turns low it also causes the output of buffer B to turn low but at a higher 0.75 V level. This level cannot be observed immediately as it is overwritten by the master's lower low-level.

However, when the master releases SDA1, its voltage potential increases and first must pass the upper input threshold of the comparator, V_{IHT1}, to release SDA2. SDA1 then increases further until it reaches the buffered output level of V_{OL1} = 0.75 V, maintained by the receive path. Once comparator C turns high, SDA2 is released after the delay in transmit direction. It takes another receive delay until B's output turns high and fully releases SDA1 to move toward VCC1 potential.

10.2 Typical Application

In Figure 30, the ultra low-power micro controller, MSP430G2132, controls the I²C data traffic of configuration data and conversion results for the analog inputs and outputs. Low-power data converters build the analog interface to sensors and actuators. The ISO1541 provides the necessary isolation between different ground potentials of the system controller, remote sensor, and actuator circuitry to prevent ground loop currents that otherwise may falsify the acquired data.

The entire circuit operates from a single 3.3-V supply. A low-power push-pull converter, SN6501, drives a center-tapped transformer whose output is rectified and linearly regulated to provide a stable 5-V supply for the data converters.

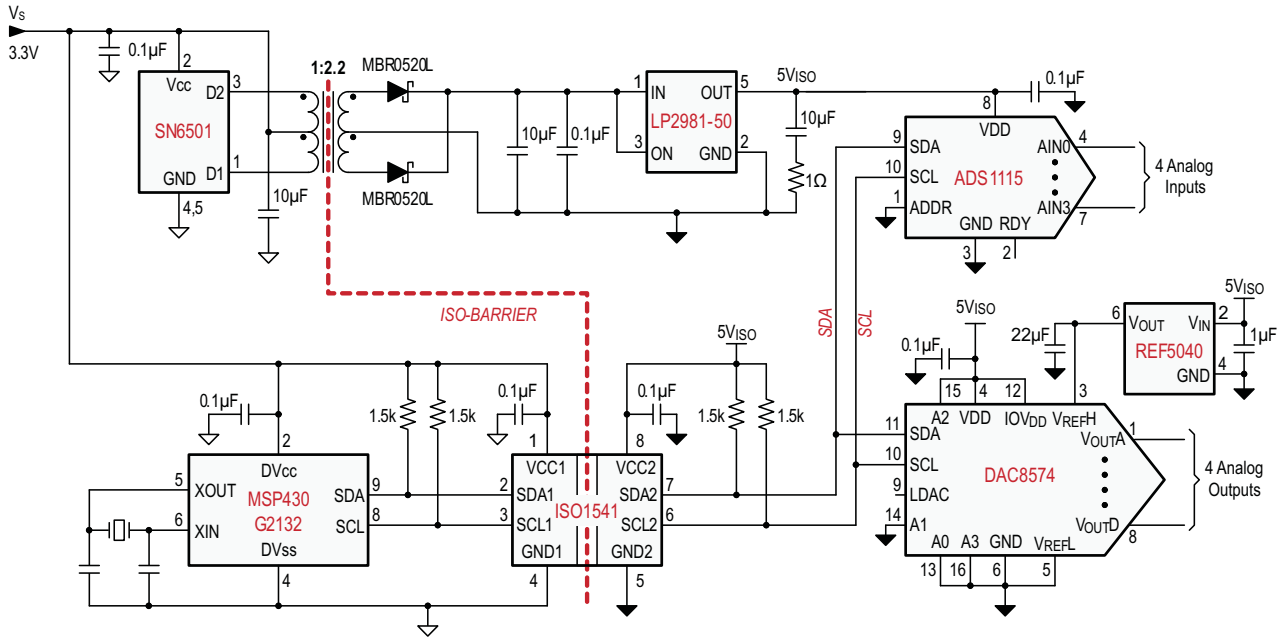


Figure 30. Isolated I²C Data Acquisition System

10.2.1 Design Requirements

Recommended power supply voltages (VCC1 and VCC2) must be from 3 V to 5.5 V. Recommended decoupling capacitor of 0.1-µF is required between both VCC1 to GND1 and VCC2 to GND2, to take care of power supply voltages transient and to ensure reliable operation at all data rates.

Typical Application (continued)

10.2.2 Detailed Design Procedure

The power supply capacitor of 0.1-µF must be placed as close to the power supply pins as possible. Recommended placement of capacitors must be 2-mm maximum from input and output power supply pins (VCC1 and VCC2).

Maximum load permissible on input SDA1 and SCL1 lines is ≤ 40 pF and on output lines SDA2 and SCL2 is ≤ 400 pF.

Minimum pullup resistors on input SDA1 and SCL1 lines to VCC1 must be chosen in such a way that input current drawn is ≤ 3.5 mA. Minimum pullup resistors on input SDA2 and SCL2 lines to VCC2 must be chosen in such a way that output current drawn is ≤ 35 mA. Whereas maximum pullup resistors on input lines (SDA1 and SCL1) to VCC1 and on output lines (SDA1 and SCL1) to VCC2, will depend on load and rise time requirements on respective lines.

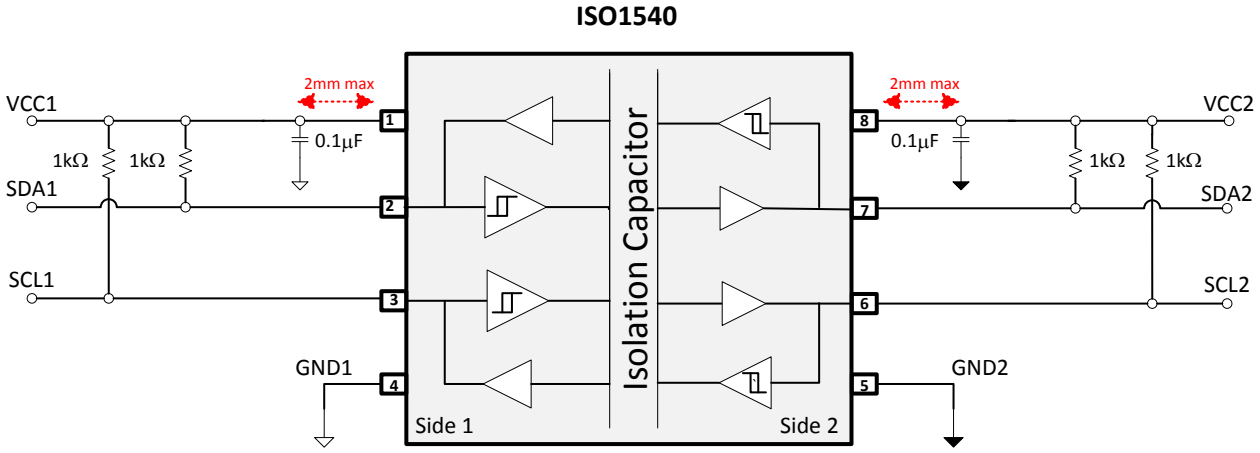


Figure 31. Typical ISO1540 Circuit Hookup

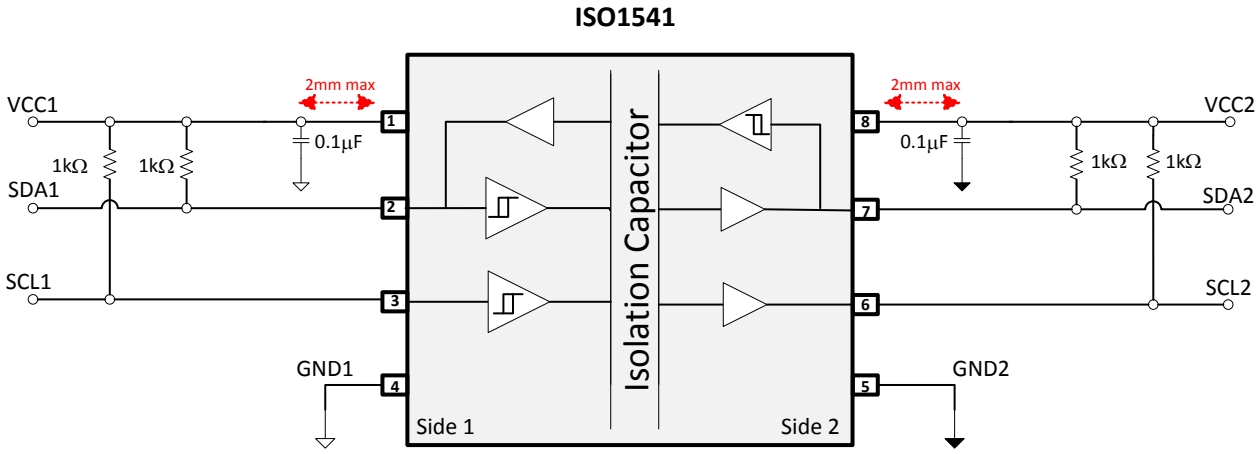


Figure 32. Typical ISO1541 Circuit Hookup

Typical Application (continued)

10.2.3 Application Curve

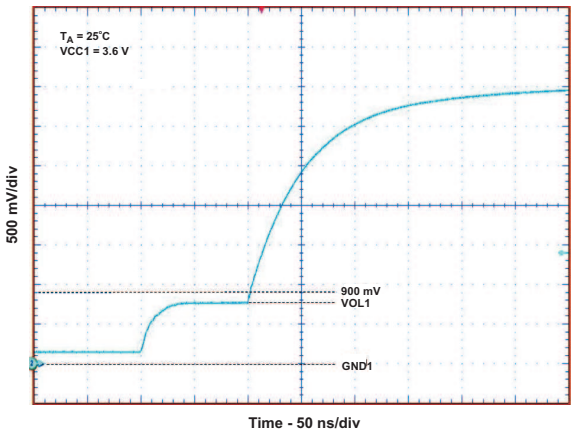


Figure 33. Side 1: Low-to-High Transition

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, TI recommends a 0.1-µF bypass capacitor at input and output supply pins (VCC1 and VCC2). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 34). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

NOTE

For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, SLLA284.

12.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over less expensive alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

12.2 Layout Example

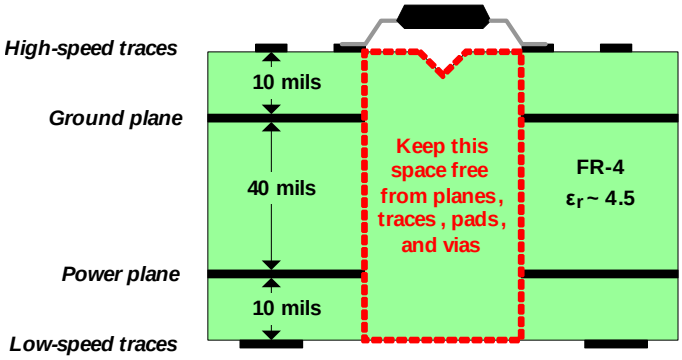


Figure 34. Recommended Layer Stack

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- SLLSEA0, *Transformer Driver for Isolated Power Supplies*
- SLLA284, *Digital Isolator Design Guide*
- SLLA353, *TI Isolation Glossary*

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO1540	Click here	Click here	Click here	Click here	Click here
ISO1541	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO1540D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IS1540	Samples
ISO1540DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IS1540	Samples
ISO1541D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IS1541	Samples
ISO1541DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IS1541	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

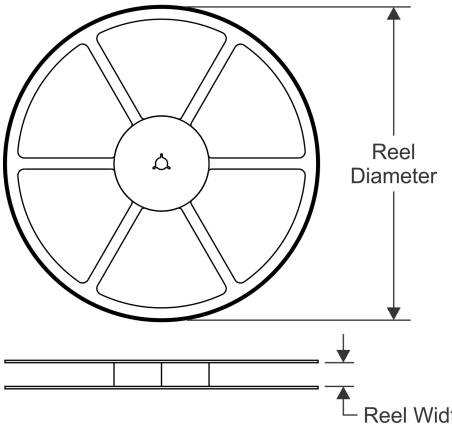
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

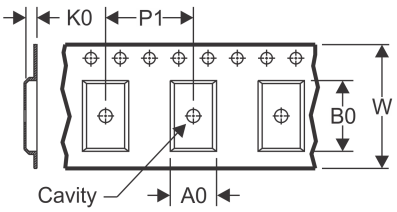
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

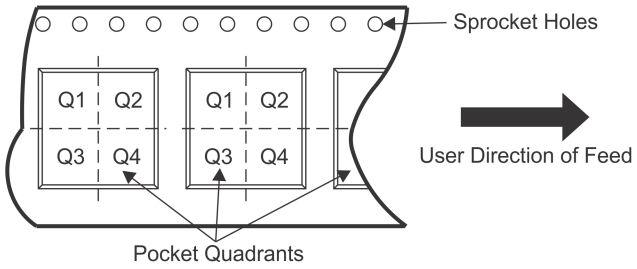


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

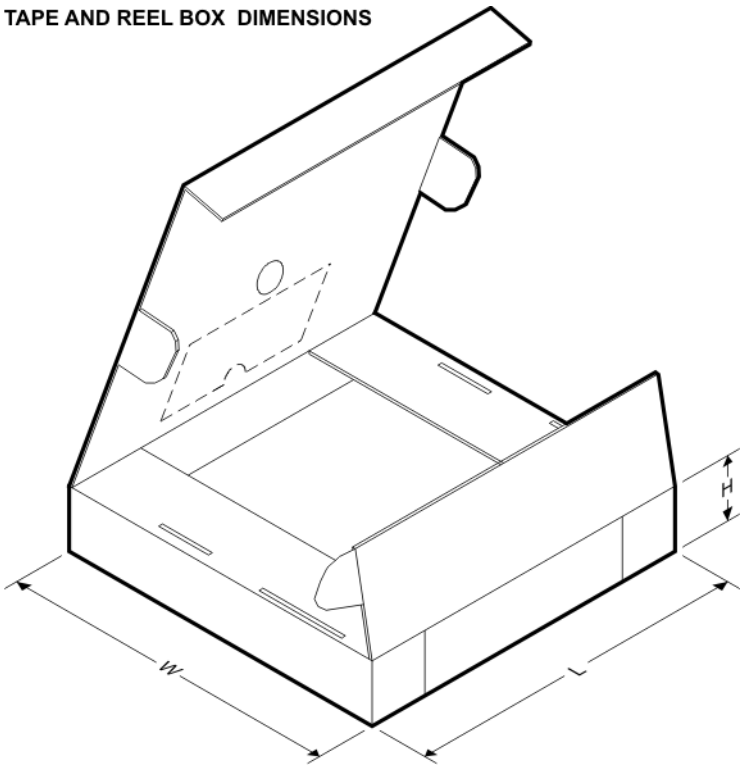
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1540DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO1541DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

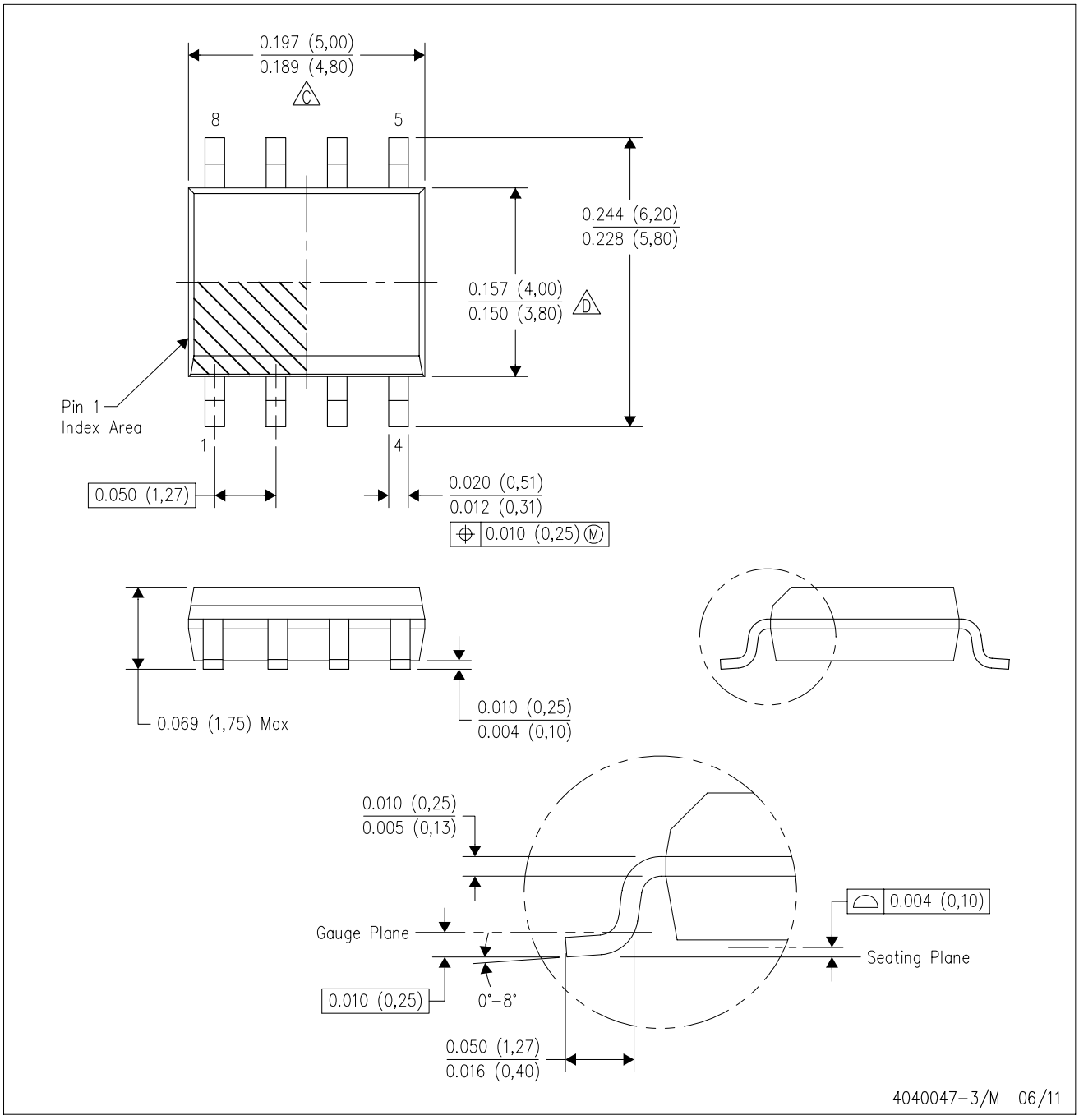
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1540DR	SOIC	D	8	2500	367.0	367.0	35.0
ISO1541DR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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