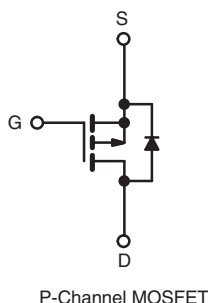
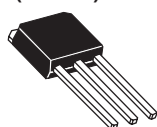




Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	- 200	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	3.0
Q_g (Max.) (nC)	8.9	
Q_{gs} (nC)	2.1	
Q_{gd} (nC)	3.9	
Configuration	Single	

DPAK
(TO-252)IPAK
(TO-251)

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR9210/SiHFR9210)
- Straight Lead (IRFU9210/SiHFU9210)
- Available in Tape and Reel
- P-Channel
- Fast Switching
- Lead (Pb)-free Available

RoHS*
COMPLIANT

DESCRIPTION

The Power MOSFETs technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness. The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU/SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR9210PbF	IRFR9210TRPbF ^a	-	IRFU9210PbF
	SiHFR9210-E3	SiHFR9210T-E3 ^a	-	SiHFU9210-E3
SnPb	IRFR9210	IRFR9210TR ^a	IRFR9210TRL ^a	IRFU9210
	SiHFR9210	SiHFR9210T ^a	SiHFR9210TL ^a	SiHFU9210

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 200	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at -10 V	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	- 7.6	W/ $^\circ\text{C}$
Linear Derating Factor		0.20	
Linear Derating Factor (PCB Mount) ^e		0.020	mJ
Single Pulse Avalanche Energy ^b	E_{AS}	300	
Repetitive Avalanche Current ^a	I_{AR}	- 1.9	A
Repetitive Avalanche Energy ^a	E_{AR}	2.5	mJ
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	W
Maximum Power Dissipation (PCB Mount) ^e		$T_A = 25^\circ\text{C}$	
Peak Diode Recovery dV/dt ^c	dV/dt	- 5.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	260 ^d	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = -50$ V, starting $T_J = 25^\circ\text{C}$, $L = 124$ mH, $R_G = 25\ \Omega$, $I_{AS} = -1.9$ A (see fig. 12).c. $I_{SD} \leq -1.9$ A, $dI/dt \leq 70$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.

d. 1.6 mm from case.

e. When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	-	50	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	5.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 200	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = - 1 mA		-	- 0.23	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 200 V, V _{GS} = 0 V		-	-	- 100	μA
		V _{DS} = - 160 V, V _{GS} = 0 V, T _J = 125 °C		-	-	- 500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 1.1 A ^b	-	-	3.0	Ω
Forward Transconductance	g _{fs}	V _{DS} = - 50 V, I _D = - 1.1 A		0.98	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 5		-	170	-	pF
Output Capacitance	C _{oss}			-	54	-	
Reverse Transfer Capacitance	C _{rss}			-	16	-	
Total Gate Charge	Q _g	V _{GS} = - 10 V	I _D = - 1.3 A, V _{DS} = - 160 V, see fig. 6 and 13 ^b	-	-	8.9	nC
Gate-Source Charge	Q _{gs}			-	-	2.1	
Gate-Drain Charge	Q _{gd}			-	-	3.9	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 100 V, I _D = - 2.3 A, R _G = 24 Ω, R _D = 41 Ω, see fig. 10 ^b		-	8.0	-	ns
Rise Time	t _r			-	12	-	
Turn-Off Delay Time	t _{d(off)}			-	11	-	
Fall Time	t _f			-	13	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 1.9	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	- 7.6	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = - 1.9 A, V _{GS} = 0 V ^b		-	-	- 5.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = - 2.3 A, dI/dt = 100 A/μs ^b		-	110	220	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.56	1.1	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

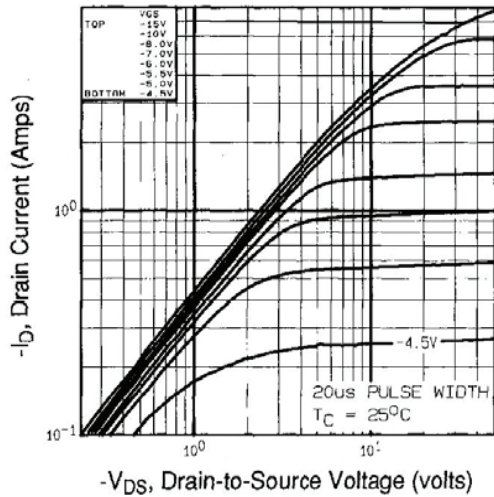


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

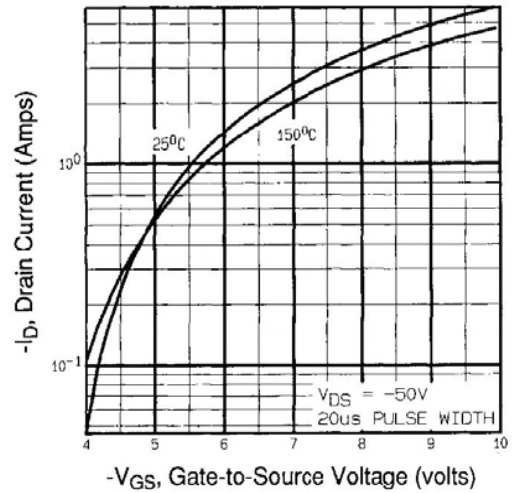


Fig. 3 - Typical Transfer Characteristics

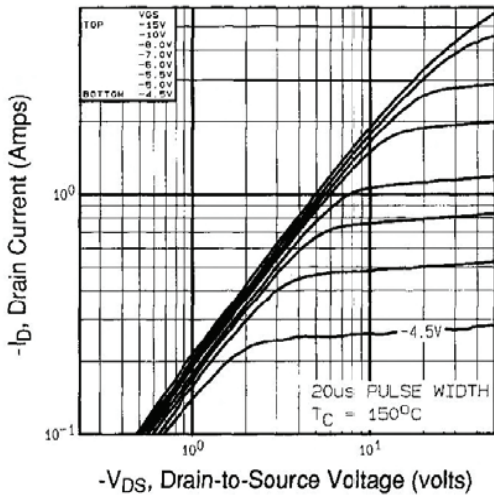


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

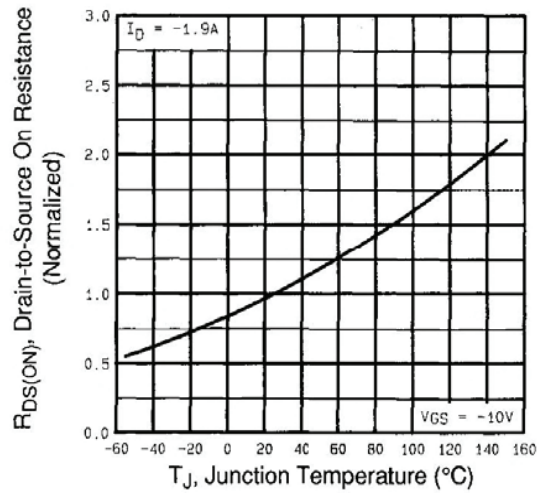


Fig. 4 - Normalized On-Resistance vs. Temperature

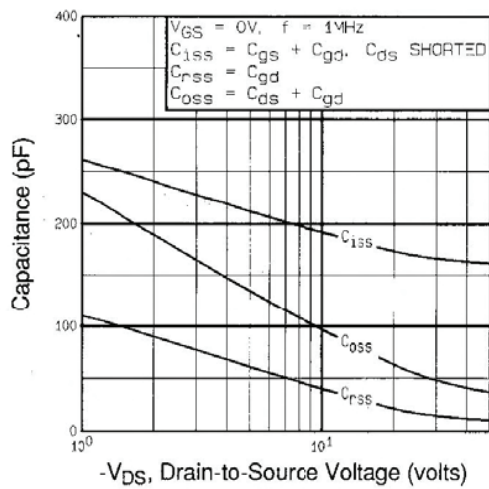


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

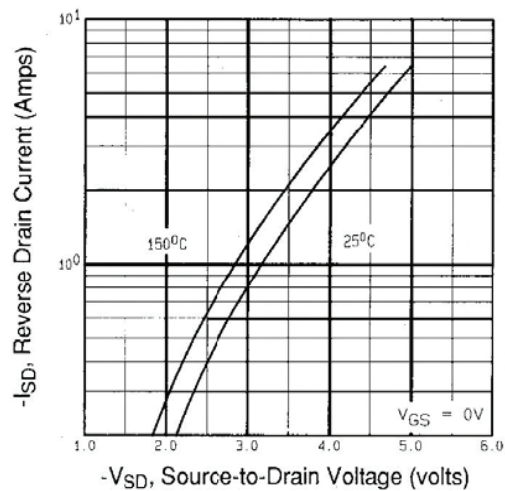


Fig. 7 - Typical Source-Drain Diode Forward Voltage

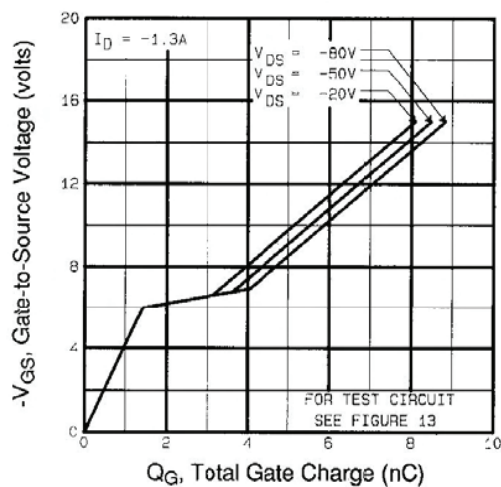


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

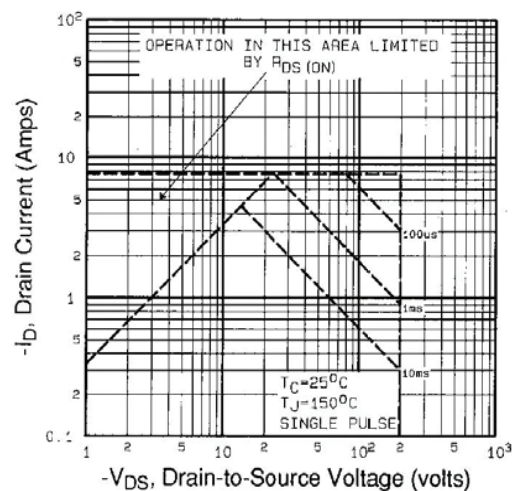


Fig. 8 - Maximum Safe Operating Area

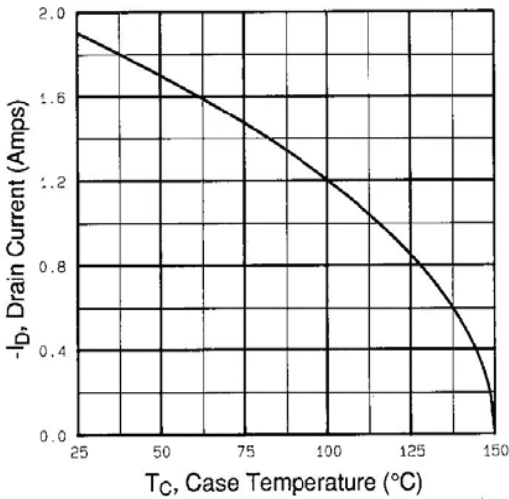


Fig. 9 - Maximum Drain Current vs. Case Temperature

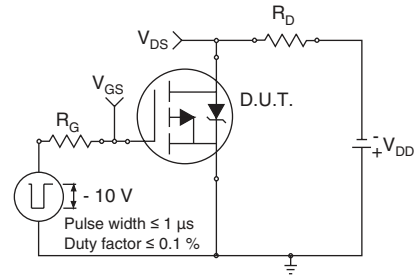


Fig. 10a - Switching Time Test Circuit

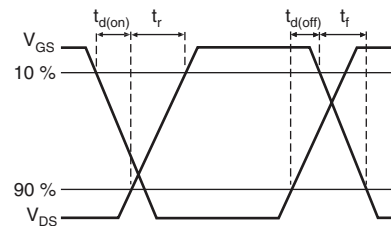


Fig. 10b - Switching Time Waveforms

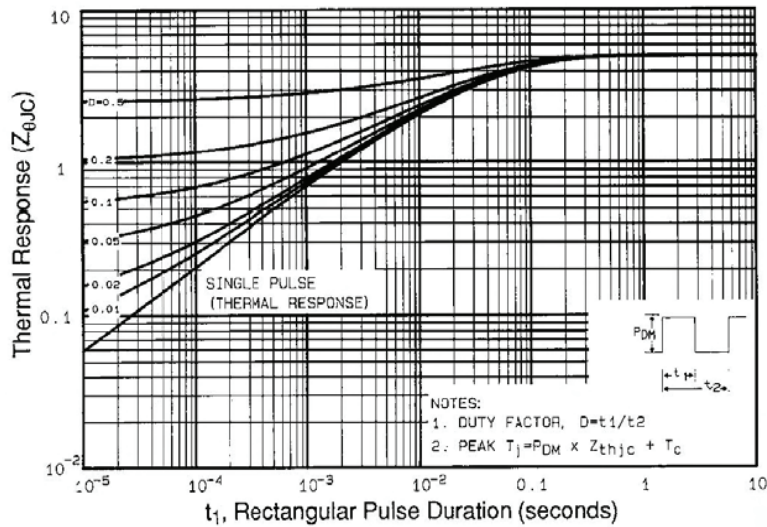


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

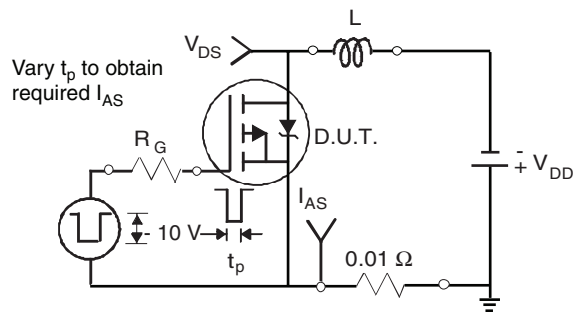


Fig. 12a - Unclamped Inductive Test Circuit

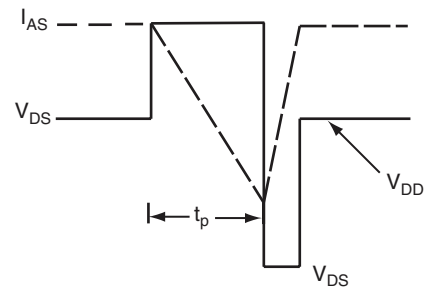


Fig. 12b - Unclamped Inductive Waveforms

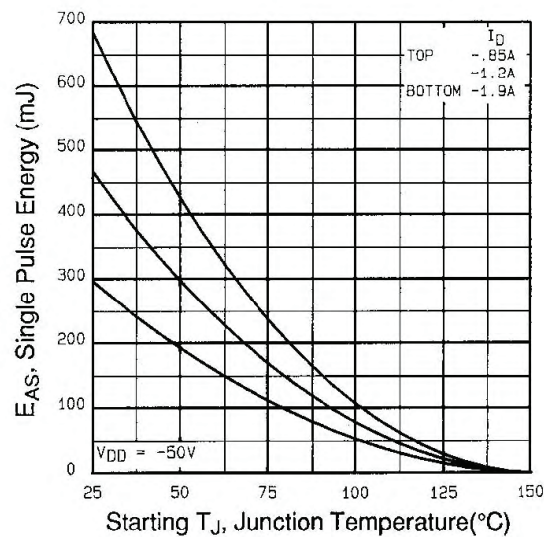


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

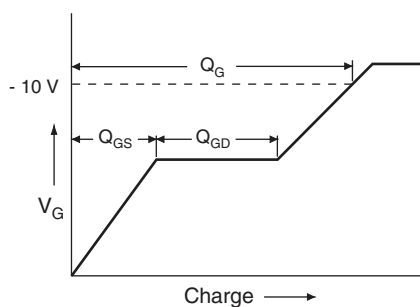


Fig. 13a - Basic Gate Charge Waveform

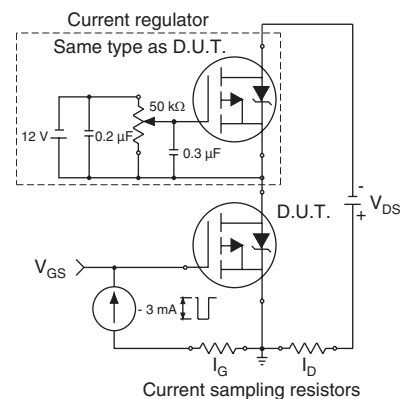
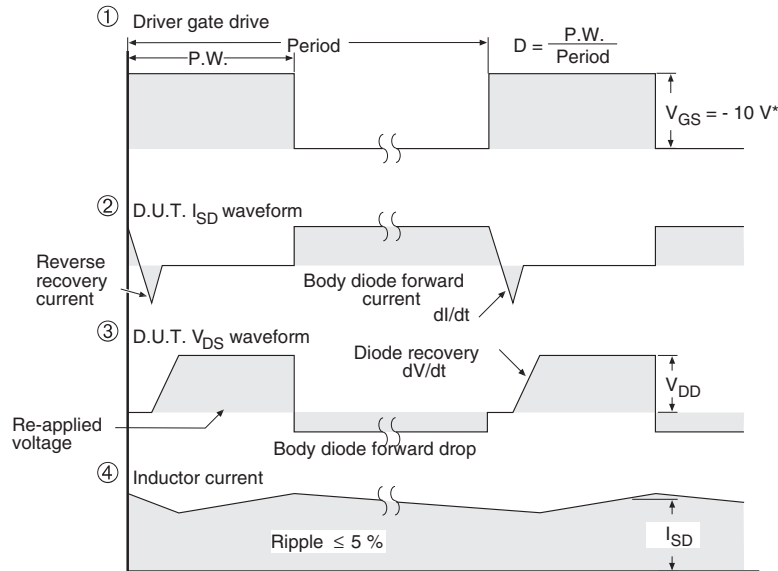
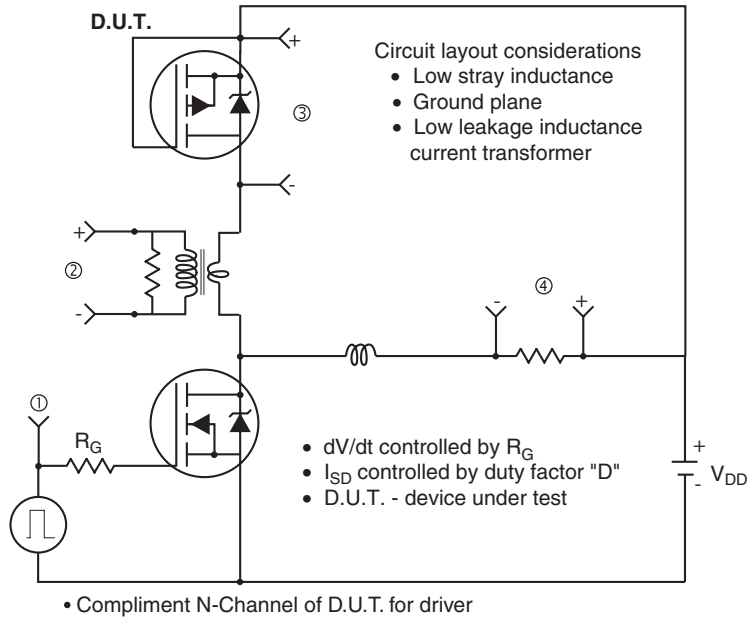


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 14 - For P-Channel

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