v2.1 UFS Memory

MTFC32GASAONS-IT, MTFC64GASAONS-IT, MTFC128GASAONS-IT, MTFC256GASAONS-IT

Features

- Universal flash storage (UFS) controller and NAND Flash
- V_{CC}: 2.7–3.6V
- V_{CCQ2}: 1.7–1.95V
- JEDEC/UFS specification version 2.1-compliant[1]
  - Advanced 6-signal interface
  - Differential I/O pins
  - 2 lanes supported
  - High speed: Gear 1/2/3 supported
  - Permanent and power-on write protection
  - Boot operation (high-speed boot)
  - Sleep mode
  - Replay-protected memory block (RPMB)
  - Background operation
  - Reliable write
  - Discard/Erase
  - Command queuing
  - FFU
  - Cache
- JEDEC/UFS specification version 3.0-features[2]
  - REFRESH operation
  - Temperature event notification
- Retention qualifications:
  - 5 years @55°C at 10% of PE
  - 1 year @55°C at maximum PE
- Package compliance:
  - RoHS certification
  - BGA, MSL3

Options	Marking
• Density	
– 32GB	32G
– 64GB	64G
– 128GB	128G
– 256GB	256G
• NAND component	
– 32Gbit	AS
• Controller	AO
• Packages – JEDEC-standard	
– 153-ball TFBGA	NS
• Operating and storage temperature ranges[3]	
– From –40°C to + 95°C	IT

Notes:
1. The JEDEC specification is available at https://www.jedec.org/sites/default/files/docs/JESD220C.pdf.
2. The JEDEC specification is available at https://www.jedec.org/sites/default/files/docs/JESD220D.pdf.
3. Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the package.

Part Numbering Information

Micron® UFS memory devices are available in different configurations and densities.

Figure 1: UFS Part Numbering

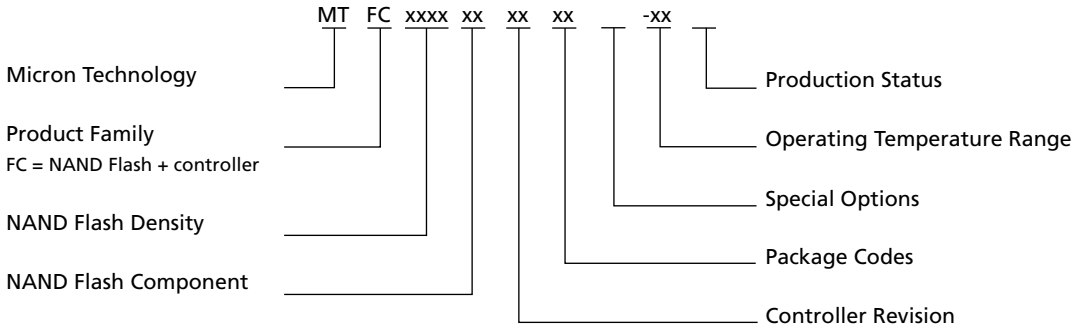

Table 1: Ordering Information

Base Part Number	Density	Package
MTFC32GASAONS-IT	32GB	153-ball TFBGA 11.5mm × 13mm × 1.2mm
MTFC64GASAONS-IT	64GB	
MTFC128GASAONS-IT	128GB	
MTFC256GASAONS-IT	256GB	

Note: 1. All the above MPNs can be ordered in the shipping form of tray and tape and reel.

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder.

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General Description

Micron universal flash storage (UFS) is a communication and mass data storage device that includes an M-PHY interface, one or more NAND Flash components, and a controller on an advanced 6-signal bus, which is compliant with the UFS system specification. Its cost per bit, small package sizes, and high reliability make it an ideal choice for industrial applications like infrastructure and networking equipment, PC and servers, a variety of other industrial and portable products.

The nonvolatile UFS draws no power to maintain stored data, delivers high performance across a wide range of operating temperatures, and resists shock and vibration disruption.

UFS Performance and Current Consumption

Table 2: Performance

Condition[1]		Typical Values				Unit
		32GB	64GB	128GB	256GB	
Sequential	Write	130	250	500	625	MB/s
	Read	500	940	950	950	MB/s
Random	Write	24,000	49,000	65,000	65,000	IOPS
	Read	26,000	47,000	70,000	70,000	IOPS

Note: 1. Two lanes, high-speed mode gear 3; Sequential access of 512KB chunk; Random access of 4KB chunk; Command queue depth = 32; Burst performance.

Additional performance data is provided in a separate document upon customer request, such as sustained and system performance on a specific application board, in system programming performance in manufacturing environment with Micron proprietary solution.

Table 3: Active Current Consumption

Condition	Typical Values (I_{CC}/I_{CCQ2})[1]				Peak Values (I_{CC}/I_{CCQ2})[2]				Unit
	32GB	64GB	128GB	256GB	32GB	64GB	128GB	256GB	
Write	60/365	105/365	150/365	255/365	250/560	400/560	550/560	700/560	mA
Read	50/465	105/465	115/465	130/465	200/560	360/560	450/560	510/560	mA

Notes: 1. Two lanes, high-speed mode gear 3; V_{CC} = 3.3V; V_{CCQ2} = 1.8V; T_{OPER} = 85°C, measurements done as average RMS current consumption.
2. Two lanes, high-speed mode gear 3; V_{CC} = 3.3V; V_{CCQ2} = 1.8V; T_{OPER} = 85°C, measurements done as maximum of average values in any 4µs operation windows.

Table 4: Low-Power Mode

Condition[1]	Typical Values (I_{CC}/I_{CCQ2})				Maximum Values (I_{CC}/I_{CCQ2})				Unit
	32GB	64GB	128GB	256GB	32GB	64GB	128GB	256GB	
Sleep	35/500	45/500	70/500	120/500	70/650	100/650	150/650	300/650	µA
Idle	35/500	45/500	70/500	120/500	70/650	100/650	150/650	300/650	µA

Note: 1. Two lanes, low-speed mode PWM gear 1, M-PHY in hibernate; V_{CC} = 3.3V; V_{CCQ2} = 1.8V; T_{OPER} = 25°C.

Signal Descriptions

Table 5: Signal Descriptions

Symbol	Type	Description
REF_CLK	Input	Reference clock: When not active, this signal should be pull-down or driven LOW by the host SoC
RST_n	Input	Hardware reset signal
D_{IN0}_t, D_{IN0}_c	Input	Downstream data lane 0: Differential input signals into UFS device from the host
D_{IN1}_t, D_{IN1}_c	Input	Downstream data lane 1: Differential input signals into UFS device from the host
D_{OUT0}_t, D_{OUT0}_c	Output	Upstream data lane 0: Differential output signals from the UFS device to the host
D_{OUT1}_t, D_{OUT1}_c	Output	Upstream data lane 1: Differential output signals from the UFS device to the host
VSF[9:1]	Input/ Output	Vendor specific function: VSF[9:1] must be left floating; VSF2 is not used. Exposing VSF balls on test points is recommended.
V_{CC}	Supply	Supply voltage for the NAND memory device
V_{CCQ2}	Supply	Supply voltage used for the M-PHY interface and the memory controller
V_{DDiQ}	Input	Input terminal to provide bypass capacitor for internal regulator related to the memory controller
V_{SS}	Supply	Ground
NC	–	No connect: NC pins must be connected to ground or left floating
RFU	–	Reserved for future use: RFU pins must be left floating

Signal Assignments

Figure 2: 153-Ball (Top View, Ball Down)

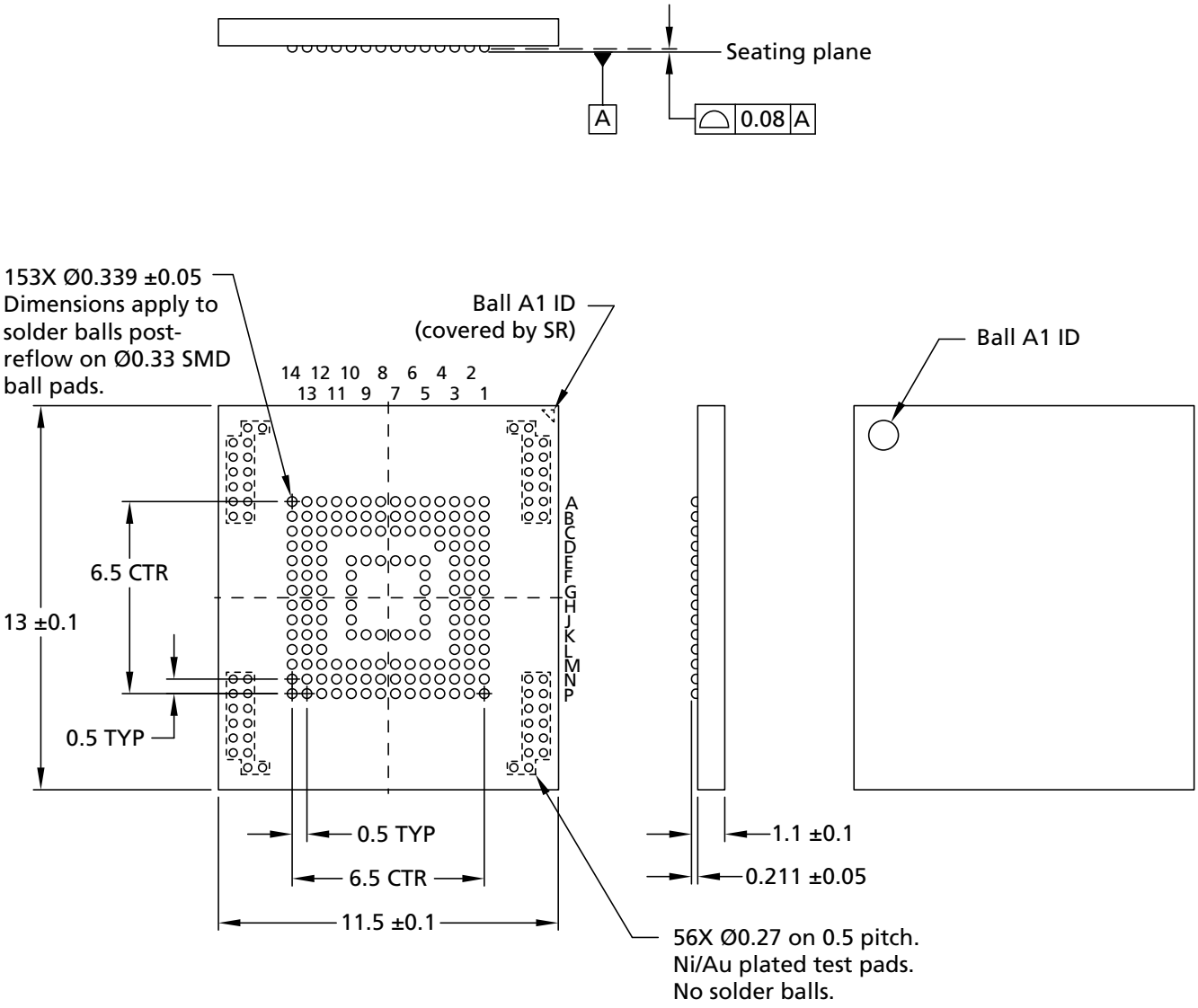
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	V_{DDiQ}	NC	NC	V_{CCQ2}	V_{CCQ2}	NC	NC	NC	NC	NC	NC	NC	A
B	NC	V_{SS}	RFU	NC	NC	V_{CCQ2}	V_{CCQ2}	V_{CC}	V_{CC}	NC	V_{SS}	V_{SS}	RFU	NC	B
C	V_{SS}	V_{SS}	V_{SS}	NC	NC	V_{CCQ2}	V_{CCQ2}	V_{CC}	V_{CC}	RFU	V_{SS}	V_{SS}	RFU	RFU	C
D	$D_{IN1\_}t$	$D_{IN1\_}c$	V_{SS}	NC								V_{SS}	V_{SS}	V_{SS}	D
E	V_{SS}	V_{SS}	V_{SS}		NC	VSF1	NC	V_{CC}	VSF3	VSF4		V_{SS}	RFU	RFU	E
F	$D_{IN0\_}t$	$D_{IN0\_}c$	V_{SS}		NC					VSF5		V_{SS}	V_{SS}	V_{SS}	F
G	V_{SS}	V_{SS}	V_{SS}		VSF6					V_{SS}		V_{SS}	RFU	RFU	G
H	REF_ CLK	RST_n	V_{SS}		V_{SS}					V_{SS}		V_{SS}	V_{SS}	V_{SS}	H
J	V_{SS}	V_{SS}	V_{SS}		V_{SS}					VSF7		V_{SS}	RFU	RFU	J
K	$D_{OUT0\_}c$	$D_{OUT0\_}t$	V_{SS}		V_{SS}	V_{CCQ2}	V_{CCQ2}	V_{CC}	NC	VSF8		V_{SS}	V_{SS}	V_{SS}	K
L	V_{SS}	V_{SS}	V_{SS}									V_{SS}	RFU	RFU	L
M	$D_{OUT1\_}c$	$D_{OUT1\_}t$	V_{SS}	V_{SS}	V_{SS}	RFU	RFU	NC	NC	RFU	NC	V_{SS}	V_{SS}	V_{SS}	M
N	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	RFU	RFU	V_{CC}	V_{CC}	RFU	V_{SS}	V_{SS}	RFU	NC	N
P	NC	NC	RFU	V_{SS}	V_{SS}	RFU	RFU	V_{CC}	V_{CC}	VSF9	V_{SS}	V_{SS}	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Top View (ball down)

Note: 1. The following balls are not connected in this product family, although specified by JEDEC Standard No. 21-C: A[5:4], A[12:8], B[5:4], B10, C[5:4], E5, E7 and F5.

Package Dimensions

Figure 3: 153-Ball TFBGA – 11.5mm × 13.0mm × 1.2mm (Package Code: NS)



Note: 1. Dimensions are in millimeters.

Architecture

Figure 4: UFS Functional Block Diagram

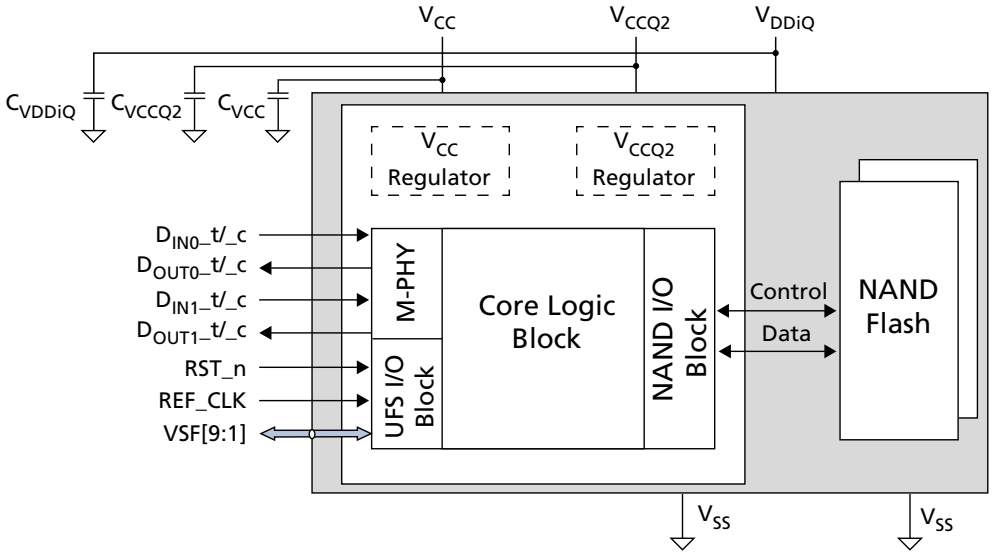


Table 6: Recommended Capacitor Values

Parameters	Symbol	Min	Typ	Max	Unit
V_{CC} capacitor	C_{VCC}	1.0	4.7	–	µF
V_{CCQ2} capacitor	C_{VCCQ2}	1.0	4.7	–	µF
V_{DDiQ} capacitor[2]	C_{VDDiQ}	0	4.7	–	µF

Notes:
1. An additional capacitor on each of the three lines can be added with a value about 1/10th that of the current capacitors.
2. V_{DDiQ} capacitor is optional.

UFS M-PHY Attributes

Micron device supports 2-lane configuration. Attribute values in the tables below apply to both lanes (lane 0 and lane 1).

Table 7: PHY M-TX Capability Attributes

Name	ID	Value	Type	Notes
TX_HSMODE_Capability	01h	01h	R	0 = FALSE
				1 = TRUE
TX_HSGEAR_Capability	02h	03h	R	1 = HS_G1_ONLY
				2 = HS_G1_TO_G2
				3 = HS_G1_TO_G3
TX_PWMG0_Capability	03h	00h	R	0 = NO
				1 = YES
TX_PWMGEAR_Capability	04h	07h	R	Range from PWM_G1 to PWM_G7
TX_Amplitude_Capability	05h	03h	R	1 = SA
				2 = LA
				3 = BOTH
TX_ExternalSYNC_Capability	06h	01h	R	0 = FALSE
				1 = TRUE
TX_HS_Unterminated_LINE_Drive_Capability	07h	01h	R	0 = NO
				1 = YES
TX_LS_Terminated_LINE_Drive_Capability	08h	01h	R	0 = NO
				1 = YES
TX_Min_SLEEP_NoConfig_Time_Capability	09h	08h	R	1 to 15
TX_Min_STALL_NoConfig_Time_Capability	0Ah	80h	R	1 to 255
TX_Min_SAVE_Config_Time_Capability	0Bh	7Fh	R	1 to 250
TX_REF_CLOCK_SHARED_Capability	0Ch	01h	R	0 = NO
				1 = YES
TX_PHY_MajorMinor_Release_Capability	0Dh	30h	R	Bit[7:4]: Major version number
				Bit[3:0]: Minor version number
TX_PHY_Editorial_Release_Capability	0Eh	01h	R	Bit[7:0] = 1 to 99
TX_Hibern8Time_Capability	0Fh	01h	R/W	1 to 128
TX_Advanced_Granularity_Capability	10h	05h	R/W	Bit[2:1]: Step size
				Bit[0]: Supports fine granularity steps
TX_Advanced_Hibern8Time_Capability	11h	07h	R/W	1 to 128
TX_HS_Equalizer_Setting_Capability	12h	03h	R	Bit[1:0]

Table 8: PHY M-RX Capability Attributes

Name	ID	Value	Type	Notes	
RX_HSMODE_Capability	81h	01h	R	0 = NO	
				1 = YES	
RX_HSGEAR_Capability	82h	03h	R	1 = HS_G1_ONLY	
				2 = HS_G1_TO_G2	
				3 = HS_G1_TO_G3	
RX_PWMG0_Capability	83h	00h	R	0 = NO	
				1 = YES	
RX_PWMGEAR_Capability	84h	07h	R	Range from PWM_G1 to PWM_G7	
RX_HS_Unterminated_LINE_Drive_Capability	85h	00h	R	0 = NO	
				1 = YES	
RX_LS_Terminated_LINE_Drive_Capability	86h	01h	R	0 = NO	
				1 = YES	
RX_Min_SLEEP_NoConfig_Time_Capability	87h	0Fh	R	1–15	
RX_Min_STALL_NoConfig_Time_Capability	88h	FAh	R	1–255	
RX_Min_SAVE_Config_Time_Capability	89h	FAh	R	1–250	
RX_REF_CLOCK_SHARED_Capability	8Ah	01h	R/W	0 = NO	
				1 = YES	
RX_HS_G1_SYNC_LENGTH_Capability	8Bh	49h	R/W	Bit[7:6]: SYNC_range	FINE = 0
					COARSE = 1
				Bit[5:0]: SYNC_length	FINE = 1–15
					COARSE = 0–15
RX_HS_G1_PREPARE_LENGTH_Capability	8Ch	0Fh	R	0–15	
RX_LS_PREPARE_LENGTH_Capability	8Dh	06h	R	0–15	
RX_PWM_Burst_Closure_Length_Capability	8Eh	1Fh	R/W	0–31	
RX_Min_ActivateTime_Capability	8Fh	04h	R/W	1–9	
RX_PHY_MajorMinor_Release_Capability	90h	30h	R	Bit[7:4]: Major version number	
				Bit[3:0]: Minor version number	
RX_PHY_Editorial_Release_Capability	91h	01h	R	1–99	
RX_Hibern8Time_Capability	92h	01h	R/W	1–128	
RX_PWM_G6_G7_SYNC_LENGTH_Capability	93h	0Fh	R/W	Bit[7:6]: SYNC_range	FINE = 0
					COARSE = 1
				Bit[5:0]: SYNC_length	0–15
RX_HS_G2_SYNC_LENGTH_Capability	94h	4Ah	R/W	Bit[7:6]: SYNC_range	FINE = 0
					COARSE = 1
				Bit[5:0]: SYNC_length	FINE = 1–15
					COARSE = 0–15

Table 8: PHY M-RX Capability Attributes (Continued)

Name	ID	Value	Type	Notes	
RX_HS_G3_SYNC_LENGTH_Capability	95h	4Bh	R/W	Bit[7:6]: SYNC_range	FINE = 0
					COARSE = 1
				Bit[5:0]: SYNC_length	FINE = 1–15
					COARSE = 0–15
RX_HS_G2_PREPARE_LENGTH_Capability	96h	0Fh	R/W	Bit[3:0]: 0 to 15	
RX_HS_G3_PREPARE_LENGTH_Capability	97h	0Fh	R/W	Bit[3:0]: 0 to 15	
RX_Advanced_Granularity_Capability	98h	07h	R/W	Bit[2:1]: Step size	
				Bit[0]: Supports fine granularity steps	
RX_Advanced_Hibern8Time_Capability	99h	04h	R/W	1–128	
RX_Advanced_Min_ActivateTime_Capability	9Ah	0Bh	R/W	Bit[3:0]: 1–14	

UPIU Transaction Codes

Micron devices support the following UPIU transaction codes. For detailed information, refer to JEDEC UFS 2.1 specification.

Table 9: UPIU Transaction Codes

Initiator to Target	Transaction Code	Target to Initiator	Transaction Code
NOP OUT	00h	NOP IN	20h
COMMAND	01h	RESPONSE	21h
DATA OUT	02h	DATA IN	22h
TASK MANAGEMENT REQUEST	04h	TASK MANAGEMENT RESPONSE	24h
Reserved	11h	READY TO TRANSFER	31h
QUERY REQUEST	16h	QUERY RESPONSE	36h

Note: 1. Bit[5] of Transaction Code indicates the direction of flow and the originator of the UPIU: when bit[5] = 0, the originator is the Initiator device; when bit[5] = 1 the originator is the Target device.

UFS Descriptors

Descriptors are blocks or pages of parameters that describe something about the device. Descriptors are classified into types: Device descriptors, configuration descriptors, unit descriptors and so forth. Micron devices support the UFS descriptors defined in the following tables.

Unless otherwise stated, values for all descriptor tables are device default values. For detailed information, refer to the JEDEC UFS specification.

Table 10: N Descriptor Identification Values

DescriptorIDN[1]	Descriptor Type	Length[2]
00h	Device	40h
01h	Configuration	90h
02h	Unit	23h
	RPMB Unit[3]	23h
03h	Reserved	
04h	Interconnect	06h
05h	String	Various
	Manufacturer Name String[3]	12h
	Serial Number String[3]	12h
	OEM ID String[3]	0Eh
	Product Revision String[3]	0Ah
	Product Name String[3]	22h
06h	Reserved	
07h	Geometry	48h
08h	Power	62h
09h	Device Health[4]	25h
0Ah...FFh	Reserved	

Notes:
1. For all descriptors, DescriptorIDN offset = 01h and size = 1 byte
2. For all descriptors, Length offset = 00h and Length size = 1 byte
3. Specialized descriptor
4. Descriptor is Micron specific

Table 11: Device Descriptor

Offset	Size	Name	Value	Description	Configuration Options
00h	1	bLength	40h	Size of this descriptor	None
01h	1	bDescriptorIDN	00h	Device descriptor type identifier	None
02h	1	bDevice	00h	Device type	None
03h	1	bDeviceClass	00h	UFS device class: Mass storage	None
04h	1	bDeviceSubClass	00h	UFS device subclass: Bootable, embedded	None

Table 11: Device Descriptor (Continued)

Offset	Size	Name	Value	Description	Configuration Options
05h	1	bProtocol	00h	Protocol supported by UFS device: SCSI	None
06h	1	bNumberLU	00h	Number of logical units, not including well-known LUs	Value is calculated by the device based on bLUEnable field value in unit descriptors
07h	1	bNumberWLU	04h	Number of well known logical units	None
08h	1	bBootEnable	00h	Indicates whether the device is enabled for boot	00h: Boot feature disabled 01h: Boot feature enabled 02h–FFh: Reserved
09h	1	bDescrAccessEN	00h	Descriptor access enable indicates whether the device descriptor can be read after the partial initialization phase of the boot sequence	00h: No device descriptor access 01h: Device descriptor access 02h–FFh: Reserved
0Ah	1	bInitPowerMode	01h	Initial power mode defines the power mode after device initialization or hardware reset defines the high priority logical unit	00h: UFS-sleep mode 01h: Active mode 02h–FFh: Reserved
0Bh	1	bHighPriorityLUN	7Fh	Defines the high priority logical unit	Any value from 00h to bMaxNumberLU 7Fh: All LUN have the same priority
0Ch	1	bSecureRemovalType	00h	Defines which method is used for removing data from designated addresses	00h: Physical erase 01h: Overwrite locations with single characters then physical erase 02h: Overwrite locations with single characters, over write with character compliments, then physical erase 03h: Vendor defined mechanism 04h–FFh: Reserved
0Dh	1	bSecurityLU	01h	RPMB security logical unit supported	None
0Eh	1	bBackgroundOpsTermLat	05h	Background operations termination latency (expressed in units of 10ms) defines the maximum latency for the termination of ongoing background operations	None
0Fh	1	bInitActiveICCLevel	00h	Defines the active I_{CC} level value after power-on or reset	Any value from 00h to 0Fh 10h–FFh: Reserved
10h	2	wSpecVersion	0210h	Specification version reported in BCD format	Bits[15:8] = Major version Bits[7:4] = Minor version Bits[3:0] = Version suffix
12h	2	wManufactureDate	–	Device manufactured date reported in BCD format	None

Table 11: Device Descriptor (Continued)

Offset	Size	Name	Value	Description	Configuration Options	
14h	1	iManufactureName	00h	Index to the Manufacturer Name String; OEM ID String	None	
15h	1	iProductName	01h	Index to the Product Name String	None	
16h	1	iSerialNumber	02h	Index to the Serial Number String	None	
17h	1	iOEMID	03h	Index to the OEM ID String	None	
18h	2	wManufactureID	12Ch	Manufacturer ID as defined in JEDEC standard JEP106 "Standard Manufacturer's Identification Code"	None	
1Ah	1	bUD0BaseOffset	10h	Offset of the Unit Descriptor 0 configurable parameters within the Configuration Descriptor	None	
1Bh	1	bUDConfigPLength	10h	Total size of the configurable unit descriptor parameters	None	
1Ch	1	bDeviceRTTCap	02h	Maximum number of outstanding RTTs supported by device (minimum value is 2)	None	
1Dh	2	wPeriodicRTCUpdate	0000h	Frequency and method of real-time clock update Bit[9] = TIME_BASELINE[1] Bits[8:6] = TIME_UNIT Bits[5:0] = TIME_PERIOD[2]	Bits[15:10]: Reserved	
					Bit[9]:	0b: Time elapsed from the previous dSecondsPassed update
						1b: Absolute time elapsed from January 1st 2010 00:00
					Bits[8:6]:	000b: = Undefined
						001b = Months
						010b = Weeks
						011b = Days
						100b = Hours
						101b = Minutes
						110b–111b = Reserved
					Bits[5:0]: Time period	

Table 11: Device Descriptor (Continued)

Offset	Size	Name		Value	Description	Configuration Options
1Fh	1	bUFSFeaturesSupport		7Fh	Indicates which features are supported by the device with a value of 1 for the associated bit Bit[0]: Field firmware update (FFU) Bit[1]: Production state awareness (PSA) Bit[2]: Device life span Bit[3]: REFRESH operation Bit[4]: TOO_HIGH_TEMPERATURE Bit[5]: TOO_LOW_TEMPERATURE Bit[6]: Extended temperature Bit[7]: Reserved	None
20h	1	bFFUTimeout		0Ah	Maximum time, in seconds, that access to the device is limited or not possible through any ports associated due to execution of a WRITE BUFFER command	None
21h	1	bQueueDepth		20h	Shared queuing architecture with depth of 20h	None
22h	2	wDeviceVersion		–	This field provides the device version	None
24h	1	bNumSecureWPArea		20h	Total number of secure write protect areas supported by the device	None
25h	4	dPSAMax-DataSize	32GB	27BD55h	PSA maximum data size, expressed in units of 4KB: - Specifies the maximum amount of data that may be written during the pre-soldering phase of the PSA flow - Indicates the total amount of data for all logical units with bPSASensitive = 01h	None
			64GB	4F7AAAh		
			128GB	9EED55h		
			256GB	13DD2AAh		
29h	1	bPSAStateTimeout		12h	PSA timeout specifies maximum command timeout for a change in bPSAStatate state The formula to calculate maximum timeout value is: PSA timeout = 100µs × 2^bPSAStateTimeout (Note: value of 00h is undefined)	None
2Ah	1	iProductRevisionLevel		04h	Index to the string which contains the product revision level	None
2Bh	5	Reserved		–	Reserved	
30h	16	Reserved		–	Reserved for Unified Memory Extension specification	

Notes: 1. For host device with Real Time Clock set TIME BASELINE = 1. Otherwise use TIME BASELINE = 0.

2. If TIME_UNIT = 0, TIME_PERIOD is ignored and period between RTC update is undefined.

Table 12: Configuration Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	90h	Size of this descriptor
01h	1	bDescriptorIDN	01h	Configuration descriptor type identifier
02h	1	bConfDescContinue	00h	Indicates whether the configuration descriptor is the last in a sequence of descriptor query requests 00h: Configuration descriptor is the last in sequence so device shall perform internal configuration according to received configuration descriptor 01h: Configuration descriptor is NOT the last in sequence so device shall NOT perform internal configuration as more configuration descriptors are expected
03h	1	bBootEnable	00h	Enables to boot feature
04h	1	bDescrAccessEn	00h	Enables access to the device descriptor after the partial initialization phase of the boot sequence
05h	1	bInitPowerMode	01h	Configures the power mode after device initialization or hardware reset
06h	1	bHighPriorityLUN	7Fh	Configures the high priority logical unit
07h	1	bSecureRemovalType	00h	Configures the secure removal type
08h	1	bInitActiveICCLevel	00h	Configures the I_{CC} level in active mode after device initialization or hardware reset
09h	2	wPeriodicRTCUpdate	00h	Frequency and method of real-time clock update (see Device Descriptor)
0Bh	1	Reserved	–	Reserved
0Ch	1	bRPMBRegionEnable	00h	Configures which RPMB regions are enabled in RPMB well known logical unit
0Dh	1	bRPMBRegion1Size	00h	Configures the size of RPMB region 1 if RPMB region 1 is enabled
0Eh	1	bRPMBRegion2Size	00h	Configures the size of RPMB region 2 if RPMB region 2 is enabled
0Fh	1	bRPMBRegion3Size	00h	Configures the size of RPMB region 3 if RPMB region 3 is enabled

Table 13: Unit Descriptor

Offset	Size	Name	Value	Description	Configuration Options
00h	1	bLength	23h	Size of this descriptor	None
01h	1	bDescriptorIDN	02h	Unit descriptor type identifier	None
02h	1	bUnitIndex	00h to 1Fh	Unit index	None
03h	1	bLUEnable	00h	Logical unit enablement	00h: Logical unit enabled 01h: Logical unit disabled All other values reserved
04h	1	bBootLunID	00h	Boot LUN identifier	00h: Not bootable from LUN 01h: Boot LU A 02h: Boot LU B All other values reserved

Table 13: Unit Descriptor (Continued)

Offset	Size	Name	Value	Description	Configuration Options
05h	1	BLUWriteProtect	00h	Logical Unit write protection setting	00h: No write protection 01h: Power-on write protection (fPowerOnWPEn =1) 02h: Permanent write protection (fPermanentWPEn =1) All other values reserved
06h	1	bLUQueueDepth	00h	Logical Unit available queue depth available in this LU Value of 0 indicates device autonomous service of command tasks	None
07h	1	bPSASensitive	01h	LU sensitivity to soldering (1b = sensitive, 0b = Not sensitive, all others reserved)	None[1]
08h	1	bMemoryType	00h	Defines Logical Unit memory type	00h: Normal (default) memory 01h: System code memory 02h: Non-Persistent memory type 03h–06h: Enhanced memory type 1–type 4 All other values reserved
09h	1	bDataReliability	00h	Defines the device data protection behavior when a power failure occurs during a write operation to the logical unit	00h: LU data is not protected and susceptible to data loss 01h: LU data is protected All other values reserved
0Ah	1	bLogicalBlockSize	0Ch	Exponent used to determine the size of addressable logical blocks Minimum value is 0Ch, corresponding to 4KB	Logical block size = $2^{bLogicalBlockSize}$
0Bh	8	qLogicalBlockCount	00h	Total number of addressable logical blocks in the logical unit	Configured by setting Configuration Descriptor "dNumAllocUnits" parameter
13h	4	dEraseBlockSize	00h	Number of logical blocks within an erase block[1]	None
17h	1	bProvisioningType	00h	Provisioning type	00h: Thin provisioning disabled (default) 02h: Thin provisioning enabled; TPRZ = 0 03h: Thin provisioning enabled; TPRZ = 1 All other values reserved
18h	8	qPhyMemResourceCount	00h	Total physical memory resource available in the logical unit	None

Table 13: Unit Descriptor (Continued)

Offset	Size	Name	Value	Description	Configuration Options
20h	2	wContextCapabilities	00h	Logical Unit context capabilities include: MaxContextID is the maximum amount of contexts simultaneously supported by the LU - Boundary: Sum of all MaxContextID ≤ bMaxContexIDNumber) LARGE_UNIT_MAX_MULTIPLIER_M1 is a "read-only" field whose value is one less than the highest multiplier that can be configured for Large Unit contexts - Boundaries: 1 ≤ multiplier ≤ (LARGE_UNIT_MAX_MULTIPLIER_M1 + 1)	Bits [3:0]: MaxContextID Bits [6:4]: LARGE_UNIT_MAX_MULTIPLIER_M1 All other values reserved
22h	1	bLargeUnitGranularity_M1	00h	Granularity of the large unit, minus 1	None

Note: 1. Value is updated automatically by the device after device configuration

Table 14: RPMB Unit Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	23h	Size of this descriptor
01h	1	bDescriptorIDN	02h	Unit descriptor type identifier
02h	1	bUnitIndex	C4h	Unit index
03h	1	bLUEnable	01h	Logical unit enabled
04h	1	bBootLunID	00h	Non-bootable LUN ID
05h	1	bLUWriteProtect	00h	Logical unit not write protected
06h	1	bLUQueueDepth	00h	RPMB LU queue is not available (shared queuing is used)
07h	1	bPSASensitive	01h	LU is sensitive to soldering
08h	1	bMemoryType	0Fh	RPMB memory type
09h	1	bRPMBRegionEnable	00h	RPMB region 0 enabled independent of bit[0] Bit[0]: "Don't Care" Bit[1]: RPMB region 1 is enabled when Bit1 = 1 Bit[2]: RPMB region 2 is enabled when Bit2 = 1 Bit[3]: RPMB region 3 is enabled when Bit3 = 1 All other bits reserved
0Ah	1	bLogicalBlockSize	08h	Size of addressable logical blocks is 256 bytes Calculation of logical block size = 2^(bLogicalBlockSize)
0Bh	8	qLogicalBlockCount	10000h	Logical block count
13h	4	dEraseBlockSize	00h	Erase bock size
17h	1	bProvisioningType	00h	Provisioning type

Table 14: RPMB Unit Descriptor (Continued)

Offset	Size	Name	Value	Description
18h	8	qPhyMemResourceCount	10000h	Physical memory resource count
20h	3	Reserved	00h	Reserved

Table 15: Interconnect Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	06h	Size of this descriptor
01h	1	bDescriptorIDN	04h	Interconnect descriptor type identifier
02h	2	bcdUniproVersion	0160h	MIPI UniPro version number in BCD format[1]
04h	2	bcdMphyVersion	0300h	MIPI M-PHY version number in BCD format[1]

Note: 1. BCD format example: Value 0321h = version 3.21

Table 16: String Descriptors

String Descriptor Characteristics			String Descriptor Values			
Offset	Size	Name[1]	Manufacturer Name	Serial Number[2]	OEM ID	Product Revision[3]
00h	1	bLength	12h	12h	0Eh	0Ah
01h	1	bDescriptorIDN	05h	05h	05h	05h
02h	2	UC[0]	004Dh	UID[0]	004Dh	*
04h	2	UC[1]	0049h	UID[1]	0049h	*
06h	2	UC[2]	0043h	*	0043h	*
08h	2	UC[3]	0052h	*	0052h	*
0Ah	2	UC[4]	004Fh	*	004Fh	
0Ch	2	UC[5]	004Eh	*	004Eh	
0Eh	2	UC[6]	0020h	*		
10h	2	UC[7]	0020h	*		

Notes: 1. UC = Unicode string character
2. Each device is created with a unique identification number (UID) provided in UC[0] and UC[1] fields; UC[2] to UC[7] field values are "Don't Care"
3. Product revision descriptor may differ between product designs

Table 17: Product Name String Descriptor

Descriptor Characteristics			Product Name Values			
Offset	Size	Name[1]	32GB	64GB	128GB	256GB
00h	1	bLength	22h	22h	22h	22h
01h	1	bDescriptorIDN	05h	05h	05h	05h
02h	2	UC[0]	004Dh	004Dh	004Dh	004Dh
04h	2	UC[1]	0054h	0054h	0054h	0054h

Table 17: Product Name String Descriptor (Continued)

Descriptor Characteristics			Product Name Values			
Offset	Size	Name[1]	32GB	64GB	128GB	256GB
06h	2	UC[2]	0030h	0030h	0031h	0032h
08h	2	UC[3]	0033h	0036h	0032h	0035h
0Ah	2	UC[4]	0032h	0034h	0038h	0036h
0Ch	2	UC[5]	0047h	0047h	0047h	0047h
0Eh	2	UC[6]	0041h	0041h	0041h	0041h
10h	2	UC[7]	0053h	0053h	0053h	0053h
12h	2	UC[8]	0041h	0041h	0041h	0041h
14h	2	UC[9]	004Fh	004Fh	004Fh	004Fh
16h	2	UC[10]	0031h	0032h	0034h	0038h
18h	2	UC[11]	0055h	0055h	0055h	0055h
1Ah	2	UC[12]	0032h	0032h	0032h	0032h
1Ch	2	UC[13]	0031h	0031h	0031h	0031h
1Eh	2	UC[14]	0020h	0020h	0020h	0020h
20h	2	UC[15]	0020h	0020h	0020h	0020h

Note: 1. UC = Unicode string character

Table 18: Geometry Descriptor

Offset	Size	Name		Value	Description
00h	1	bLength		48h	Size of this descriptor
01h	1	bDescriptorIDN		07h	Geometry descriptor type identifier
02h	1	bMediaTechnology		00h	Reserved
03h	1	Reserved		00h	Reserved
04h	8	qTotalRawDeviceCapacity	32GB	3B9C000h	Expressed in units of 512 bytes, total memory quantity available to the user to configure the device logical units (RPMB excluded)
			64GB	7738000h	
			128GB	EE64000h	
			256GB	1DCBC000h	
0Ch	1	bMaxNumberLU		01h	Max number of logical unit supported by the UFS device 01h: 32 logical units
1Dh	4	dSegmentSize		2000h	Segment size expressed in unit of 512 bytes
11h	1	bAllocationUnitSize		01h	Allocation unit size expressed in number of segments Each logical unit can be allocated as a multiple of allocation units
12h	1	bMinAddrBlockSize		08h	Min addressable block size expressed in units of 512 bytes Minimum value 08h corresponds to 4KB
13h	1	bOptimalReadBlockSize		40h	Optional parameter expressed in unit of 512 bytes Value of 00h = Not available

Table 18: Geometry Descriptor (Continued)

Offset	Size	Name	Value	Description
14h	1	bOptimalWriteBlock-Size	40h	Value expressed in unit of 512 bytes
15h	1	bMaxInBufferSize	40h	Max data-in buffer size expressed in unit of 512 bytes Minimum value 08h corresponds to 4KB
16h	1	bMaxOutBufferSize	40h	Max data-out buffer size expressed in unit of 512 bytes Minimum value 08h corresponds to 4KB
17h	1	bRPMB_ReadWriteSize	20h	Maximum number of RPMB frames (256-byte of data) allowed in security protocol in and security protocol out (for example, associated with a single command UPIU). If the data to be transferred is larger than bRPMB_Read- Write-Size x 256 bytes, the host will transfer it using multiple SECURITY PROTOCOL IN/OUT commands.
18h	1	bDynamicCapacityResourcePolicy	01h	Dynamic capacity resource policy specifies the device spare blocks resource management policy 00h: Spare blocks resource management policy is per logical unit. The host should release amount of logical blocks from each logical unit as asked by the device. 01h: Spare blocks resource management policy is per memory type. The host may deallocate the required amount of logical blocks from any logical units with the same bMemoryType.
19h	1	bDataOrdering	00h	Support for out-of-order data transfer 00h: Out-of-order data transfer not supported; in-order data transfer is required 01h: Out-of-order data transfer is supported All others bit reserved
1Ah	1	bMaxContexIDNumber	20h	Max available number of contexts supported by the device Minimum number of supported contexts shall be 5
1Bh	1	bSysDataTagUnitSize	00h	bSysDataTagUnitSize provides system data tag unit size Tag unit size = $2^{bSysDataTagUnitSize}$ × bMinAddrBlockSize × 512 bytes
1Ch	1	bSysDataTagResSize	06h	Maximum storage area size in bytes allocated by the device to handle system data by the tagging mechanism: Valid range from 0 to 6
1Dh	1	bSupportedSecRTypes	09h	Bit map representing supported secure removal types[1] Bit[0]: Data removed by an erase of the physical memory Bit[1]: Data removed by overwriting the addressed locations with a single character followed by an erase Bit[2]: Data removed by overwriting the addressed locations with a character, its complement, then a random character Bit[3]: Data removed using a vendor defined mechanism All other bits reserved

Table 18: Geometry Descriptor (Continued)

Offset	Size	Name		Value	Description
1Eh	2	wSupportedMemory-Types		8009h	Bit map which represents the supported memory types[1] Bit0]: normal memory type (always = 1 for UFS) Bit[1]: System code memory type Bit[2]: Non-persistent memory type Bit[3]–bit[4]: Enhanced memory type 1–type 4 Bit[7]–bit[14]: Reserved Bit[15]: RPMB memory type (always = 1 for UFS)
20h	4	dSystemCodeMaxNAl-locU		0h	Maximum available quantity of system code memory type for the entire device expressed in number of allocation units
24h	2	wSystemCodeCapAdj-Fac[2]		0h	System code capacity adjustment factor
26h	4	dNonPersistMaxNAllo-cU		0h	Maximum available quantity of non-persistent memory type for the entire device expressed in number of alloca-tion units
2Ah	2	wNonPersistCapAdj-Fac[2]		0h	Non-persistent capacity adjustment factor
2Ch	4	dEn-hanced1Max-NAllocU	32GB	1DCEh	Maximum available quantity of enhanced memory type 1 for the entire device expressed in number of allocation units
			64GB	3B9Ch	
			128GB	7732h	
			256GB	EE5Eh	
30h	2	wEnhanced1CapA-djFac[2]		0300h	Capacity adjustment factor for the enhanced memory type 1
32h	4	dEnhanced2MaxNAllo-cU		00h	Maximum available quantity of enhanced memory type 2 for the entire device expressed in number of Allocation Units
36h	2	wEnhanced2CapA-djFac[2]		00h	Capacity adjustment factor for the enhanced memory type 2
38h	4	dEnhanced3MaxNAllo-cU		00h	Maximum available quantity of enhanced memory type 3 for the entire device expressed in number of Allocation Units
3Ch	2	wEnhanced3CapA-djFac[2]		00h	Capacity adjustment factor for the enhanced memory type 3
3Eh	4	dEnhanced4MaxNAllo-cU		00h	Maximum available quantity of enhanced memory type 4 for the entire device expressed in number of Allocation Units
42h	2	wEnhanced4CapA-djFac[2]		00h	Capacity adjustment factor for the enhanced memory type 4

Table 18: Geometry Descriptor (Continued)

Offset	Size	Name	Value	Description
44h	4	dOptimalLogicalBlock-Size	00h	The optimal logical block size for each memory type can be calculated from the related dOptimalLogicalBlockSize field as follows: Optimal size= $2^{dOptimalLogicalBlockSize}$ x bMinAddrBlockSize x 512 bytes dOptimalLogicalBlockSize bit definitions: Bit[3:0]: Normal memory type Bit[7:4]: System code memory type Bit[11:8]: Non-persistent memory type Bit[15:12]: Enhanced memory type 1 Bit[19:16]: Enhanced memory type 2 Bit[23:20]: Enhanced memory type 3 Bit[27:24]: Enhanced memory type 4 All other bits reserved

Notes:
1. A bit value of 1 indicates that the corresponding descriptor type is supported (for example, memory type or secure removal type)
2. Capacity Adjustment Factors are integer value of the ratio between the capacity obtained with normal memory type and the capacity obtained with a specific memory type for the same amount of allocation units. CapAdjFactor for a specific memory type is calculated as follows:

   w*MEMORYTYPE*CapAdjFactor = INTEGER(256 × CapacityAdjFactor)

   where: CapacityAdjFactor = $Capacity_{NormalMem}/Capacity_{MEMORYTYPE}$

   Note that if normal memory type is used for the specific *MEMORYTYPE*, the Capacity Adjustment Factor value 1

Table 19: Power Parameters Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	62h	Size of this descriptor
01h	1	bDescriptorIDN	08h	Power parameters descriptor type identifier
02h	2	wActiveICCLevelsVCC[0]	82BCh	Maximum V_{CC} current value for bActiveICCLevel = 0
04h	2	wActiveICCLevelsVCC[1]	82BCh	Maximum V_{CC} current value for bActiveICCLevel = 1
...	...	...	...	...
20h	2	wActiveICCLevelsVCC[15]	82BCh	Maximum V_{CC} current value for bActiveICCLevel = 15
22h	2	wActiveICCLevelsVCCQ[0]	0h	Maximum V_{CCQ} current value for bActiveICCLevel = 0
24h	2	wActiveICCLevelsVCCQ[1]	0h	Maximum V_{CCQ} current value for bActiveICCLevel = 1
...	...	...	...	...
40h	2	wActiveICCLevelsVCCQ[15]	0h	Maximum V_{CCQ} current value for bActiveICCLevel = 15
42h	2	wActiveICCLevelsVCCQ2[0]	82BCh	Maximum V_{CCQ2} current value for bActiveICCLevel = 0
44h	2	wActiveICCLevelsVCCQ2[1]	82BCh	Maximum V_{CCQ2} current value for bActiveICCLevel = 1
...	...	...	...	...
60h	2	wActiveICCLevelsVCCQ2[15]	82BCh	Maximum V_{CCQ2} current value for bActiveICCLevel = 15

Table 20: Device Health Descriptor

Offset	Size	Name	Value	Description
00h	1	bLength	25h	Size of this descriptor
01h	1	bDescriptorIDN	09h	Device health descriptor type identifier
02h	1	bPreEOLInfo	01h	Pre-"end-of-life" information provides indication about device life time reflected by average reserved blocks (value 01h = Normal)
03h	1	bDeviceLifeTimeEstA	01h	This field provides an indication of the device life time based on the amount of performed PROGRAM/ERASE cycles. The calculation method is vendor specific and referred as method A. 01h: 0%–10% device life time used
04h	1	bDeviceLifeTimeEstB	01h	This field provides an indication of the device life time based on the amount of performed PROGRAM/ERASE cycles. The calculation method is vendor specific and referred as method B. 00h: Information not available
05h	32	VendorPropInfo	00h	Reserved for vendor proprietary health report
25h	4	dRefreshTotalCount	00h	Total refresh count indicates the number of completed refresh cycles for the entire device. Incremented by 1 when dRefreshProgress reaches 100000 (100.000%).
29h	4	dRefreshProgress	00h	Refresh progress indicates refresh progress in percentage (0.000%~100.000%) Example: dRefreshProgress value of 2000 (dec) = 2.000% When this value reaches 100000 (100.000%): 1. Device stops refreshing even if it did not complete the number of units specified by bRefreshUnit 2. dRefreshProgress value resets '0' 3. dRefreshTotalCount increments by 1 When bRefreshMethod = 02h (Manual-selective), even though some of physical blocks are not refreshed by device choice, dRefreshProgress should be incremented just as much as bRefreshUnit.

Note: 1. Micron offers proprietary solution for additional health status information.

UFS Flags, Attributes, and Commands

A flag is a single boolean value that represents 0 or 1 type of value. Flags are useful to enable or disable certain functions, modes, or states with the device.

Table 21: Flags

IDN	Name	Type	Default Value	Description
00h	Reserved	–	–	Reserved
01h	fDeviceInit	Read/Set only	00h	Device initialization: 0b: Device initialization completed or not started yet 1b: Device initialization in progress

Table 21: Flags (Continued)

IDN	Name	Type	Default Value	Description
02h	fPermanentWPEn	Read/Write once	00h	Permanent write protection enable: 00h: Permanent write protection disabled 01h: Permanent write protection enabled
03h	fPowerOnWPEn	Read/Power on reset	00h	Power-on write protection enable: 00h: Power-on write protection disabled 01h: Power-on write protection enabled
04h	FBackgroundOpsEn	Read/Volatile	01h	Background operations enable: 00h: Device is not permitted to run background operations 01h: Device is permitted to run background operations
05h	fDeviceLifeSpan-ModeEn	Read/Volatile	00h	Device life span mode: 0b: Device life span mode is disabled 1b: Device life span mode is enabled
06h	fPurgeEnable	Write only/Volatile	00h	PURGE enable: 00h: PURGE operation is disabled 01h: PURGE operation is enabled
07h	fRefreshEnable	Write only/Volatile	00h	Refresh enable 0b: REFRESH operation is disabled. 1b: REFRESH operation is enabled. This flag shall only be set when the command queue of all logical units are empty and the bRefreshStatus is 00h (idle). fRefreshEnable is automatically cleared by the UFS device when the operation completes or an error condition occurs. fRefreshEnable can be cleared by the host to interrupt an ongoing REFRESH operation
08h	fPhyResourceRemoval	Read/Persistent	00h	Physical resource removal: The host sets this flag to 1 to indicate that the dynamic capacity operation commences upon device EndPointReset or hardware reset. The device resets this flag to 0 after completion of dynamic capacity operation. The host cannot reset this flag.
09h	fBusyRTC	Read only	00h	Busy real-time clock: 00h: Device is not executing internal operation related to RTC 01h: Device is executing internal operation related to RTC
0Ah	Reserved	–	–	Reserved for unified memory extension standard.

Table 21: Flags (Continued)

IDN	Name	Type	Default Value	Description
0Bh	fPermanentlyDisableF-WUpdate	Read/Write once	00h	Permanently disable firmware update: 00h: The UFS device firmware may be modified. 01h: The UFS device permanently disallows future firmware updates to the UFS device.
0Ch	Reserved	–	–	Reserved for unified memory extension standard.
0Dh	Reserved	–	–	Reserved for unified memory extension standard.

All the flags reported in the table are device level flags. They are addressed setting INDEX = 00h and SELECTOR = 00h.

An attribute is a parameter that represents a specific range of numeric values that can be written or read. Attribute size can be from 1-bit to 32-bit. Attributes of the same type can be organized in arrays, each element of them identified by an index.

Table 22: Attributes

IDN	Name	Type	Size (Byte)	Default Value	Description
00h	bBootLunEN	Read/Persistent	1	00h	Boot LUN enable: 00h: Boot disabled 01h: Enabled boot from boot LU A 02h: Enabled boot from boot LU B All others: Reserved
01h	Reserved	–	–	–	Reserved
02h	bCurrentPowerMode	Read only	1	11h	Current power mode: 00h: Idle mode 10h: Pre-active mode 11h: Active mode 20h: Pre-sleep mode 22h: UFS-sleep mode 30h: Pre-power down mode 33h: UFS power-down mode Others: Reserved
03h	bActiveICCLevel	Read/Volatile	1	00h	Active I_{CC} level: bActiveICCLevel defines the maximum current consumption allowed during active mode. 00h: Lowest active I_{CC} level 0Fh: Highest active I_{CC} level Others: Reserved
04h	bOutOfOrderDataEn	Read/Write once	1	00h	Out-of-order data transfer enable: 00h: Out-of-order data transfer is disabled 01h: Out-of-order data transfer is enabled Others: Reserved

Table 22: Attributes (Continued)

IDN	Name	Type	Size (Byte)	Default Value	Description
05h	bBackgroundOpStatus	Read only	1	00h	Background operations status device health status for background operation: 00h: Not required 01h: Required, not critical 02h: Required, performance impact 03h: Critical Others: Reserved
06h	bPurgeStatus	Read only	1	00h	PURGE operation status: 00h: Idle (PURGE operation disabled) 01h: PURGE operation in progress 02h: PURGE operation stopped prematurely 03h: PURGE operation completed successfully 04h: PURGE operation failed due to logical unit queue not empty 05h: PURGE operation general failure Others: Reserved
07h	bMaxDataInSize	Read/Persistent	1	40h	Maximum data in size
08h	bMaxDataOutSize	Read/Persistent	1	40h	Maximum data out size
09h	dDynCapNeeded	Read only	4	00h	Dynamic capacity needed
0Ah	bRefClkFreq	Read/Persistent	1	01h	Reference clock frequency value: 00h: 19.2 MHz 01h: 26 MHz 02h: 38.4 MHz 03h: 52 MHz Others: Reserved
0Bh	bConfigDescrLock	Read/Write once	1	00h	Configuration descriptor lock: 00h: Configuration descriptor not locked 01h: Configuration descriptor locked Others: Reserved
0Ch	bMaxNumOfRTT	Read/Persistent	1	02h	Maximum current number of outstanding RTTs in device that is allowed.
0Dh	wExceptionEventControl	Read/Volatile	2	00h	Exception event control: Bit 0: DYNCAP_EVENT_EN Bit 1: SYSPOOL_EVENT_EN Bit 2: URGENT_BKOPS_EN Bit 3–15: Reserved
0Eh	wExceptionEventStatus	Read only	2	00h	Bit 0: DYNCAP_NEEDED Bit 1: SYSPOOL_EXHAUSTED Bit 2: URGENT_BKOPS Bit 3–15: Reserved
0Fh	dSecondsPassed	Write only	4	00h	Bits[31:0]: Seconds passed from TIME BASELINE

Table 22: Attributes (Continued)

IDN	Name	Type	Size (Byte)	Default Value	Description
10h	wContextConf	Read/Volatile	2	00h	INDEX specifies the LU number. SELECTOR specifies the context ID within the LU. Valid values are 01h–Fh.
11h	Obsolete	–	–	–	–
12h	Reserved	–	–	–	Reserved for Unified Memory Extension standard.
13h	Reserved	–	–	–	Reserved for Unified Memory Extension standard.
14h	bDeviceFFUStatus	Read only	1	00h	Device FFU status: 00h: No information 01h: Successful microcode update 02h: Microcode corruption error 03h: Internal error 04h: Microcode version mismatch 05h–FEh: Reserved FFh: General error
15h	bPSAState	Read/Persistent	1	00h	00h: Off. PSA feature is off. 01h: Pre-soldering. PSA feature is on, device is in the pre-soldering state. 02h: Loading complete. PSA feature is on. The host will set to this value after the host finished writing data during pre-soldering state. 03h: Soldered. PSA feature is no longer available. Set by the device to indicate it is in post-soldering state. This attribute unchangeable after it is in soldered state.
16h	dPSADataSize	Read/Persistent	4	00h	The amount of data that the host plans to load to all logical units with bPSASensitive set to 1.
18h	bDeviceCaseRoughTemperaure	Read only	1	00h	Device's rough package case surface temperature. This value shall be valid when (TOO_HIGH_TEMPERATURE is supported and TOO_HIGH_TEMP_EN is enabled) or (TOO_LOW_TEMPERATURE is supported and TOO_LOW_TEMP_EN is enabled). 0: Unknown temperature 1~250: (this value - 80) degrees in Celsius (that is, –79°C~170°C) Others: Reserved

Table 22: Attributes (Continued)

IDN	Name	Type	Size (Byte)	Default Value	Description
19h	bDeviceTooHighTemp-Boundar	Read only	1	BCh	High temperature boundary from which TOO_HIGH_TEMP in wExceptionEventStatus is turned on. 0: Unknown 100~250: (this value - 80) degrees in Celsius (that is, 20°C~170°C) Others: Reserved
1Ah	bDeviceTooLowTemp-Boundary	Read only	1	2Bh	Low temperature boundary from which TOO_LOW_TEMP in wExceptionEventStatus is turned on. 0: Unknown 1~80: (this value - 80) degrees in Celsius (that is, –79°C~0°C) Others: Reserved
1Bh	Reserved	–	–	–	–
…	Reserved	–	–	–	–
2Bh	Reserved	–	–	–	–
2Ch	bRefreshStatus	Read only	1	00h	REFRESH operation status: 00h: Idle (REFRESH operation disabled) 01h: REFRESH operation in progress 02h: REFRESH operation stopped prematurely 03h: REFRESH operation completed successfully 04h: REFRESH operation failed due to logical unit queue not empty 05h: REFRESH operation general failure Others: Reserved When the bRefreshStatus is equal to the values 02h, 03h, 04h, or 05h, the bRefreshStatus is automatically cleared to 00h (idle) the first time that it is read.
2Dh	bRefreshFreq	Read/Persistent	1	00h	Refresh frequency: Host should make sure that dRefreshTotalCount will be incremented on this frequency. 00h: Not defined 01h: 1 month 02h: 2 month … FFh: 255 month.

Table 22: Attributes (Continued)

IDN	Name	Type	Size (Byte)	Default Value	Description
2Eh	bRefreshUnit	Read/Persistent	1	00h	REFRESH operation unit: This attribute may be set to adjust the minimum physical block numbers to be refreshed upon a single request (for example, fRefreshEnable set to 1) 00h: Minimum refresh capability of device 01h: 100.000% (for example, entire device) Others: Reserved
2Fh	bRefreshMethod	Read/REFRESH Persistent	1	00h	Refresh method: This parameter specifies the REFRESH operation method. 00h : Not defined 01h: Manual-force. The device is obliged to refresh the amount of physical blocks as requested by the host, regardless whether these blocks need refresh or not. The REFRESH command refreshes the amount of physical blocks given in bRefreshUnit. Refresh starts at the next physical block from where it stopped (or the first block if refresh was never triggered before). 02h: Manual-selective. The REFRESH command refreshes the amount of physical blocks given in bRefreshUnit. Refresh starts at the next physical block from where it stopped (or the first block if refresh was never triggered before). The device only refreshes the blocks that it considers to be in need of refresh. Regardless of the actually refreshed blocks, dRefreshProgress is increased by bRefreshUnit once the REFRESH command is completed. Others: Reserved .

Notes: 1. dDynCapNeeded and wContextConf are arrays of attributes.
2. Default value means attribute's value after device manufacturing.

Table 23: SCSI Commands

Command Name	Opcode	Command Name	Opcode
FORMAT UNIT	04h	SECURITY PROTOCOL IN	A2h
INQUIRY	12h	SECURITY PROTOCOL OUT	B5h
MODE SELECT (10)	55h	SEND DIAGNOSTIC	1Dh
MODE SENSE (10)	5Ah	START STOP UNIT	1Bh
PREFETCH (10)	34h	SYNCHRONIZE CACHE (10)	35h

Table 23: SCSI Commands (Continued)

Command Name	Opcode	Command Name	Opcode
PREFETCH (16)	90h	SYNCHRONIZE CACHE (16)	91h
READ (6)	08h	TEST UNIT READY	00h
READ (10)	28h	UNMAP	42h
READ (16)	88h	VERIFY (10)	2Fh
READ BUFFER	3Ch	WRITE (6)	0Ah
READ CAPACITY (10)	25h	WRITE (10)	2Ah
READ CAPACITY(16)	9Eh	WRITE (16)	8Ah
REPORT LUNS	A0h	WRITE BUFFER	3Bh
REQUEST SENSE	03h	–	–

UFS Supported Pages

Micron devices support the following UFS mode pages. For detailed information, refer to the JEDEC UFS specification.

Table 24: UFS Supported Pages

Page Name	Page Code	Subpage Code	Description
Control	0Ah	00h	Return control mode page
Read-write error recovery	01h	00h	Return read-write error recovery mode page
Caching	08h	00h	Return caching mode page
All pages	3Fh	00h	Return all mode pages (not including subpages)
All subpages	3Fh	FFh	Return all mode pages and subpages

Table 25: Control Mode Page

Offset	Bit	Field	Default Value	Description
00h	5:0	PAGE CODE	0Ah	Indicates the format and parameters for particular mode page.
00h	6	SPF	0h	Indicates SUBPAGE format.
00h	7	PS	01h	Indicates the page parameters can be saved.
01h	7:0	PAGE LENGTH	0Ah	Indicates the size in bytes of the following mode page parameters.
02h	0	RLEC	0h	Report log exception condition. Setting this bit to 0 specifies that the device server shall not report log exception conditions.
02h	1	GLTSD	0h	Global logging target save disable (GLTSD): Setting this bit to 0 specifies that the logical unit implicitly saves, at vendor specific intervals, each log parameter in which the TSD bit is set to 0.
02h	2	D_SENSE	0h	A descriptor format sense data (D_SENSE) bit set to 0 specifies that the device server shall return fixed format sense data when returning sense data in the same I_T_L_Q nexus transaction as the status.
02h	3	DPICZ	0h	A disable protection information check if protect field is 0 (DPICZ) bit set to 0 indicates that checking of protection information bytes is enabled.
02h	4	TMF_ONLY	0h	The allow task management functions only (TMF_ONLY) bit set to 0 specifies that the device server shall process commands with the auto contingent allegiance (ACA) task attribute received on the faulted I_T nexus when an ACA condition has been established.
02h	7:5	TST	0h	Indicates task set type (TST).
03h	0	Obsolete	0h	Not available

Table 25: Control Mode Page (Continued)

Offset	Bit	Field	Default Value	Description
03h	2:1	QERR	0h	The queue error management (QERR) field specifies how the device server shall handle other commands when one command is terminated with check condition status. If an ACA condition is established, the affected commands in the task set shall resume after the ACA condition is cleared. Otherwise, all commands other than the command that received the check condition status shall be processed as if no error occurred.
03h	3	NUAR	0h	No unit attention on release (NUAR) bit set to 0 specifies that the device server shall establish a unit attention condition.
03h	7:4	QUEUE ALGORITHM MODIFIER	01h	A value of 1 in this field specifies that the device server may reorder the processing sequence of commands having the SIMPLE task attribute in any manner.
04h	2:0	Obsolete	0h	Not available
04h	3	SWP	0h	A software write protect (SWP) bit (user configurable)
04h	5:4	UA_INTLCK_CTRL	0h	The unit attention interlocks control (UA_INTLCK_CTRL) field set to 00b specifies that the logical unit shall clear any unit attention condition reported in the same I_T_L_Q nexus transaction as a check condition status and shall not establish a unit attention condition when a command is completed with busy, task set full, or reservation conflict status.
04h	6	RAC	0h	A report a check (RAC) bit set to 0 specifies that the device server may return busy status regardless of the length of time the reason for returning busy status may persist.
04h	7	VS	0h	Not available
05h	2:0	AUTOLOAD MODE	0h	This field specifies the action to be taken by a removable medium device server when a medium is inserted. Setting it to 0 means that medium shall be loaded for full access.
05h	3	Reserved	–	–
05h	4	RWWP	0h	A reject write without protection (RWWP) bit set to 0 specifies that WRITE commands without protection information shall be processed.
05h	5	ATMPE	0h	An application tag mode page enabled (ATMPE) bit set to 0 specifies that the application tag mode page is disabled and the contents of logical block application tags are not defined by this standard.
05h	6	TAS	0h	A task aborted status (TAS) bit set to 0 specifies that aborted commands shall be terminated by the device server without any response to the application client.
05h	7	ATO	0h	An application tag owner (ATO) bit set to 0 specifies that the device server may modify the contents of the LOGICAL BLOCK APPLICATION TAG field and, depending on the protection type, may modify the contents of the LOGICAL BLOCK REFERENCE TAG field.
06h	15:0	Obsolete	0h	Not available

Table 25: Control Mode Page (Continued)

Offset	Bit	Field	Default Value	Description
08h	15:0	BUSY TIMEOUT PERIOD	01h	Busy timeout period: 0001h = 100ms
0Ah	15:0	EXTENDED SELF-TEST COMPLETION TIME	0h	This field contains advisory data that is the time in seconds that the device server requires to complete an extended self-test when the device server is not interrupted by subsequent commands and no errors occur during processing of the self-test.

Note: 1. Some fields are user configurable.

Table 26: Read – Write Error Recovery Mode Page

Offset	Bit	Field	Default Value	Description
00h	5:0	PAGE CODE	01h	Indicates the format and parameters for particular mode page.
00h	6	SPF	0h	Indicates SUBPAGE format.
00h	7	PS	01h	Indicates the page parameters can be saved.
01h	7:0	PAGE LENGTH	0Ah	Indicates the size in bytes of the following mode page parameters.
02h	0	DCR	0h	A disable correction (DCR) bit set to 0 allows the use of additional information (for example, ECC bytes) for data error recovery. If the EER bit is set to 1, the DCR bit shall be set to 0.
02h	1	DTE	0h	A data terminate on error (DTE) bit set to 0 specifies that the device server shall not terminate the data-in or data-out buffer transfer of a command performing a READ or WRITE operation upon detection of a recovered error.
02h	2	PER	0h	A post error (PER) bit set to 0 specifies that if a recovered read error occurs during a command performing a READ or WRITE operation, then the device server shall perform error recovery procedures within the limits established by the error recovery parameters and only terminate the command with check condition status if the error becomes uncorrectable based on the established limits. If the DTE bit is set to 1, then the PER bit shall be set to 1.
02h	3	EER	0h	An enable early recovery (EER) bit set to 0 specifies that the device server shall use an error recovery procedure that minimizes the risk of error mis-detection or mis-correction.
02h	4	RC	0h	A read continuous (RC) bit set to 0 specifies that ERROR RECOVERY operations that cause delays during the data transfer are acceptable. Data shall not be fabricated.
02h	5	TB	0h	A transfer block (TB) bit set to 0 specifies that if an unrecovered read error occurs during a READ operation, then the device server shall not transfer any data for the logical block to the data-in buffer.

Table 26: Read – Write Error Recovery Mode Page (Continued)

Offset	Bit	Field	Default Value	Description
02h	6	ARRE	0h	An automatic read reassignment enabled (ARRE) bit set to 0 specifies that the device server shall not perform automatic reassignment of defective logical blocks during READ operations.
02h	7	AWRE	01h	An automatic write reassignment enabled (AWRE) bit set to 1 specifies that the device server shall enable automatic reassignment of defective logical blocks during WRITE operations.
03h	7:0	READ RETRY COUNT	01h	This field (user configurable) specifies the number of times that the device server shall attempt its recovery algorithm during READ operations.
04h	7:0	Obsolete	0h	Not available
05h	7:0	Obsolete	0h	Not available
06h	7:0	Obsolete	0h	Not available
07h	1:0	Restricted for MMC-6	0h	Not available
07h	6:2	Reserved	–	–
07h	7	TPERE	0h	Not available
08h	7:0	WRITE RETRY COUNT	00h	This field (user configurable) specifies the number of times that the device server shall attempt its recovery algorithm during WRITE operations.
09h	7:0	Reserved	–	–
0Ah	15:0	RECOVERY TIME LIMIT	4B0h	This field (user configurable) specifies in milliseconds the maximum time duration that the device server shall use for data error recovery procedures. When both a retry count and a recovery time limit are specified, the field that specifies the recovery action of least duration shall have priority.

Table 27: Caching Mode Page

Offset	Bit	Field	Default Value	Description
00h	5:0	PAGE CODE	08h	Indicates the format and parameters for particular mode page.
00h	6	SPF	0h	Indicates SUBPAGE format.
00h	7	PS	01h	Indicates the page parameters can be saved.
01h	7:0	PAGE LENGTH	12h	Indicates the size in bytes of the following mode page parameters.
02h	0	RCD	0h	A read cache disable (RCD) bit (user configurable) set to 0 specifies that the device server may return data requested by a READ command by accessing either the cache or medium. A RCD bit set to 1 specifies that the device server shall transfer all of the data requested by a READ command from the medium (for example, data shall not be transferred from the cache).

Table 27: Caching Mode Page (Continued)

Offset	Bit	Field	Default Value	Description
02h	1	MF	0h	A multiplication factor (MF) bit set to 0 specifies that the device server shall interpret the MINIMUM PREFETCH field and the MAXIMUM PREFETCH field in terms of the number of logical blocks for each of the respective types of prefetch.
02h	2	WCE	01h	A write back cache enable (WCE) bit (user configurable) set to 0 specifies that the device server shall complete a WRITE command with good status only after writing all of the data to the medium without error. A WCE bit set to 1 specifies that the device server may complete a WRITE command with good status after receiving the data without error and prior to having written the data to the medium.
02h	3	SIZE	0h	A size enable (SIZE) bit set to 0 specifies that the NUMBER OF CACHE SEGMENTS field is used to control caching segmentation. Simultaneous use of both the number of segments and the segment size is vendor specific.
02h	4	DISC	0h	A discontinuity (DISC) bit set to 0 specifies that prefetches be truncated or wrapped at time discontinuities.
02h	5	CAP	0h	A caching analysis permitted (CAP) bit set to 0 specifies that caching analysis is disabled (for example, to reduce overhead time or to prevent non-pertinent operations from impacting tuning values).
02h	6	ABPF	0h	An abort prefetch (ABPF) bit set to 0 when the DRA bit set to 0 specifies that the termination of any active prefetch is dependent upon caching mode page bytes 4 through 11 and is vendor specific.
02h	7	IC	0h	An initiator control (IC) enable bit set to 0 specifies that the device server uses its own adaptive caching algorithm.
03h	3:0	WRITE RETENTION PRIORITY	0h	This field set to 0h means that the device server should not distinguish between retaining the indicated data and data placed into the cache by other means (for example, prefetch).
03h	7:4	DEMAND READ RETENTION PRIORITY	0h	This field set to 0 means that the device server should not distinguish between retaining the indicated data and data placed into the cache by other means (for example, prefetch).
04h	15:0	DISABLE PREFETCH TRANSFER LENGTH	0h	This field specifies the selective disabling of anticipatory prefetch on long transfer lengths. If this field is set to 0, then all anticipatory prefetching is disabled for any request for data, including those with a transfer length of 0.
06h	15:0	MINIMUM PREFETCH	0h	This field specifies the number of logical blocks to prefetch regardless of the delays it might cause in processing subsequent commands. If MF bit is set to 0, this field contains the number of logical blocks.
08h	15:0	MAXIMUM PREFETCH	0h	This field specifies the number of logical blocks to prefetch if the prefetch does not delay processing of subsequent commands. If MF bit is set to 0, this field contains the number of logical blocks.

Table 27: Caching Mode Page (Continued)

Offset	Bit	Field	Default Value	Description
0Ah	15:0	MAXIMUM PREFETCH CEILING	0h	This field specifies an upper limit on the number of logical blocks computed as the maximum prefetch. If this number of logical blocks is greater than the value in the MAXIMUM PREFETCH field, then the number of logical blocks to prefetch shall be truncated to the value stored in this field.
0Ch	0	NV_DIS	0h	An NV_DIS bit set to 0 specifies that the device server may use a nonvolatile cache and indicates that a nonvolatile cache may be present and enabled.
0Ch	2:1	Reserved	–	–
0Ch	4:3	Vendor specific	0h	Vendor specific
0Ch	5	DRA	0h	A disable read-ahead (DRA) bit set to 0 specifies that the device server may continue to read logical blocks into the prefetch buffer beyond the addressed logical block(s).
0Ch	6	LBCSS	0h	A logical block cache segment size (LBCSS) bit set to 0 specifies that the CACHE SEGMENT SIZE field units shall be interpreted as bytes. The LBCSS shall not impact the units of other fields.
0Ch	7	FSW	0h	A force sequential write (FSW) bit set to 0 specifies that the device server may reorder the sequence of writing logical blocks (for example, in order to achieve faster command completion).
0Dh	7:0	NUMBER OF CACHE SEGMENTS	0h	This field specifies the number of segments into which the device server shall divide the cache.
0Eh	15:0	CACHE SEGMENT SIZE	0h	This field specifies the segment size in bytes if the LBCSS bit is set to 0 or in logical blocks if the LBCSS bit is set to 1. This field is valid only when the SIZE bit is set to 1.
10h	7:0	Reserved	–	–
11h	15:0	Obsolete	0h	Not available

Note: 1. Some fields are user configurable.

UFS Vital Product Data Parameters

The vital product data (VPD) pages are returned by an INQUIRY command with the EVPD bit set to 1 and contain vendor specific product information about a logical unit and SCSI target device. A UFS device supports the following VPD pages.

Table 28: Supported VPD Pages

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device 1Eh: Well known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	0h	This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB.
02h	15:0	PAGE LENGTH	07h	This field indicates the length in bytes of the VPD parameters that follow this field.
04h	7:0	Supported VPD Page List[0]	0h	The supported VPD page list contains a list of all VPD page codes implemented by the logical unit in ascending order beginning with page code 00h: SUPPORTED_VPD_PAGE
05h	7:0	Supported VPD Page List[1]	80h	UNIT_SERIAL_NUM
06h	7:0	Supported VPD Page List[2]	83h	DEVICE_ID
07h	7:0	Supported VPD Page List[3]	87h	MODE_PAGE_POLICY
08h	7:0	Supported VPD Page List[4]	B0h	BLOCK_LIMITS
09h	7:0	Supported VPD Page List[5]	B1h	BLOCK_DEVICE_CHARACTERISTICS
0Ah	7:0	Supported VPD Page List[6]	B2h	LOGICAL_BLOCK_PROVISIONING

Table 29: Unit Serial Number VPD Page

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device 1Eh: Well known logical unit

Table 29: Unit Serial Number VPD Page (Continued)

Offset	Bit	Field	Default Value	Description
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	80h	This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB.
02h	15:0	PAGE LENGTH	4h	This field indicates the length in bytes of the VPD parameters that follow this field.
04h	7:0	PRODUCT SERIAL NUMBER	–	This field contains right-aligned ASCII data that is vendor-assigned serial number.

Table 30: Device Identification VPD Page

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device 1Eh: Well known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	83h	This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB.
02h	15:0	PAGE LENGTH	Ch	This field indicates the length in bytes of the VPD parameters that follow this field.
04h	4:0	CODE SET	2h	This field contains a code set enumeration that indicates the format of the DESIGNATOR field.
04h	7:5	PROTOCOL IDENTIFIER	0h	This field may indicate the SCSI transport protocol to which the designation descriptor applies.
05h	3:0	DESIGNATOR TYPE	1h	This field indicates the format and assignment authority for the designator.
05h	5:4	ASSOCIATION	0h	This field indicates the entity with which the DESIGNATOR field is associated. If a logical unit returns a designation descriptor with this field set to 00b or 10b, it shall return the same descriptor when it is accessed through any other I_T nexus.
05h	6	Reserved	–	–
05h	7	PIV	0h	A protocol identifier valid (PIV) bit set to 0 indicates the PROTOCOL IDENTIFIER field contents are reserved.

Table 30: Device Identification VPD Page (Continued)

Offset	Bit	Field	Default Value	Description
06h	7:0	Reserved	–	–
07h	7:0	DESIGNATOR LENGTH	8h	This field indicates the length in bytes of the DESIGNATOR field.
08h	23:0	IEEE COMPANY ID	–	–
0Bh	39:0	VENDOR SPECIFIC EXTENSION IDENTIFIER	–	–

Table 31: Mode Page Policy VPD Page

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device 1Eh: Well known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	87h	This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB.
02h	15:0	PAGE LENGTH	0Ch	This field indicates the length in bytes of the VPD parameters that follow this field.
Mode page policy descriptor [0]				Contains information describing the mode page policy for read-write error recovery mode page.
04h	5:0	Policy page code	1h	
04h	7:6	Reserved1	0h	
05h	7:0	Policy subpage code	0h	
06h	1:0	ModePagePolicy	0h	
06h	6:2	Reserved 2	0h	
06h	7	MLUS	1h	
07h	7:0	Reserved 3	0h	
Mode page policy descriptor [1]				Contains information describing the mode page policy for caching mode page.
08h	5:0	Policy page code	8h	
08h	7:6	Reserved1	0h	
09h	7:0	Policy subpage code	0h	
0Ah	1:0	Mode page policy	0h	
0Ah	6:2	Reserved 2	0h	
0Ah	7	MLUS	01h	
0Bh	7:0	Reserved 3	0h	

Table 31: Mode Page Policy VPD Page (Continued)

Offset	Bit	Field	Default Value	Description
Mode page policy descriptor [2]				Contains information describing the mode page policy for control mode page.
0Ch	5:0	Policy page code	Ah	
0Ch	7:6	Reserved 1	0h	
0Dh	7:0	Policy subpage code	0h	
0Eh	1:0	ModePagePolicy	0h	
0Eh	6:2	Reserved 2	0h	
0Eh	7	MLUS	0h	
0Fh	7:0	Reserved 3	0h	
Mode page policy descriptor [3]				Contains information describing the mode page policy for all mode pages.
10h	5:0	Policy page code	3Fh	
10h	7:6	Reserved1	0h	
11h	7:0	Policy subpage code	0h	
12h	1:0	ModePagePolicy	0h	
12h	6:2	Reserved 2	0h	
12h	7	MLUS	0h	
13h	7:0	Reserved 3	0h	
Mode page policy descriptor [4]				Contains information describing the mode page policy for all mode pages and subpages.
14h	5:0	Policy page code	3Fh	
14h	7:6	Reserved1	0h	
15h	7:0	Policy subpage code	FFh	
16h	1:0	ModePagePolicy	0h	
16h	6:2	Reserved 2	0h	
16h	7	MLUS	0h	
17h	7:0	Reserved 3	0h	

Table 32: Block Limits VPD Page

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device 1Eh: Well known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.

Table 32: Block Limits VPD Page (Continued)

Offset	Bit	Field	Default Value	Description
01h	7:0	PAGE CODE	B0h	This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB.
02h	15:0	PAGE LENGTH	3Ch	This field indicates the length in bytes of the VPD parameters that follow this field.
04h	7:0	Reserved	–	–
05h	7:0	MAXIMUM COMPARE AND WRITE LENGTH	0h	This field is set to 0, if the device server does not support this command.
06h	15:0	OPTIMAL TRANSFER LENGTH GRANULARITY	20h	This field indicates the optimal transfer length granularity in blocks for a single ORWRITE command, PREFETCH command, READ command, VERIFY command, WRITE command, WRITE AND VERIFY command, XDREAD command, XDWRITE command, XDWRITEREAD command, or XPWRITE command.
08h	31:0	MAXIMUM TRANSFER LENGTH	0h	This field indicates the maximum transfer length in blocks that the device server accepts for a single ORWRITE command, READ command, VERIFY command, WRITE command, WRITE AND VERIFY command, XDWRITEREAD command, or XPWRITE command.
0Ch	31:0	OPTIMAL TRANSFER LENGTH	20h	This field indicates the optimal transfer length in blocks for a single ORWRITE command, PREFETCH command, READ command, VERIFY command, WRITE command, WRITE AND VERIFY command, XDREAD command, XDWRITE command, XDWRITEREAD command, or XPWRITE command.
10h	31:0	MAXIMUM PREFETCH XDREAD XDWRITE TRANSFER LENGTH	100h	This field indicates: a) the maximum transfer length in blocks that the device server accepts for a single PREFETCH command b) if the XOR control mode page is implemented, then the maximum value supported by the MAXIMUM XOR WRITE SIZE field in the XOR control mode page. c) if the XOR control mode page is not implemented, then the maximum transfer length in blocks that the device server accepts for a single XDWRITE command or XDREAD command. The device server should set this field to less than or equal to the MAXIMUM TRANSFER LENGTH field.
14h	31:0	MAXIMUM UNMAP LBA COUNT	FFFFFFFFh	This field indicates the maximum number of LBAs that may be unmapped by an UNMAP command. If the number of LBAs that may be unmapped by an UNMAP command is constrained only by the amount of data that may be contained in the UNMAP parameter list, then the device server shall set this field to FFFF_FFFFh. If the device server implements the UNMAP command, then the value in this field shall be greater than or equal to 1.

Table 32: Block Limits VPD Page (Continued)

Offset	Bit	Field	Default Value	Description
18h	31:0	MAXIMUM UNMAP BLOCK DESCRIPTOR COUNT	1h	This field indicates the maximum number of unmap block descriptors that shall be contained in the parameter data transferred to the device server for an UNMAP command. If there is no limit on the number of unmap block descriptors contained in the parameter data, then the device server shall set this field to FFFF_FFFFh. If the device server implements the UNMAP command, then the value in this field shall be greater than or equal to 1.
1Ch	31:0	OPTIMAL UNMAP GRANULARITY	1h	This field indicates the optimal granularity in logical blocks for unmap requests. An unmap request with a number of logical blocks that is not a multiple of this value may result in UNMAP operations on fewer LBAs than requested. If this field is set to 0000_0000h, then the optimal unmap granularity is not specified.
20h	30:0	UNMAP GRANULARITY ALIGNMENT	0h	This field indicates the LBA of the first logical block to which the OPTIMAL UNMAP GRANULARITY field applies. The unmap granularity alignment is used to calculate an optimal unmap request starting LBA as follows: Optimal unmap request starting LBA = (n × OPTIMAL UNMAP GRANULARITY) + UNMAP GRANULARITY ALIGNMENT Where n is 0 or any positive integer value.
20h	31	UGAVALID	0h	An unmap granularity alignment valid (UGAVALID) bit set to 0 indicates that the UNMAP GRANULARITY ALIGNMENT field is not valid.

Table 33: Block Device Characteristics

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device 1Eh: Well known logical unit
00h	7:5	PERIPHERAL QUALIFIER	000h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	B1h	This fields identifies the VPD page and contains the same value as in the PAGE CODE field in the INQUIRY CDB
02h	15:0	PAGE LENGTH	3Ch	This field indicates the length in bytes of the VPD parameters that follow this field.
04h	15:0	MEDIUM ROTATION RATE	0001h	0001h means device is a non-rotating medium (for example, solid state).

Table 33: Block Device Characteristics (Continued)

Offset	Bit	Field	Default Value	Description
06h	7:0	Reserved	–	–
07h	3:0	NOMINAL FORM FACTOR	05h	This field indicates the nominal form factor of the device containing the logical unit.
07h	7:4	Reserved	–	–

Table 34: Logical Block Provisioning

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device 1Eh: Well known logical unit
00h	7:5	PERIPHERAL QUALIFIER	000h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	7:0	PAGE CODE	B2h	This fields identifies the VPD page and contains the same value as in the PAGE CODE field in the INQUIRY CDB
02h	15:0	PAGE LENGTH	04h	This field indicates the length in bytes of the VPD parameters that follow this field.
04h	7:0	THRESHOLD EXPONENT	16h	This field indicates the threshold set size in LBAs as a power of 2.
05h	0	DP	00h	A descriptor present (DP) bit set to 0 indicates that a PROVISIONING GROUP DESCRIPTOR is not present.
05h	1	ANC_SUP	00h	This bit set to 0 indicates that the device server does not support anchored LBAs.
05h	5:2	Reserved	–	–
05h	6	TBPWS	00h	This bit set to 0 indicates that the device server does not support the use of the WRITE SAME (16) command to unmap LBAs.
05h	7	TPU	01h	This bit set to 1 indicates that the device server supports the UNMAP command.
06h	7:0	Reserved	–	–
07h	7:0	Reserved	–	–

When the EVPD bit is set to 0 and page code = 0, the standard INQUIRY DATA is responded to INQUIRY command. The standard INQUIRY DATA format is shown in the table below:

Table 35: Standard Inquiry Data

Offset	Bit	Field	Default Value	Description
00h	4:0	PERIPHERAL DEVICE TYPE	1Eh	This bit set to 1 means device server is a direct access block device 1Eh: Well known logical unit
00h	7:5	PERIPHERAL QUALIFIER	0h	A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access.
01h	6:0	Reserved	–	–
01h	7	RMB	0h	A removable medium (RMB) bit set to 0 indicates that the medium is not removable.
02h	7:0	VERSION	6h	This field indicates the implemented version of this standard. This field set to 06h means the conformance to SPC.
03h	3:0	RESPONSE DATA FORMAT	2h	This field value of two indicates that the data shall be in the format defined in SPC.
03h	7:4	NA1	0h	Not available in UFS standard
04h	7:0	ADDITIONAL LENGTH	1Fh	This field indicates the length in bytes of the remaining standard INQUIRY data.
05h	7:0	NA2	0h	Not available in UFS standard
06h	7:0	NA3	0h	Not available in UFS standard
07h	0	NA4	0h	Not available in UFS standard
07h	1	CMDQUE	1h	This bit is set to 1 indicating that the logical unit supports the command management model (SAM).
07h	7:2	NA5	0h	Not available in UFS standard
08h	15:0	VENDOR IDENTIFICATION	–	This field contains left-aligned ASCII data identifying the vendor of the product.
10h	15:0	PRODUCT IDENTIFICATION	–	This field contains left-aligned ASCII data defined by the vendor.
20h	15:0	PRODUCT REVISION LEVEL	–	This field contains left-aligned ASCII data defined by the vendor.

Electrical Specifications

According to JEDEC UFS v2.1 specification, power-up timing starts when the supply voltage crosses 300mV and ends when it reaches the minimum operating value. Micron device only supports V_{CC} and V_{CCQ2}. V_{CCQ} is not used.

Table 36: Power Supply Parameters

Parameter	Symbol	Min	Max	Unit
V_{CC} operating range	V_{CC}	2.7	3.6	V
V_{CCQ} operating range	V_{CCQ}	–	–	–
V_{CCQ2} operating range	V_{CCQ2}	1.7	1.95	V
Supply power-up timing for 3.3V	t_{PRUH}	–	35	ms
Supply power-up timing for 1.8V	t_{PRUL}	–	25	ms
Supply power-up timing for 1.2V	t_{PRUV}	–	–	–

Table 37: Reference Clock Parameters[1]

Parameter	Symbol	Min	Max	Units
Frequency	f_{ref}	19.2 26 38.4 52		MHz
Frequency error	f_{ERROR}	–150	+150	ppm
Clock rise time[1]	t_{IRISE}	–	2	ns
Clock fall time	t_{IFALL}	–	2	ns
Duty cycle	t_{DC}	45	55	%
Phase noise	N	–	–66	dBc
Noise floor density	$N_{density}$	–	–140	dBc/Hz
Input impedance	RL_{RX}	100	–	kΩ
	CL_{RX}	–	5	pF

Note: 1. V_{IL} parameter is 0.2V on RST_n and REF_CLK signals.

Revision History

Rev. B – 04/2020

- Production release
- Added 256GB device

Rev. A – 11/19

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.