

### DESCRIPTION

The MP6925 is a dual, fast turn-off, intelligent rectifier for synchronous rectification in LLC resonant converters.

The IC drives two N-channel MOSFETs, regulates their forward voltage drop to  $V_{fwd}$  (about 29mV), and turns the MOSFETs off before the switching current goes negative.

The MP6925 has a light-load function to latch off the gate driver under light-load conditions, limiting the current to 175 $\mu$ A.

The MP6925's fast turn-off enables both continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

The MP6925 requires a minimal number of external components, and is available in an SOIC-8 package.

### FEATURES

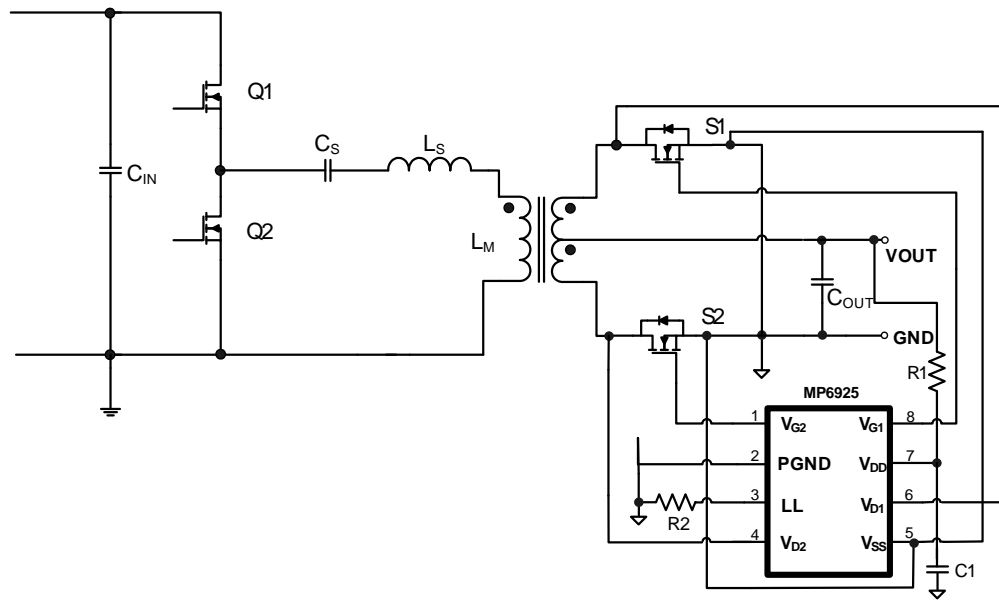
- Works with Standard and Logic Level MOSFETs
- Compatible with Energy Star
- Fast Turn-Off Total Delay of 35ns
- Wide 4.2V to 35V  $V_{DD}$  Operating Range
- 175 $\mu$ A Low Quiescent Current in Light-Load Mode
- Supports CCM, CrCM, and DCM Operation
- Supports High-Side and Low-Side Rectification
- Available in an SOIC-8 Package

### APPLICATIONS

- AC/DC Adapters
- PC Power Supplies
- LCD and LED TVs
- Isolated DC/DC Power Converters

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### TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6925GS	SOIC-8	See Below

\* For Tape & Reel, add suffix -Z (e.g. MP6925GS-Z).

### TOP MARKING

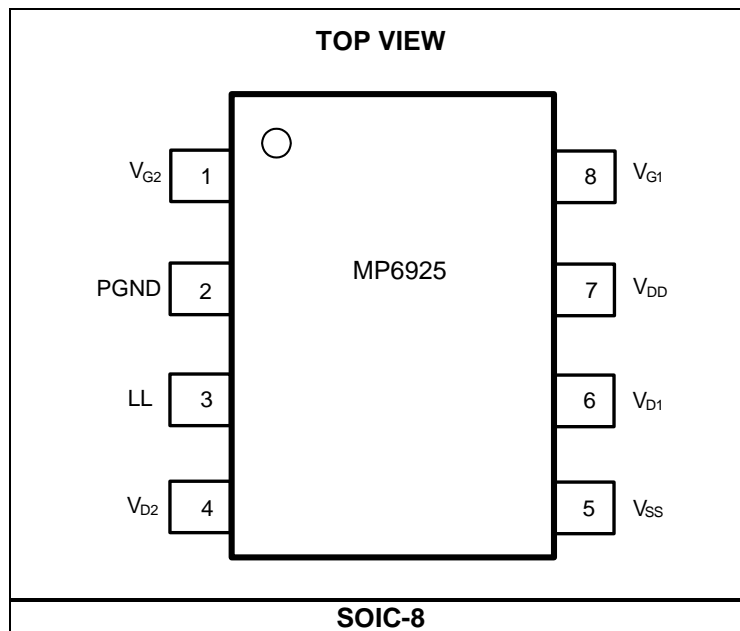
**MP6925**

**LLLLLLLL**

**MPSYWW**

MPS: MPS prefix  
 Y: Year code  
 W: Week code  
 6925: First four digits of the part number  
 LLLLLLLL: Lot number

### PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	V <sub>G2</sub>	<b>MOSFET 2 gate driver output.</b>
2	PGND	<b>Power ground.</b> PGND is the power switch return.
3	LL	<b>Light-load timing setting.</b> Connect a resistor on this pin to set the light-load timing. Leave the LL pin open to disable the light-load function (it is recommended to connect a capacitor on this pin in such a case). Pull LL low to disable the gate driver.
4	V <sub>D2</sub>	<b>MOSFET 2 drain voltage sense.</b>
5	V <sub>SS</sub>	<b>Source pin used as reference for V<sub>D1</sub> and V<sub>D2</sub>.</b>
6	V <sub>D1</sub>	<b>MOSFET 1 drain voltage sense.</b>
7	V <sub>DD</sub>	<b>Supply voltage.</b>
8	V <sub>G1</sub>	<b>MOSFET 1 gate driver output.</b>

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

$V_{DD}$ to $V_{SS}$ .....	-0.3V to +38V
PGND to $V_{SS}$ .....	-0.3V to +0.3V
$V_G$ to $V_{SS}$ .....	-0.3V to +20V
$V_D$ to $V_{SS}$ .....	-1V to +180V
LL to $V_{SS}$ .....	-0.3V to +6.5V
Continuous power dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2)</sup>	
SOIC-8 .....	1.4W
Junction temperature .....	150°C
Lead temperature (solder) .....	260°C
Storage temperature.....	-55°C to +150°C

**Recommended Operation Conditions** <sup>(3)</sup>

$V_{DD}$ to $V_{SS}$ .....	4.2V to 35V
Operating junction temp ( $T_J$ ) ....	-40°C to +125°C

<b>Thermal Resistance</b> <sup>(4)</sup>	$\theta_{JA}$	$\theta_{JC}$
SOIC-8.....	90.....	45 ... °C/W

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{DD} = 12V$ ,  $-40^{\circ}C \leq T_J \leq +125^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
$V_{DD}$ voltage range			4.2		35	V
$V_{DD}$ UVLO rising			3.7	3.95	4.2	V
$V_{DD}$ UVLO hysteresis			0.13	0.185	0.24	V
Operating current	$I_{CC}$	$C_{LOAD} = 4.7nF$ , $f_{SW} = 100kHz$		16	20	mA
Quiescent current	$I_Q$	$V_{SS} - V_D = 0.5V$		4.6	6	mA
Shutdown current		$V_{DD} = 4V$ , $LL = 0V$		135	190	$\mu A$
		$V_{DD} = 20V$ , $LL = 0V$		155	210	
Light-load mode current				175	225	$\mu A$
Thermal shutdown <sup>(5)</sup>				175		$^{\circ}C$
Thermal shutdown hysteresis <sup>(5)</sup>				10		$^{\circ}C$
<b>Control Circuitry Section</b>						
$V_{SS} - V_D$ forward voltage	$V_{fwd}$		17	29	41	mV
Turn-off threshold ( $V_{SS} - V_D$ )	$V_{Drv-off}$		-56	-40	-20	mV
Turn-on delay	$t_{Don}$	$C_{LOAD} = 4.7nF$ , $V_{GS} = 2V$		190	300	ns
	$t_{Don}$	$C_{LOAD} = 10nF$ , $V_{GS} = 2V$		270	410	ns
Input bias current on $V_D$		$V_D = 180V$			1	$\mu A$
Turn-on blanking time	$t_{B\_ON}$	$C_{LOAD} = 4.7nF$	0.75	1.1	1.65	$\mu s$
Turn-off blanking time <sup>(5)</sup>	$t_{B\_OFF}$	$C_{LOAD} = 4.7nF$		1750		ns
Light-load enter pulse width	$t_{LL}$	$R_{LL} = 100k\Omega$	1.7	2.3	3	$\mu s$
Light-load turn-on pulse width hysteresis	$t_{LL-H}$	$R_{LL} = 100k\Omega$		0.45		$\mu s$
Light-load enter delay	$t_{LL-D}$		45	78	121	$\mu s$
Light-load enter pulse-width threshold ( $V_{G1,2} - V_{SS}$ ) <sup>(5)</sup>	$V_{LL-GS}$			0.6		V
Gate disable threshold on LL	$V_{LL\_DIS}$		0.1	0.2	0.3	V
Turn-on threshold ( $V_{DS}$ )	$V_{LL\_DS}$	$V_{DD} = 12V$	-330	-230	-130	mV
<b>Gate Driver Section</b>						
$V_G$ (low)	$V_{G\_L}$	$I_{LOAD} = 1mA$			0.1	V
$V_G$ (high)	$V_{G\_H}$	$V_{DD} > 10V$		11.5	13	V
		$V_{DD} \leq 10V$		$V_{DD}$		
Turn-off propagation delay		$V_D = V_{SS}$		15		ns
Turn-off total delay	$t_{Doff}$	$V_D = V_{SS}$ , $C_{LOAD} = 4.7nF$ , $R_{GATE} = 0\Omega$ , $V_{GS} = 2V$		35	80	ns
	$t_{Doff}$	$V_D = V_{SS}$ , $C_{LOAD} = 10nF$ , $R_{GATE} = 0\Omega$ , $V_{GS} = 2V$		45	100	ns
Pull-down impedance				0.6	1.5	$\Omega$

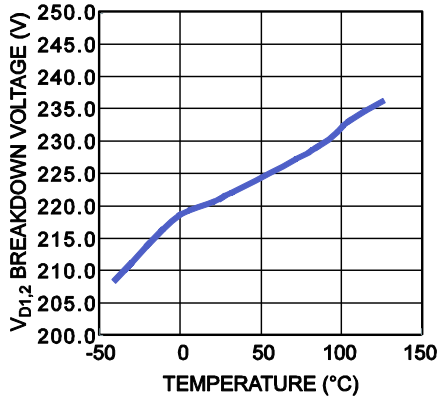
**Note:**

5) Guaranteed by characterization.

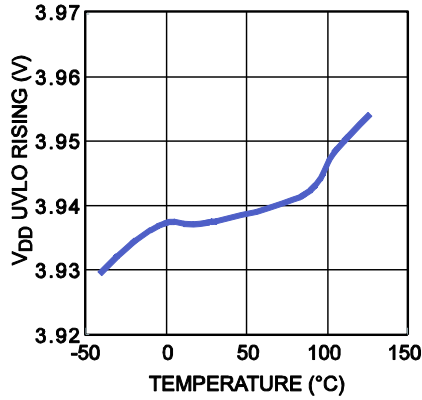
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 12V$ , unless otherwise noted.

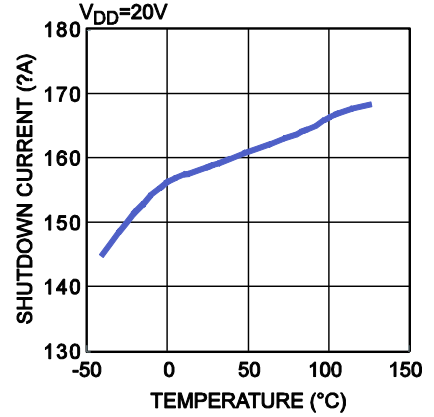
**$V_{D1,2}$  Breakdown Voltage vs. Temperature**



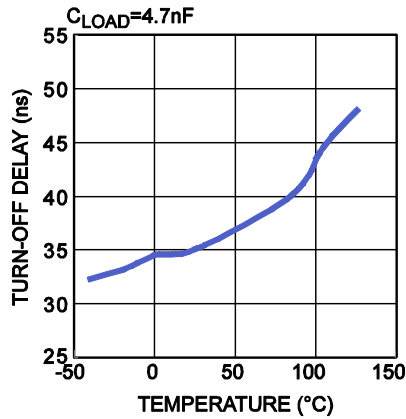
**$V_{DD}$  UVLO Rising vs. Temperature**



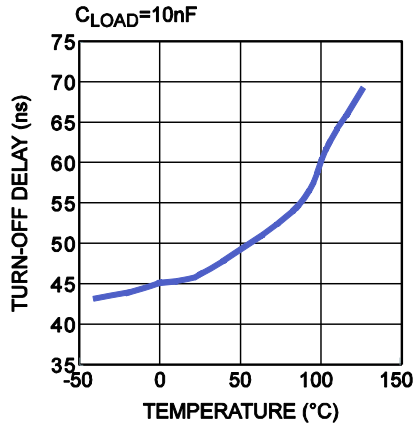
**Shutdown Current vs. Temperature**



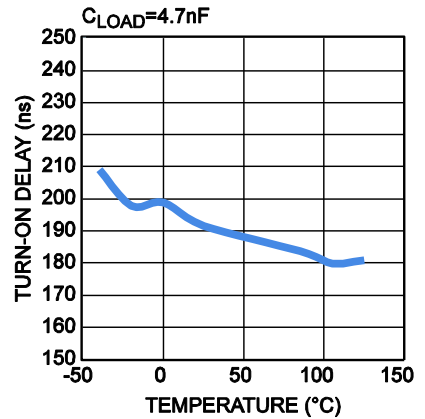
**Turn-Off Delay vs. Temperature**



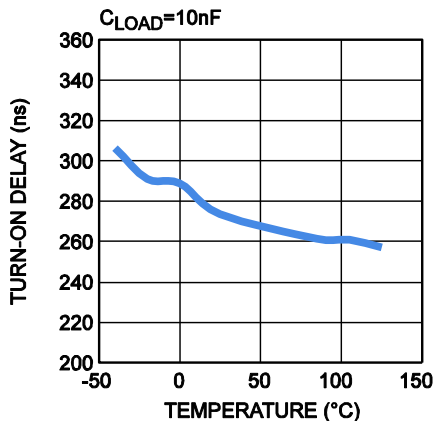
**Turn-Off Delay vs. Temperature**



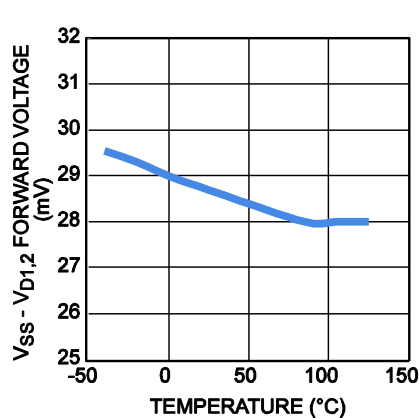
**Turn-On Delay vs. Temperature**



**Turn-On Delay vs. Temperature**



**$V_{SS} - V_{D1,2}$  Forward Voltage vs. Temperature**

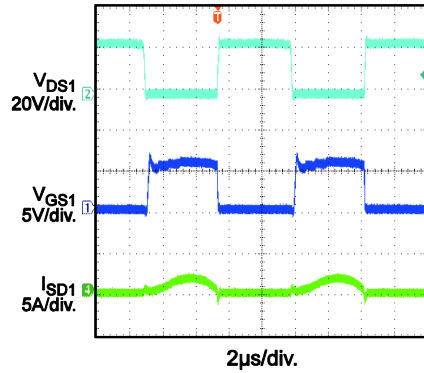


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} = 12V$ , unless otherwise noted.

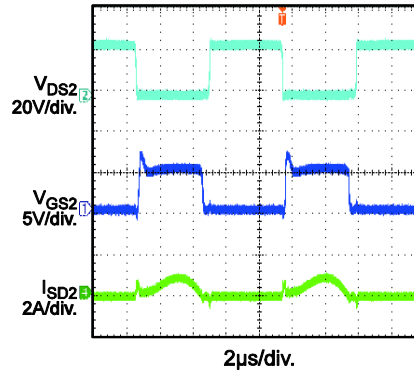
### Operation in 90W LLC Converter

$V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=0.75A$



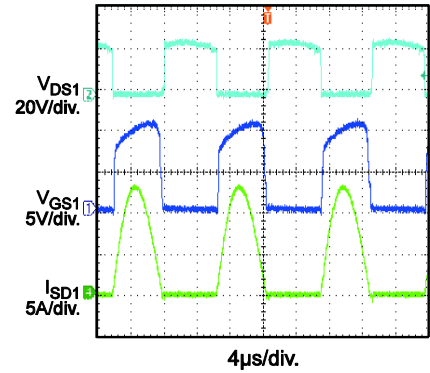
### Operation in 90W LLC Converter

$V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=0.75A$



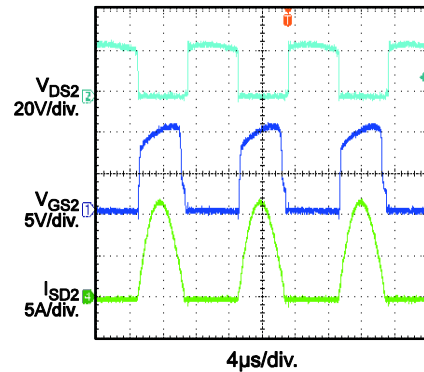
### Operation in 90W LLC Converter

$V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=7.5A$



### Operation in 90W LLC Converter

$V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=7.5A$



### FUNCTIONAL BLOCK DIAGRAM

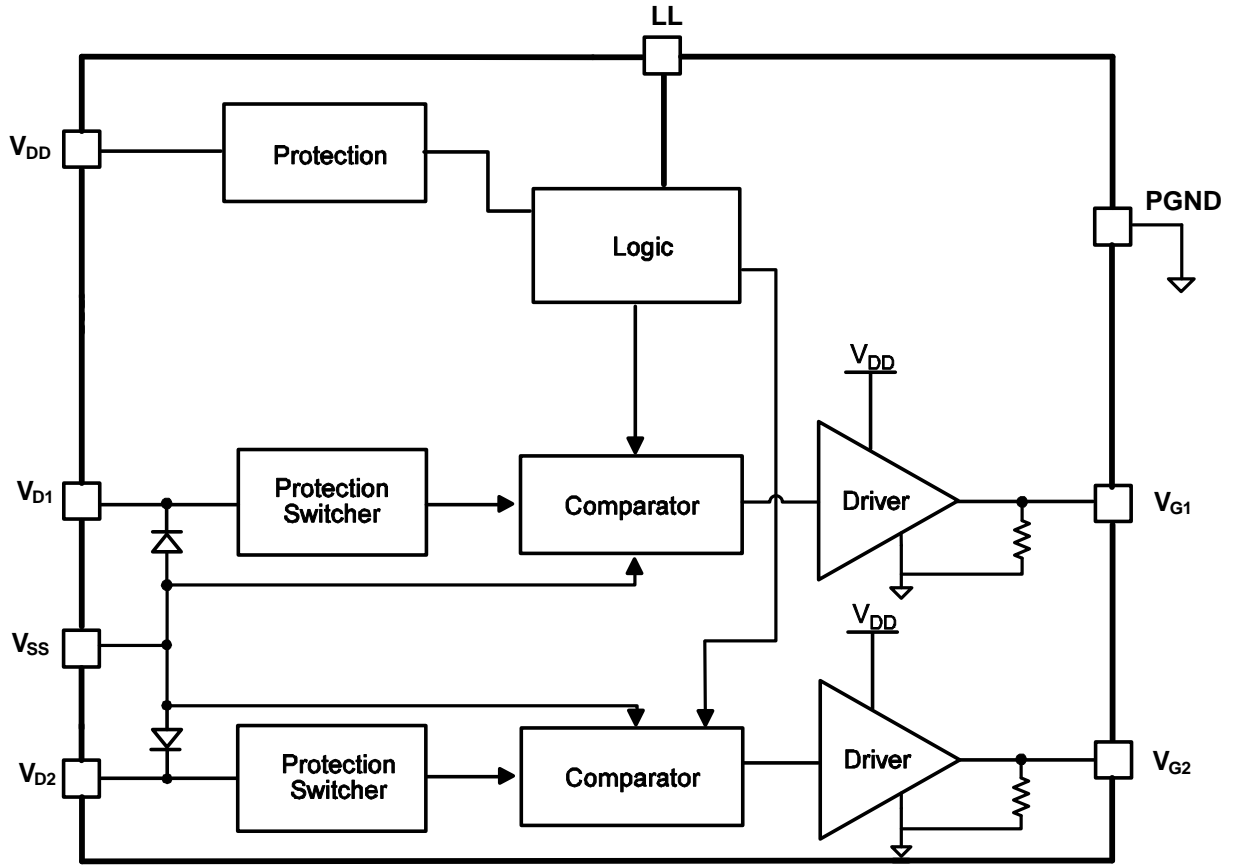


Figure 1: Functional Block Diagram



## OPERATION

The MP6925 can operate in discontinuous conduction mode (DCM), continuous conduction mode (CCM), and critical conduction mode (CrCM). When the MP6925 operates in DCM or CrCM, the control circuitry controls the gate in forward mode. The gate turns off when the MOSFET current is low. In CCM, the control circuitry turns off the gate during very fast transients.

### VD Clamp

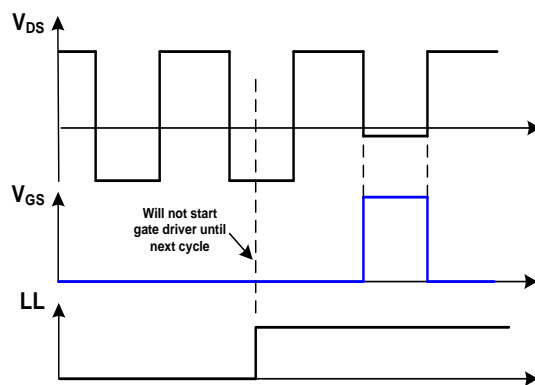
Because  $V_{D1,2}$  can rise as high as 180V, a high-voltage JFET is used at the input. To prevent excessive currents when  $V_{DS1,2}$  falls below -0.7V, a 1k $\Omega$  resistor is recommended between  $V_{D1,2}$  and the drain of the external MOSFET.

### Under-Voltage Lockout (UVLO)

When  $V_{DD}$  is below the  $V_{DD}$  UVLO threshold, the MP6925 goes into sleep mode, and  $V_{G1,2}$  remains at a low level.

### Enable

If LL is pulled low, the MP6925 enters shutdown mode, which consumes 175 $\mu$ A of shutdown current. If LL is pulled high during the rectification cycle, the gate driver does not appear until the next rectification cycle begins (see Figure 2).



**Figure 2: LL Control Scheme**

### Thermal Shutdown

If the junction temperature of the chip exceeds the thermal shutdown threshold,  $V_{G1,2}$  is pulled low, and the MP6925 stops switching. The IC resumes normal functioning after the junction temperature drops by 10 $^{\circ}$ C.

### Turn-On Phase

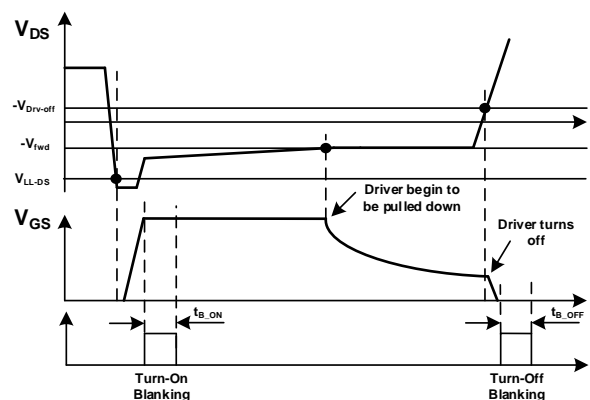
When the switch current flows through the body diode of the MOSFET, there is a negative voltage drop ( $V_D - V_{SS}$ ) across the body diode.  $V_{DS}$  is much lower than the turn-on threshold of the control circuitry ( $V_{LL-DS}$ ), which triggers a charge current to turn on the MOSFET (see Figure 3).

### Turn-On Blanking

The control circuitry contains a blanking function that ensures that when the MOSFET turns on or off, it remains in that state for  $t_{B\_ON}$  (~1.1 $\mu$ s), which determines the minimum on time. During the turn-on blanking period, the turn-off threshold is not blanked completely, but changes to about +100mV (instead of  $-V_{Drv-off}$ ). This ensures that the part can always turn off, even during the turn-on blanking period, although it does so more slowly. Avoid setting the synchronous period below  $t_{B\_ON}$  in CCM in the LLC converter to eliminate shoot-through.

### Conduction Phase

When  $V_{DS}$  rises above the forward voltage drop ( $-V_{fwd}$ ) according to the decrease of the switching current, the MP6925 pulls down the gate voltage level to make the on resistance of the synchronous MOSFET larger, which eases the rise of  $V_{DS}$ .



**Figure 3: Turn-On/Turn-Off Timing Diagram**

The control scheme in Figure 3 shows  $V_{DS}$  adjusted to be about  $-V_{fwd}$ , even when the current through the MOSFET is fairly low. This function puts the driver voltage at a very low level when

the synchronous MOSFET is turning off, which boosts the turn-off speed.

### Turn-Off Phase

When  $V_{DS}$  rises to trigger the turn-off threshold, the gate voltage is pulled to zero after a very short turn-off delay (see Figure 3).

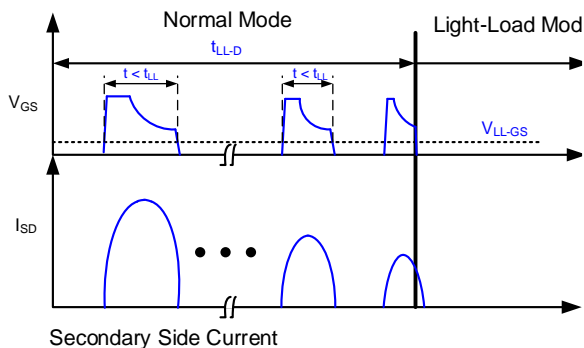
### Turn-Off Blanking

After the gate driver is pulled to zero by  $V_{DS}$  reaching the turn-off threshold, turn-off blanking is triggered to ensure that the gate driver is off for at least  $t_{B\_OFF}$  to prevent an erroneous trigger on  $V_{DS}$ .

### Light-Load Latch-Off Function

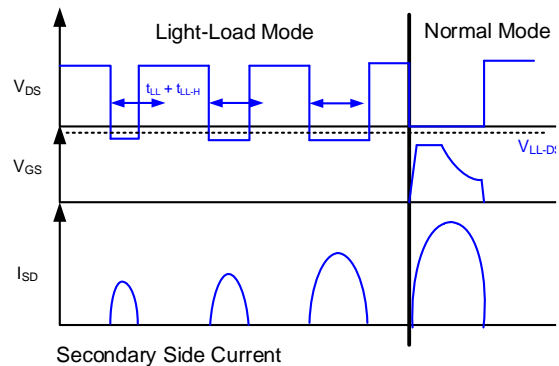
The gate driver of the IC is latched off to save driver loss in a light-load condition and improve efficiency.

The MP6925 compares the CH1 SR gate (VG1) driver with the light-load enter pulse width threshold ( $V_{LL-GS}$ ) every cycle to determine the gate driver pulse width. If the CH1 SR gate driver pulse width remains below  $t_{LL}$  every cycle for longer than the light-load enter delay ( $t_{LL-D}$ ), the MP6925 shuts down both channel gates immediately and enters light-load mode, which latches off the SR MOSFET (see Figure 4).



**Figure 4: MP6925 Entering Light-Load Mode**

In light-load mode, the MP6925 monitors the body diode conduction time of CH1 by comparing the drain-source voltage of the SR MOSFET with the turn-on threshold ( $V_{LL-DS}$ ). If this time exceeds  $t_{LL} + t_{LL-H}$ , the IC exits light-load mode and initiates the gate driver in the next new switching cycle (see Figure 5 and Figure 6).



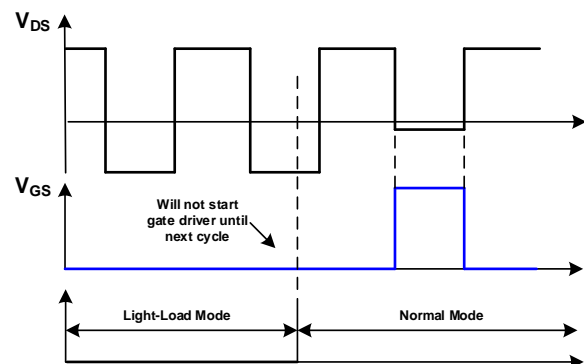
**Figure 5: MP6925 Exiting Light-Load Mode**

Light-load enter timing ( $t_{LL}$ ) is programmable by connecting a resistor ( $R_{LL}$ ) to LL. By monitoring the LL current (the LL voltage is kept at  $\sim 2V$  internally),  $t_{LL}$  can be calculated with Equation (1):

$$t_{LL} = R_{LL} (\text{k}\Omega) \cdot \frac{2.3\mu\text{s}}{100\text{k}\Omega} \quad (1)$$

If the LL pin resistor is disconnected, light-load mode is disabled. In such case, a capacitor (typically 22pF) is highly recommended on this pin to avoid noise.

If the light-load mode of the MP6925 ends during the rectification cycle, the gate driver signal does not appear until the next rectification cycle begins (see Figure 6).



**Figure 6: Gate Driver Starting after Exiting Light-Load Mode**

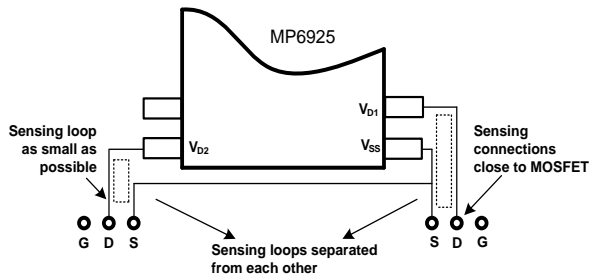
## APPLICATION INFORMATION

### Layout Considerations

Listed below are the main recommendations that should be taken into consideration when designing the PCB.

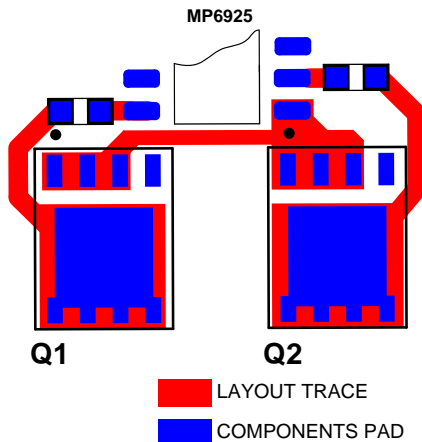
#### Sensing for $V_D/V_S$

1. Keep the sensing connections ( $V_{D1}/V_{SS}$ ,  $V_{D2}/V_{SS}$ ) as close to each of the MOSFETs (drain/source) as possible.
2. Keep the two channels' sensing loops separated from each other.
3. Make the sensing loop as small as possible (see Figure 7).



**Figure 7: Sensing for  $V_D/V_S$**

Figure 8 shows a layout example of the MP6925 driving PowerPAK SO8 package MOSFETs with two separate, small sensing loops.



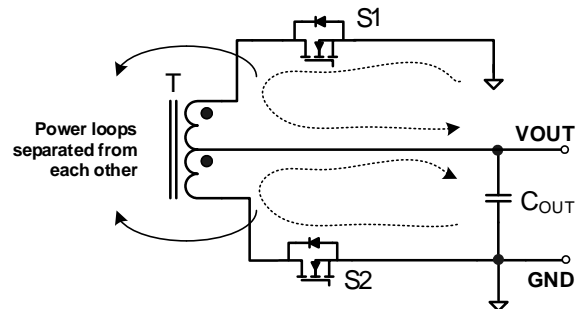
**Figure 8: Layout Example for Sensing Loop and  $V_{DD}$  Decoupling**

#### $V_{DD}$ Decoupling Capacitor

1. Place a decoupling capacitor no smaller than  $1\mu\text{F}$  from  $V_{DD}$  to PGND close to the IC for adequate filtering (see Figure 9).

### System Power Loop

1. Keep the two channels' power loops separated from each other (see Figure 9).  
*This minimizes the interaction between the two channels' power loops, which may affect the voltage sensing of the IC.*
2. Make the power loop as small as possible to reduce parasitic inductance.

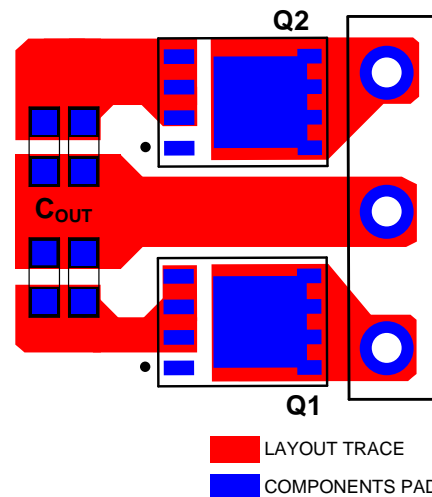


**Figure 9: System Power Loop**

Figure 10 shows a layout example of the power loop trace, which has a minimized loop length. The two channel power traces do not cross each other.

It is highly recommended to place the driver's sensing loop trace away from the power loop trace (see Figure 10). The sensing loop trace and power loop trace can be placed on different layers to keep them separate from each other.

Do not place the driver IC inside the power loop. This may affect MOSFET voltage sensing.



**Figure 10: Layout Example for System Power Loop**

### SR MOSFET Selection and Driver Ability

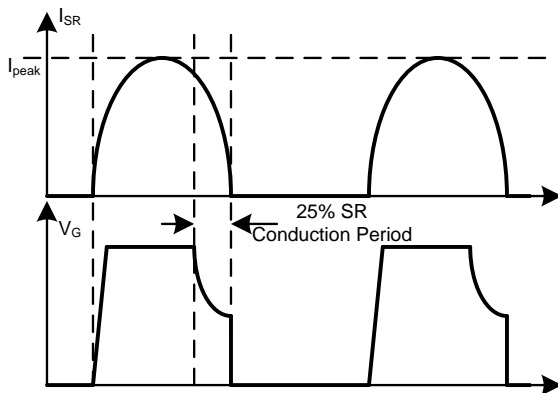
Power MOSFET selection is a trade-off between  $R_{DS(ON)}$  and  $Q_g$ . To achieve high efficiency, a MOSFET with a smaller  $R_{DS(ON)}$  is recommended. A larger  $Q_g$  with a smaller  $R_{DS(ON)}$  makes the turn-on and turn-off speed lower and the power loss greater. For the MP6925,  $V_{DS}$  is adjusted at  $V_{fwd}$  during the driving period. A MOSFET with a small  $R_{DS(ON)}$  is not recommended because the gate driver may be kept at a fairly low level with a small  $R_{DS(ON)}$ , even when the system load is high, which makes the advantage of the low  $R_{DS(ON)}$  inconspicuous.

Figure 11 shows the typical waveform of the LLC on the secondary side. To achieve a fairly high usage of the MOSFET's  $R_{DS(ON)}$ , it is expected that the MOSFET driver voltage is kept at the maximum level until the last 25% of the SR conduction period.  $V_{DS}$  can be calculated using Equation (2):

$$V_{DS} = -R_{DS(ON)} \cdot \frac{\sqrt{2}}{2} \cdot I_{peak} = -R_{DS(ON)} \cdot I_{OUT} = -V_{fwd} \quad (2)$$

Where  $V_{DS}$  is the drain-source voltage of the MOSFET.

The MOSFET's  $R_{DS(ON)}$  is recommended to be no less than  $\sim V_{fwd} / I_{OUT}$  (m $\Omega$ ). For example, in a 10A application with  $V_{fwd}$  at 29mV, the  $R_{DS(ON)}$  of the MOSFET is recommended to be no less than 2.9m $\Omega$ .

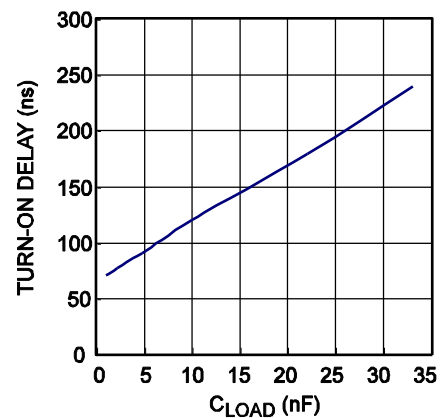


**Figure 11: Synchronous Rectification Typical Waveform in LLC**

$Q_g$  of the MOSFET affects the turn-on delay ( $t_{Don}$ ) and the turn-off delay ( $t_{Doff}$ ).  $t_{Don}$  indicates how long the body diode conducts before the MOSFET turns on, while  $t_{Doff}$  indicates how long the driver takes to turn off the MOSFET. With a longer turn-on delay, the body diode conduction duration of the MOSFET is longer, which brings down the total efficiency. However, with a longer turn-off delay, the shoot-through risk is higher in CCM operation.

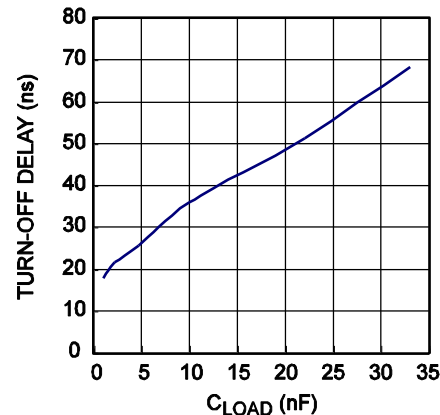
Figure 12 and Figure 13 show the  $t_{Don}$  and  $t_{Doff}$  of the MP6925 based on different  $C_{LOAD}$  values.

### Turn-On Delay vs. $C_{LOAD}$

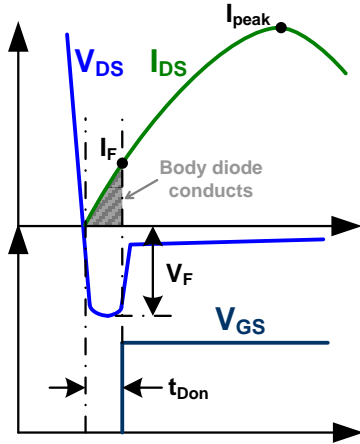


**Figure 12: Turn-On Delay vs.  $C_{LOAD}$**

### Turn-Off Delay vs. $C_{LOAD}$



**Figure 13: Turn-Off Delay vs.  $C_{LOAD}$**



**Figure 14: Turn-On Delay Effect on Efficiency**

Figure 14 shows how  $t_{Don}$  affects system efficiency. During  $t_{Don}$ , the body diode of the SR MOSFET conducts, which leads to a power loss that can be calculated with Equation (3):

$$P_{on} \approx \frac{V_F \cdot I_F}{2} \cdot 2f_{SW} \cdot t_{Don} = V_F \cdot I_F \cdot f_{SW} \cdot t_{Don} \quad (3)$$

Where  $V_F$  is the body diode forward voltage drop,  $I_F$  is the switching current when the turn-on delay ( $t_{Don}$ ) has ended, and  $f_{SW}$  is the switching frequency.

When considering the switching current as a complete sine wave,  $I_F$  can be estimated with Equation (4) and Equation (5):

$$I_F = I_{peak} \cdot \sin(2 \cdot f_{SW} \cdot t_{Don} \cdot \pi) \quad (4)$$

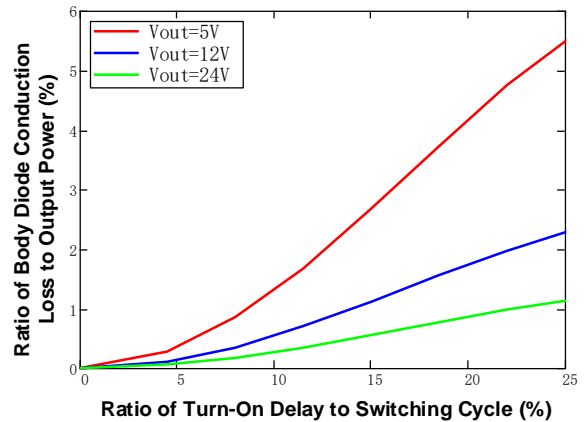
$$I_{peak} \approx \frac{\pi}{2} \cdot I_{OUT} \quad (5)$$

Where  $I_{peak}$  is the peak switching current through the MOSFET, and  $I_{OUT}$  is the system output current.

When plugging the values from Equation (4) and Equation (5) into Equation (3), the turn-on delay power loss through the SR MOSFET's body diode can be derived with Equation (6):

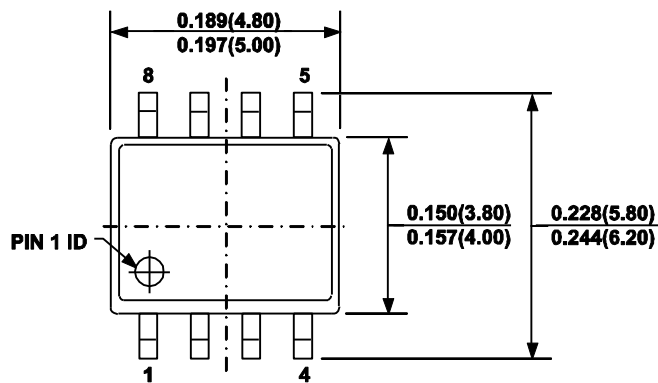
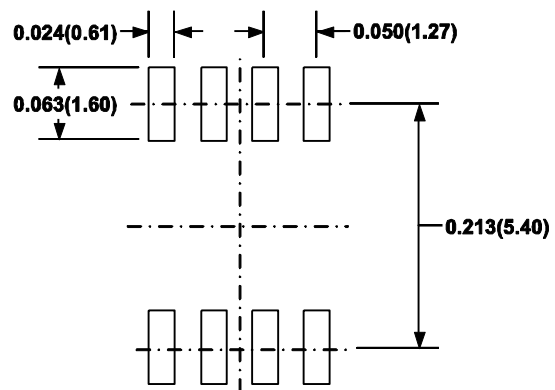
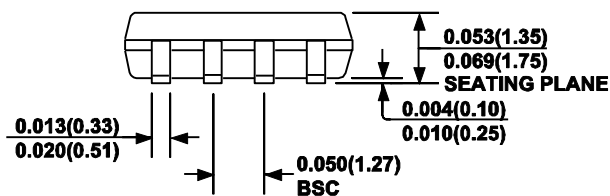
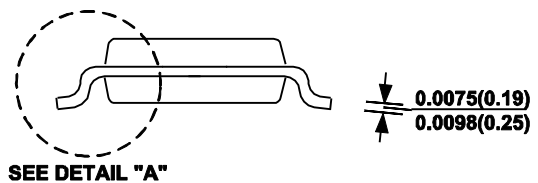
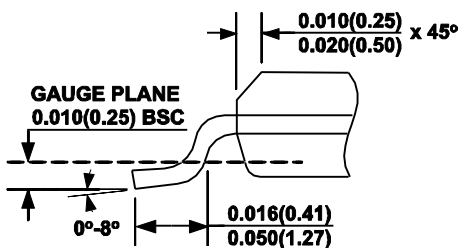
$$P_{on} = \frac{\pi}{2} \cdot I_{OUT} \cdot V_F \cdot f_{SW} \cdot t_{Don} \cdot \sin(2 \cdot f_{SW} \cdot t_{Don} \cdot \pi) \quad (6)$$

Figure 15 shows how different turn-on delay values affect efficiency, according to different output voltages. To keep the body diode conduction loss at a fairly low level (below 0.5% of the output power), the turn-on delay is recommended to be less than 5% of the switching cycle. For example, in a  $f_{SW} = 200\text{kHz}$  LLC system, the switching cycle is  $\sim 5\mu\text{s}$ . It is recommended to select a MOSFET that makes  $t_{Don} < 250\text{ns}$ .



**Figure 15: Turn-On Delay vs. Power Loss**

The turn-off delay ( $t_{Doff}$ ) is critical in some fast transient CCM applications. It is recommended to choose the MOSFET that makes  $t_{Doff}$  remain below the CCM current transient duration. Otherwise, the MOSFET may need to be selected with a lower  $Q_g$ , or an external totem pole driver circuit can be added to prevent shoot-through.

**PACKAGE INFORMATION**
**SOIC-8**

**TOP VIEW**

**RECOMMENDED LAND PATTERN**

**FRONT VIEW**

**SIDE VIEW**

**DETAIL "A"**
**NOTE:**

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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