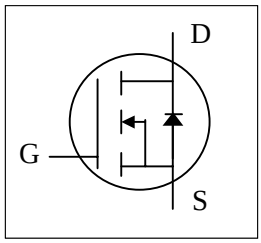
XP6NA3R0H

Halogen-Free Product

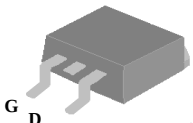
N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- **100% R_g & UIS Test**
- **Simple Drive Requirement**
- **Low On-resistance**
- **RoHS Compliant & Halogen-Free**



BV_{DSS}	60V
$R_{DS(ON)}$	3mΩ



TO-252(H)

Description

XP6NA3R0 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-252 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance.

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[4](Silicon Limited)	126	A
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[4](Package Limited)	75	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V[4](Package Limited)	75	A
I_{DM}	Pulsed Drain Current[1]	400	A
P_D@T_C=25℃	Total Power Dissipation	83.3	W
P_D@T_A=25℃	Total Power Dissipation[3]	2	W
E_{AS}	Single Pulse Avalanche Energy[6]	173	mJ
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	1.5	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient (PCB mount)[3]	62.5	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	60	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=40A	-	-	3	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2	-	4	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=40A	-	100	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=48V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g	Total Gate Charge[5]	I_D=40A	-	70	112	nC
Q_{gs}	Gate-Source Charge[5]	V_{DS}=30V	-	22	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[5]	V_{GS}=10V	-	18	-	nC
$t_{d(on)}$	Turn-on Delay Time[5]	V_{DS}=30V	-	22	-	ns
t_r	Rise Time[5]	I_D=40A	-	75	-	ns
$t_{d(off)}$	Turn-off Delay Time[5]	R_G=7.5Ω	-	52	-	ns
t_f	Fall Time[5]	V_{GS}=10V	-	88	-	ns
C_{iss}	Input Capacitance[5]	V_{GS}=0V	-	4075	6520	pF
C_{oss}	Output Capacitance[5]	V_{DS}=50V	-	650	-	pF
C_{rss}	Reverse Transfer Capacitance[5]	f=1.0MHz	-	20	-	pF
R_g	Gate Resistance	f=1.0MHz	-	0.8	1.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=40A, V_{GS}=0V	-	-	1.3	V
t_{rr}	Reverse Recovery Time[5]	I_S=40A, V_{GS}=0V	-	45	-	ns
Q_{rr}	Reverse Recovery Charge[5]	dI/dt=100A/μs	-	45	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board

4.Package limitation current is 75A .

5.Guaranteed by design.

6.Starting T_j=25°C , V_{DD}=30V , L=0.3mH , R_G=25Ω , V_{GS}=10V

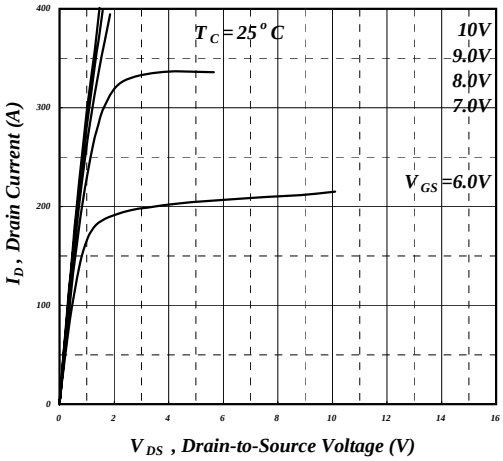


Fig 1. Typical Output Characteristics

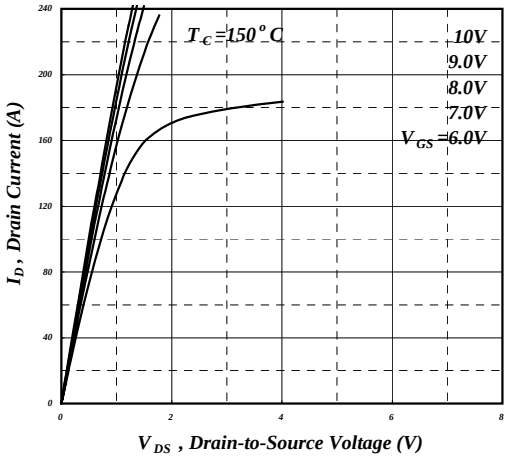


Fig 2. Typical Output Characteristics

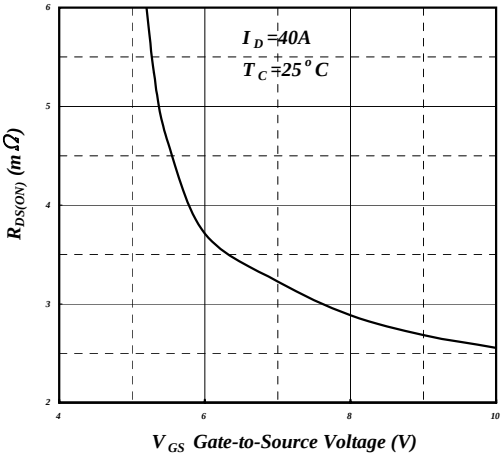


Fig 3. On-Resistance v.s. Gate Voltage

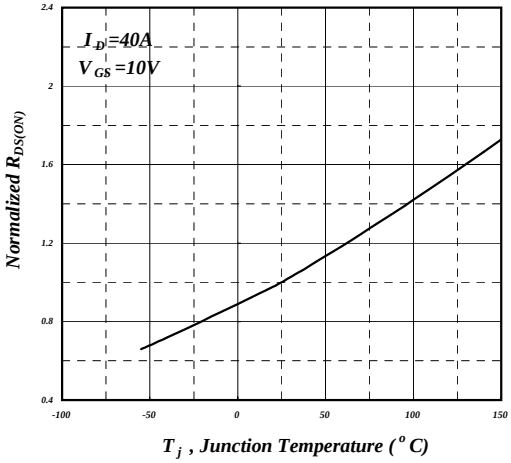


Fig 4. Normalized On-Resistance v.s. Junction Temperature

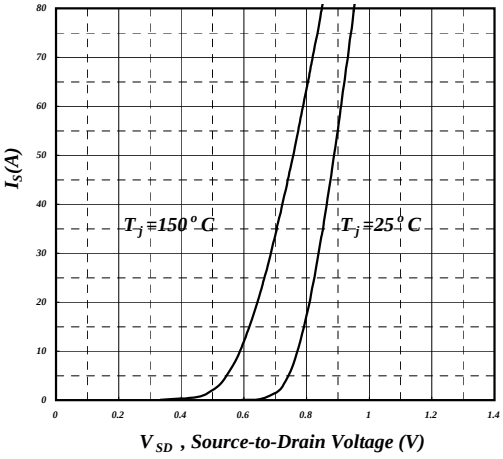


Fig 5. Forward Characteristic of Reverse Diode

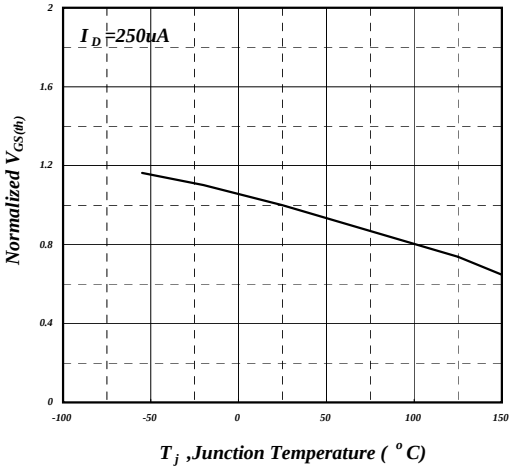


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

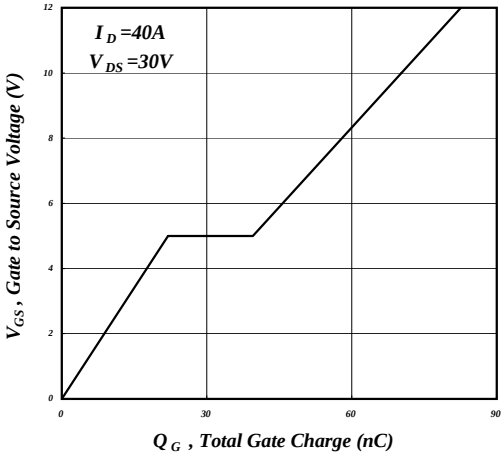


Fig 7. Gate Charge Characteristics

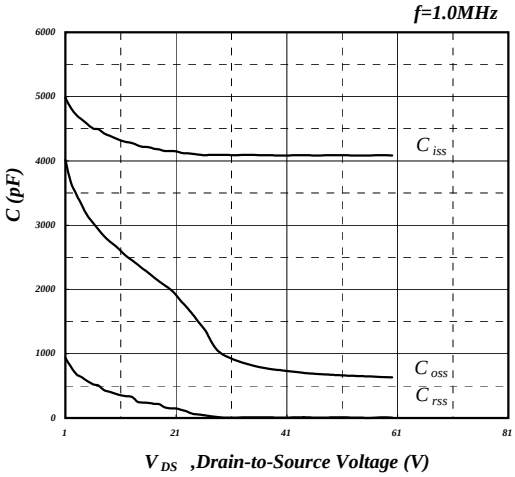


Fig 8. Typical Capacitance Characteristics

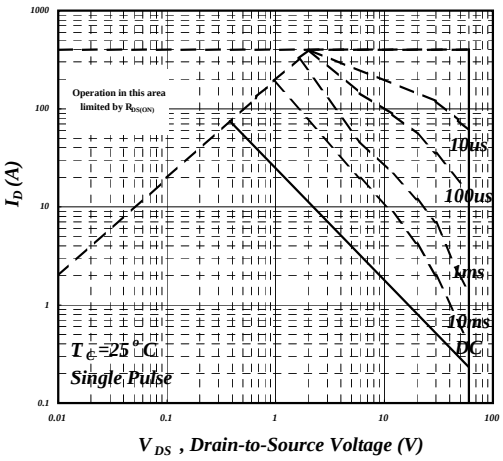


Fig 9. Maximum Safe Operating Area

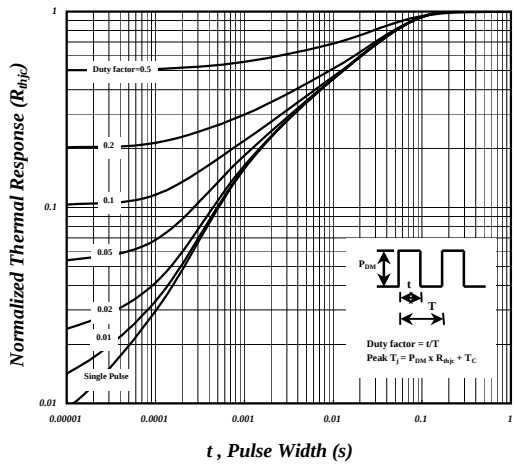


Fig 10. Effective Transient Thermal Impedance

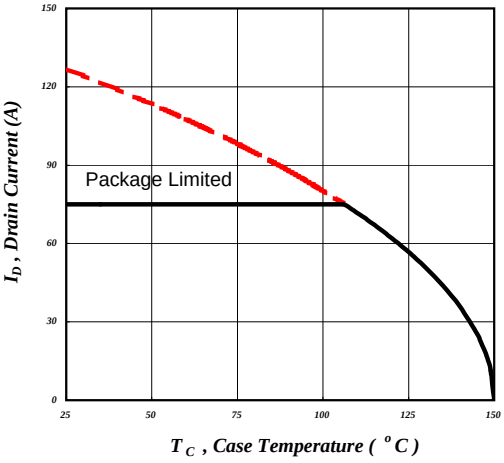


Fig 11. Drain Current v.s. Case Temperature

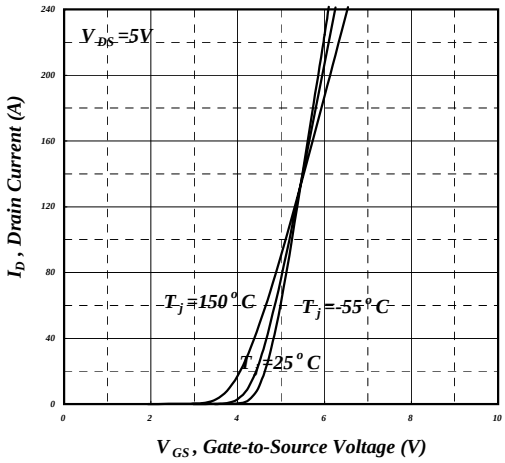


Fig 12. Transfer Characteristics

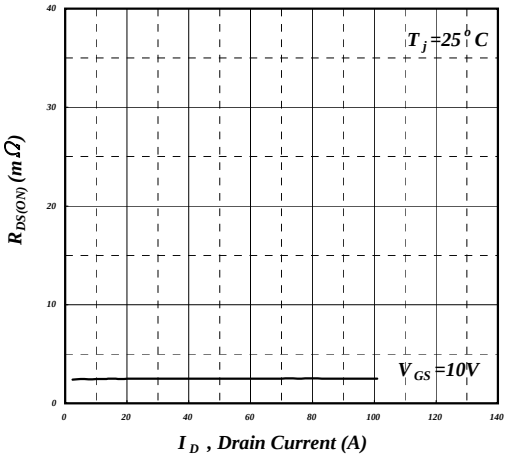


Fig 13. Typ. Drain-Source on State Resistance

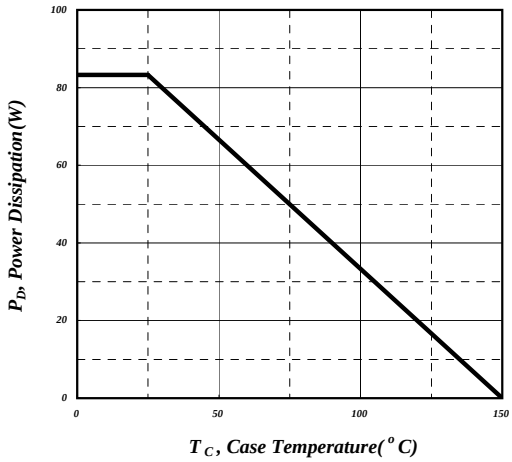


Fig 14. Total Power Dissipation

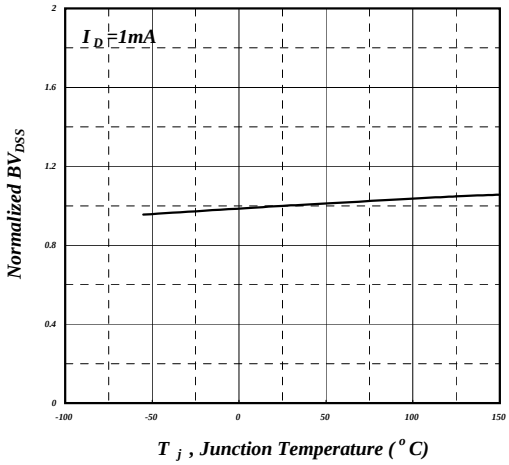


Fig 15. Normalized BV_{DSS} v.s. Junction Temperature

MARKING INFORMATION