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NTE7475
Integrated Circuit
TTL – 4–Bit Bistable Latch

Description:

The NTE7475 is a 4–bit bistable latch in a 16–Lead plastic DIP type package that is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The NTE74LS75 features complementary Q and $\overline{Q}$ outputs from a 4–bit latch and are completely compatible with all popular TTL families. All inputs are diode–clamped to minimize transmission–line effects and simplify system design.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Interemitter Voltage (Note 2) 5.5V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Voltage values are with respect to network ground terminal.
Note 2. This is the voltage between two emitters of a multiple–emitter input transistor.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Output Current	I_{OH}	–	–	–400	μA
Low–Level Output Current	I_{OL}	–	–	16	mA
Width of Enabling Pulse	t_w	20	–	–	ns
Setup Time	t_{su}	20	–	–	ns
Hold Time	t_h	5	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 3, Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2	–	–	V
Low Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −400μA	2.4	3.4		V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current D Input	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	80	μA
C Input			–	–	160	μA
Low Level Input Current D Input	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−3.2	mA
C Input			–	–	−6.4	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 5	−18	–	−57	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 6	–	32	63	mA

Note 3. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 4. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 5. Not more than one output should be shorted at a time.

Note 6. I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From D input to Q Output)	t_{PLH}	R_L = 400Ω, C_L = 15pF	–	16	30	ns
	t_{PHL}		–	14	25	ns
Propagation Delay Time (From D input to $\overline{Q}$ Output)	t_{PLH}		–	24	40	ns
	t_{PHL}		–	7	15	ns
Propagation Delay Time (From C input to Q Output)	t_{PLH}		–	16	30	ns
	t_{PHL}		–	7	15	ns
Propagation Delay Time (From C input to $\overline{Q}$ Output)	t_{PLH}		–	16	30	ns
	t_{PHL}		–	7	15	ns

Function Tables:

Inputs		Outputs	
D	**C**	**Q**	**$\overline{Q}$**
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = HIGH Level, L = LOW Level, X = Irrelevant

Q_0 = The level of Q before the high−to−low transition of G

Pin Connection Diagram