*Click here to ask about the production status of specific part numbers.*

# MAX77839

# 5.5V Input, 4.4A/3.6A Switching Current 6µA $I_Q$ Buck-Boost Converter

## General Description

The MAX77839 is a highly-efficient buck-boost regulator with an industry leading quiescent current of 6µA targeted for one-cell Li-ion and down to any battery chemistry with 1.8V discharge voltage. It supports input voltages of 1.8V to 5.5V and an output voltage range of 2.3V to 5.3V. The IC provides two different switching current limits to optimize external component sizing based on given load current requirements. The MAX77839 supports two different switching current options ("A" and "B" = 4.4A (typ), "C" and "D" = 3.6A (typ)), and two different GPIO pin configurations ("A" and "C" = FPWM pin,"B" and "D" = POK pin). These options provide design flexibility that allow the IC to cover a wide range of applications and use cases while minimizing board space.

The IC features a single-resistor adjustable output voltage from 2.3V to 5.3V. A configurable GPIO pin allows to select either a FPWM mode control input or a $\overline{POK}$ open drain output, depending on the system requirements. Maxim's unique buck-boost controller technology provides high efficiency, excellent load and line transient response, and a seamless transition between buck and boost modes of operation.

The MAX77839 is available in either a 2.07mm x 1.51mm, 15-bump wafer-level package (WLP), and a 2.5mm x 2.0mm, 11-lead FC2QFN package.

## Applications

- Asset Tracking/Fleet Management
- 5G/2G/GSM Cellular Power
- RF Amplifier
- Smartphones ToF/Facial and Gesture Recognition
- System Power Pre-Regulation
- Single-Cell Li-ion Battery Powered Devices

## Benefits and Features

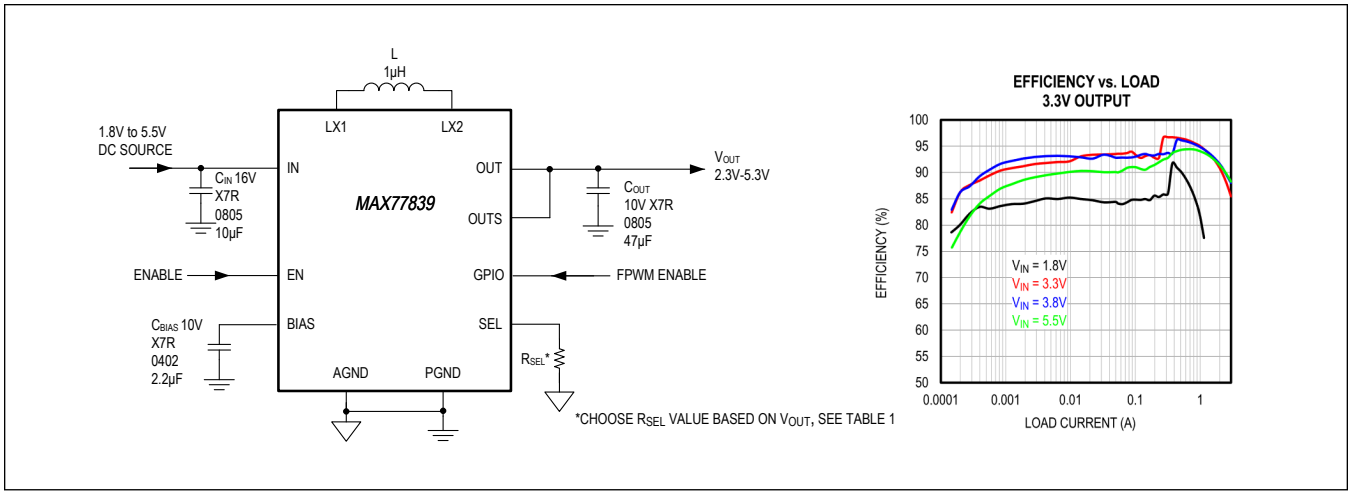
- Flexible System Integration
  - 1.8V to 5.5V Input Voltage Range
  - 2.3V to 5.3V Single Resistor Adjustable Output
  - 3.6A $I_{LIM}$ ("C" and "D" options) or 4.4A $I_{LIM}$ ("A" and "B" options)
  - 3A Maximum Output Current (4.4A $I_{LIM}$, Buck Mode)
  - 3A Maximum Output Current (4.4A $I_{LIM}$, Boost Mode $3.0V_{IN}$, $3.3V_{OUT}$)
  - 96% Peak Efficiency ($V_{IN}$ = 3.6V, $V_{OUT}$ = 3.3V)
  - Optional GPIO Pin (FPWM input, $\overline{POK}$ output)
- Low Supply Current that Extends Battery Life
  - Skip Mode that Reduces Supply Current at Light Loads
  - 6µA Ultra-Low $I_Q$
- 2.2MHz (typ) Switching Frequency
- Integrated Protections that Provide System Robustness
  - Undervoltage Lockout (UVLO)
  - Overvoltage Protection (OVP)
  - Cycle-by-Cycle Inductor Peak Current Limit
  - Thermal Shutdown ($T_{SHDN}$)
- Active Output Discharge
- Small Solution Size
  - 2.07mm x 1.51mm, 0.4mm pitch, 15-bump WLP
  - 2.5mm x 2.0mm, 0.5mm pitch, 11-pin FC2QFN

***Ordering Information appears at end of data sheet.***

*19-100983; Rev 0; 12/20*

maxim integrated™

## Simplified Block Diagram



## Absolute Maximum Ratings

IN, OUT, LX1, LX2, OUTS, BIAS to PGND, AGND . -0.3V to +6V
PGND to AGND ..... -0.3V to +0.3V
EN, GPIO, SEL to AGND .....-0.3V to $V_{BIAS}$ + 0.3V

Continuous Power Dissipation
15-WLP Package ($T_A$ = +70°C, derate 16.22mW/°C above +70°C (Note 1)).....1297.6mW

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC speficiation JESD51-7, using a four -layer board. For detailed information on pacakge thermal considerations, refer *www.maximintegrated.com/thermal-tutorial*.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Recommended Operating Conditions

| PARAMETER | SYMBOL | CONDITION | TYPICAL RANGE | UNIT |
|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | | 1.8 to 5.5 | V |
| Output Voltage | $V_{OUT}$ | | 2.3 to 5.3 | V |
| Output Current Range | $I_{OUT}$ | For continuous operation at 3A, the junction temperature ($T_J$) is limited to +105ºC. If the junction temperature is higher than +105ºC, the expected lifetime at 3A continuous operation is derated. Boost mode operation is also limited by $I_{LIM}$. | 0 to 3 | A |
| Operating Juction Temperature | $T_J$ | | -40 to +125 | ºC |

**Note:** These limits are not guaranteed.

## Package Information

### WLP

| | |
|---|---|
| Package Code | W151K2Z+1 |
| Outline Number | 21-100441 |
| Land Pattern Number | Refer to *Application Note 1891* |
| **Thermal Resistance, Four Layer Board:** | |
| Junction-to-Ambient ($\theta_{JA}$) | 61.65C°/W |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | 14.31C°/W |

### FC2QFN

| | |
|---|---|
| Package Code | F112A2F+1 |
| Outline Number | 21-100431 |
| Land Pattern Number | 90-100154 |
| **Thermal Resistance, Four Layer Board:** | |
| Junction-to-Ambient ($\theta_{JA}$) | N/A |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | N/A |

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

## Electrical Characteristics

($T_A \approx T_J$ = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, $V_{IN}$ = +3.8V, $R_{SEL}$ = Short to AGND, GPIO = Low (for A, C options), GPIO = Pull up to $V_{IN}$ with 15kΩ resistor (for B, D options) unless otherwise noted. (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT VOLTAGE AND SUPPLY CURRENT** | | | | | | |
| Operating Input Voltage | $V_{IN}$ | | 1.8 | | 5.5 | V |
| Input Undervoltage Lockout (UVLO) Voltage | $V_{UVLO\_Rising}$ | Input rising | 1.70 | 1.75 | 1.80 | V |
| Input Undervoltage Lockout (UVLO) Hysteresis | $V_{UVLO\_Hys}$ | | | 70 | | mV |
| Shutdown Supply Current | $I_{SHDN}$ | EN = low, $T_J$ = -40ºC to +85ºC | | | 2 | µA |
| Input Quiescent Current | $I_Q$ | EN = high, FPWM = low, $T_J$ = -40ºC to +125ºC, no switching | | 6 | 14 | µA |
| | $I_{Q\_FPWM}$ | EN = high, FPWM = high, $T_J$ = -40ºC to +125ºC, no switching | | 3 | | mA |
| Turn-On Delay Time | $t_{DLY\_ON}$ | From EN high to $R_{SEL}$ reading | | 100 | | µs |
| $R_{SEL}$ Reading Time | $t_{RSEL}$ | | 360 | 450 | 600 | µs |
| **BUCK-BOOST CONVERTER** | | | | | | |
| Output Voltage Range | $V_{OUT}$ | See *$R_{SEL}$ table* | 2.3 | | 5.3 | V |
| Output Voltage Accuracy | $V_{OUT\_ACC}$ | FPWM = high, $T_J$ = +25ºC, no load | -1.0 | | +1.0 | % |
| | | FPWM = low, $T_J$ = +25ºC, no load | -1.0 | | +3.5 | |
| Switching Frequency | $f_{SW}$ | | 1.936 | 2.20 | 2.464 | MHz |
| High-Side Switching Current Limit | $I_{LIM}$ | A, B options | 4.05 | 4.4 | 4.75 | A |
| | | C, D options | 3.24 | 3.6 | 3.96 | |
| High-Side Switching Current Limit During Soft-Start | $I_{LIM\_SS}$ | A, B options | 1.75 | 2.1 | 2.45 | A |
| | | C, D options | 1.28 | 1.6 | 1.92 | |
| Low-Side Switch On Resistance | $R_{DSON\_LO}$ | LX1, LX2 | | 58 | | mΩ |
| High-Side Switch On Resistance | $R_{DSON\_HI}$ | LX1, LX2 | | 50 | | mΩ |
| Thermal Shutdown Threshold | $T_{SHDN}$ | $T_J$ rising | | 150 | | ºC |
| Thermal Shutdown Hysteresis | $T_{SHDN\_HYS}$ | | | 15 | | ºC |
| Active Discharge Resistance | $R_{DSCHG}$ | | | 100 | | Ω |
| Line Regulation | $\Delta V_{OUT}/\Delta V_{IN}$ | $V_{IN}$ = 1.8V to 5.5V, FPWM = high, no load, $V_{OUT}$ = 3.3V, 5V | -0.3 | | +0.3 | %/V |
| Load Regulation | $\Delta V_{OUT}/\Delta I_{OUT}$ | $I_{OUT}$ = 0A to full load, $V_{IN}$ = 2.3V, 3.8V, 5.5V, $V_{OUT}$ = 3.3V, 3.6V, 5V | | ±0.3 | | %/A |
| Soft-Start Timeout | $t_{SS}$ | | | 4 | | ms |
| Overvoltage Protection Threshold | $V_{OVP}$ | $V_{OUT}$ - $V_{OUTS}$ | | 0.5 | | V |

## Electrical Characteristics (continued)

($T_A \approx T_J$ = -40°C to +125°C, typical values are at $T_A \approx T_J$ = +25°C, $V_{IN}$ = +3.8V, $R_{SEL}$ = Short to AGND, GPIO = Low (for A, C options), GPIO = Pull up to $V_{IN}$ with 15kΩ resistor (for B, D options) unless otherwise noted. (Note 2)

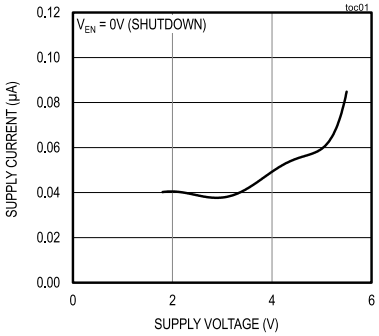
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DIGITAL LOGIC (EN, GPIO)** | | | | | | |
| Input Logic-Low Level | $V_{IL}$ | | | | 0.4 | V |
| Input Logic-High Level | $V_{IH}$ | | 1.3 | | | V |
| Internal Pulldown Resistance | $R_{PD}$ | EN, GPIO (A, C options) | | 800 | | kΩ |
| Output Logic-Low Level | $V_{OL}$ | GPIO pin (B, D options), pullup voltage = 3.3V, $I_{OL}$ = 1mA | | | 0.4 | V |

**Note 2:** Limits are 100% production tested at $T_A \approx T_J$ = +25ºC. The MAX77839 is tested under pulsed load conditions such that $T_A \approx T_J$. Limits over the operating temperature range ($T_J$ = -40ºC to +125ºC) are guaranteed by design and characterization using statistical process control methods.

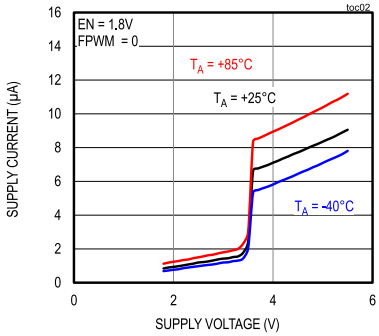
## Typical Operating Characteristics

($V_{IN}$ = 3.8V, $V_{OUT}$ = 3.3V, L = 1µH (Coilcraft XAL4020-102ME), Skip Mode, $I_{LIM\_LX}$ = 4.4A, $T_A$ = +25°C, unless otherwise noted.)

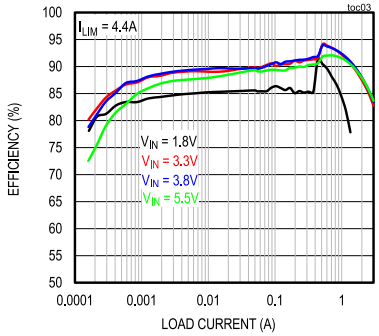
SHUTDOWN CURRENT 3.3V OUTPUT



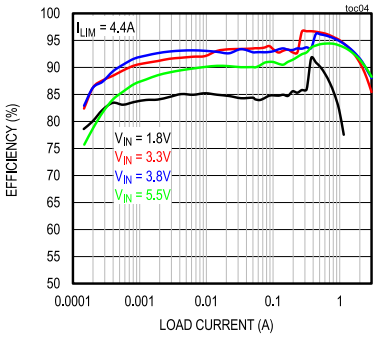

QUIESCENT CURRENT 3.3V OUTPUT



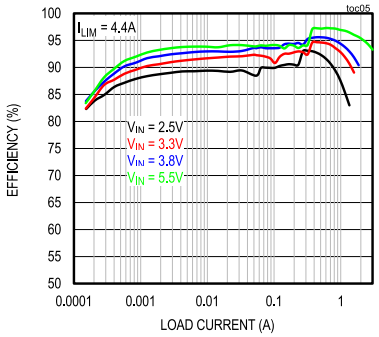

EFFICIENCY vs. LOAD 2.3V OUTPUT



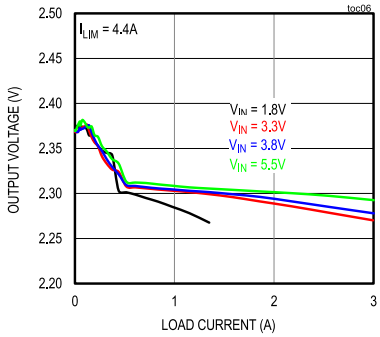

EFFICIENCY vs. LOAD 3.3V OUTPUT



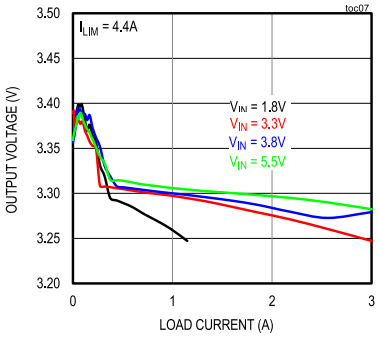

EFFICIENCY vs. LOAD 5.3V OUTPUT



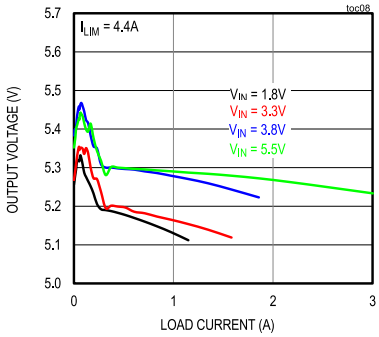

LOAD REGULATION 2.3V OUTPUT



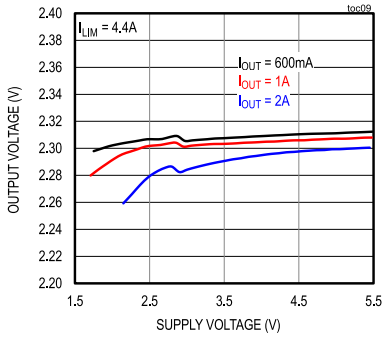

LOAD REGULATION 3.3V OUTPUT




LOAD REGULATION 5.3V OUTPUT



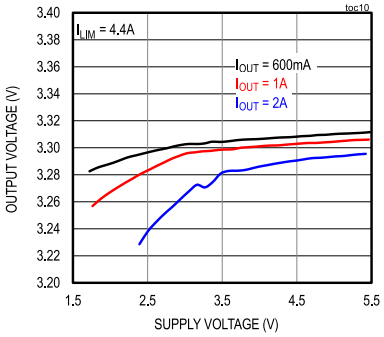

LINE REGULATION 2.3V OUTPUT



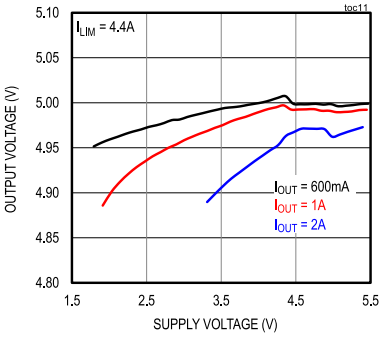
## Typical Operating Characteristics (continued)

($V_{IN}$ = 3.8V, $V_{OUT}$ = 3.3V, L = 1µH (Coilcraft XAL4020-102ME), Skip Mode, $I_{LIM\_LX}$ = 4.4A, $T_A$ = +25°C, unless otherwise noted.)

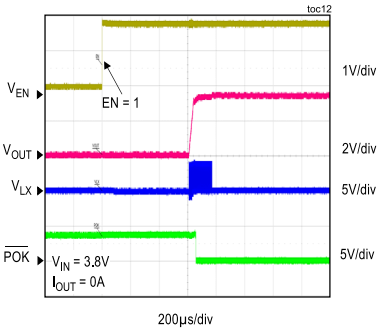
LINE REGULATION
3.3V OUTPUT



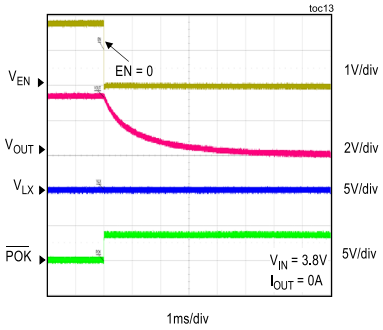

LINE REGULATION
5.0V OUTPUT



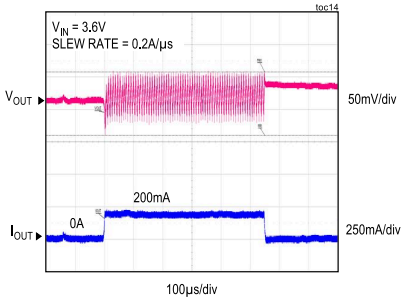

ENABLE STARTUP WAVEFORM
3.3V OUTPUT



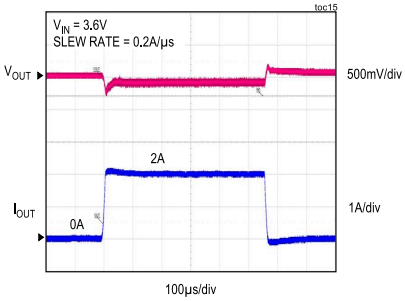

ENABLE SHUTDOWN WAVEFORM
3.3V OUTPUT



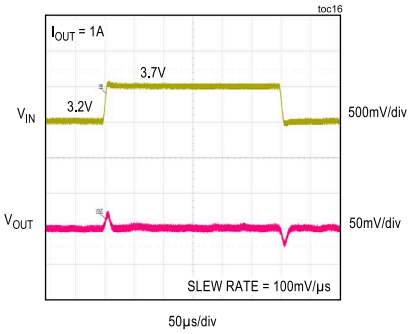

LOAD TRANSIENT RESPONSE
3.8V OUTPUT



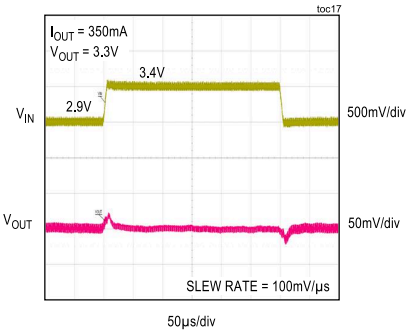

LOAD TRANSIENT RESPONSE
3.8V OUTPUT



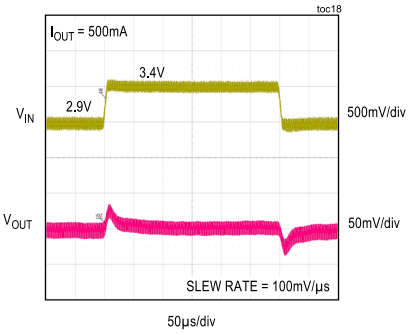

LINE TRANSIENT RESPONSE
2.3V OUTPUT




BOOST TO BUCK
LINE TRANSIENT RESPONSE



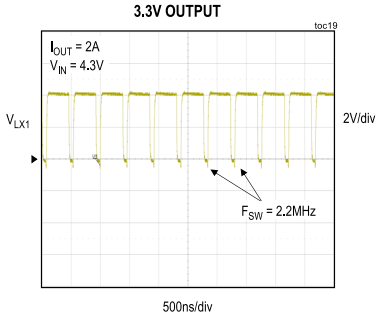

LINE TRANSIENT RESPONSE
5V OUTPUT



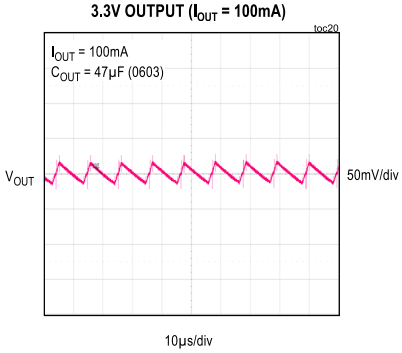
## Typical Operating Characteristics (continued)

($V_{IN}$ = 3.8V, $V_{OUT}$ = 3.3V, L = 1µH (Coilcraft XAL4020-102ME), Skip Mode, $I_{LIM\_LX}$ = 4.4A, $T_A$ = +25°C, unless otherwise noted.)

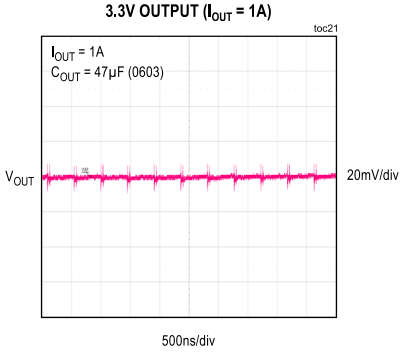
SWITCHING WAVEFORM
3.3V OUTPUT



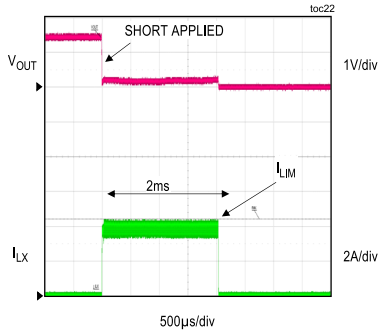

OUTPUT RIPPLE IN SKIP MODE
3.3V OUTPUT ($I_{OUT}$ = 100mA)



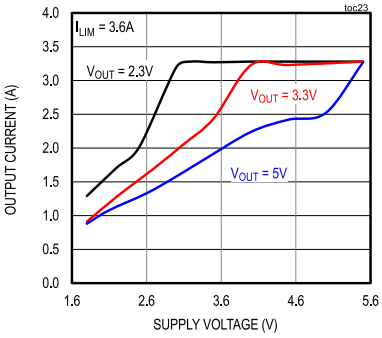

OUTPUT RIPPLE IN PWM
3.3V OUTPUT ($I_{OUT}$ = 1A)



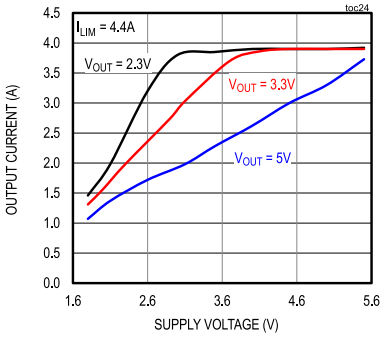

SHORT-CIRCUIT RESPONSE
3.3V OUTPUT ($I_{LIM}$ = 4.4A)




MAXIMUM OUTPUT CURRENT vs.
SUPPLY VOLTAGE



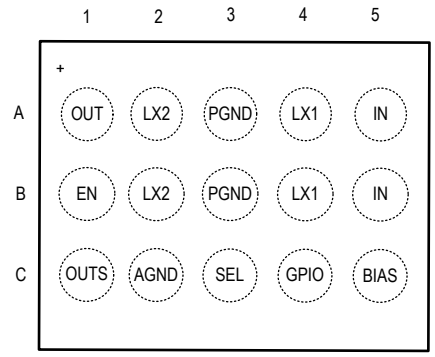

MAXIMUM OUTPUT CURRENT vs.
SUPPLY VOLTAGE



## Pin Configurations

### WLP

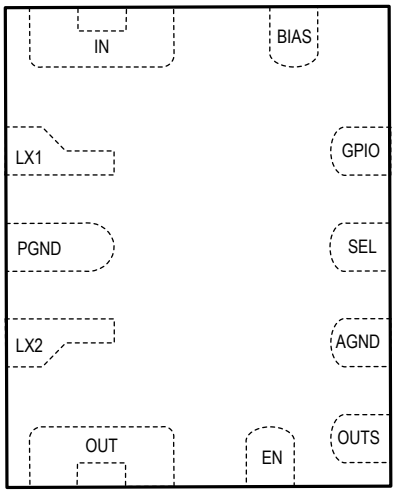
TOP VIEW
(BUMP SIDE DOWN)




15-BUMP WLP, 0.4mm PITCH

### FC2QFN

TOP VIEW
(LEAD SIDE DOWN)



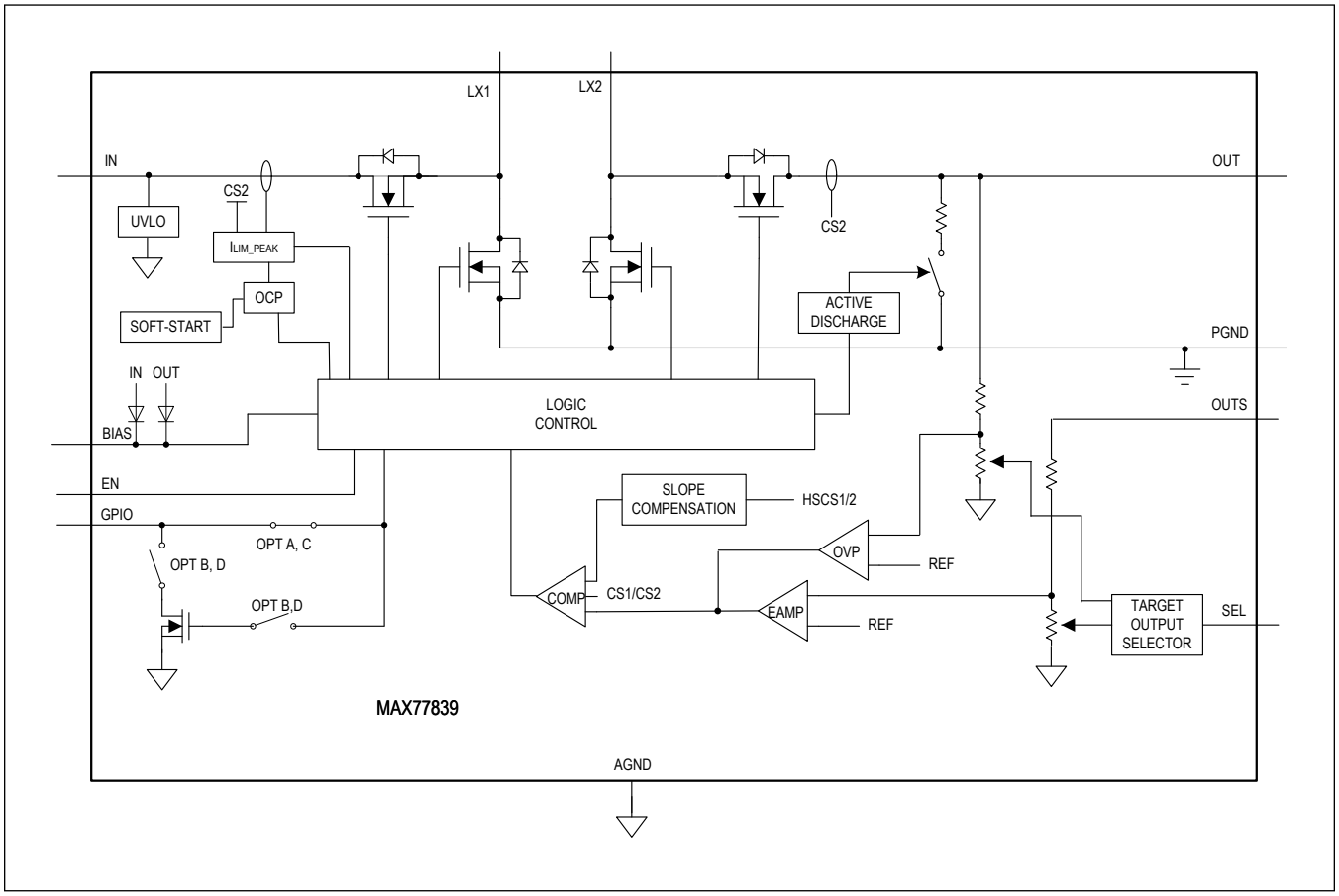

11-LEAD FC2QFN, 0.5mm PITCH

## Pin Description

| PIN | | NAME | FUNCTION | TYPE |
|---|---|---|---|---|
| WLP | FC2QFN | | | |
| A5, B5 | 11 | IN | Buck-Boost Input. Bypass to PGND with two 16V 10µF X7R ceramic capacitors. | Analog |
| C5 | 10 | BIAS | Internal Bias Supply. Bypass to AGND with a 10V 2.2µF X7R ceramic capacitor. Do not load this pin externally. | Power Output |
| A4, B4 | 1 | LX1 | Input-Side Buck-Boost Switching Node | Power |
| C4 | 9 | GPIO | GPIO pin.<br><br>For A, C options, forced-PWM mode digital input. Apply high for FPWM mode, apply low for auto skip mode operation.<br><br>For B, D options, $\overline{POK}$ open drain output. Pull up with 15kΩ resistor to IO voltage. | Digital Input/ Output |
| A3, B3 | 2 | PGND | Power Ground | Ground |
| C3 | 8 | SEL | Output Voltage Selection Input. Connect a resistor between this pin and ground to configure the output voltage. Consult *Output Voltage Configuration* for a table of recommended resistors and corresponding output voltages. | Analog |
| A2, B2 | 3 | LX2 | Output-Side Buck-Boost Switching Node | Power |
| C2 | 7 | AGND | Analog Ground | Ground |
| A1 | 4 | OUT | Buck-Boost Power Output. Bypass to PGND with two 16V X7R 10µF ceramic capacitors. | Power |
| B1 | 5 | EN | Buck-Boost Enable Input | Digital Input |
| C1 | 6 | OUTS | Buck-Boost Output Voltage Sense Input. Connect to the output at the point-of-load. | Analog |

## Functional Diagrams

### Functional Block Diagram



## Detailed Description

The MAX77839 is a simple, high-efficiency buck-boost regulator with a wide input voltage range for single cell Li-ion batteries, two cell AA batteries, LiSOCI2 batteries, or any battery chemistry with a 1.8V discharge voltage. The converter seamlessly transitions between buck and boost modes of operation. It includes two GPIO options for FPWM enable (options A and C) or $\overline{POK}$ open drain output (options B and D). The MAX77839 is also equipped with active output discharge, selection of two different inductor peak current limits, and various protections to ensure robustness in harsh operating conditions. The IC is available in WLP and FC2QFN packages.

### Startup and Shutdown

#### Startup

When the EN pin is set to high, the IC turns on the internal bias circuitry which takes typically 100µs ($t_{ON\_DLY}$) to settle. After the internal bias circuitry is settled, the controller senses the SEL pin resistance to set the reference voltage. The $R_{SEL}$ reading takes about 450µs ($t_{RSEL}$). After the IC reads the $R_{SEL}$ value, it begins the soft-start process.

To limit the inrush current during soft-start, the MAX77839 reduces the switching current limit level to about half of the normal level. Soft-start time ends when the output voltage reaches the target regulation point, increasing the switching current limit level to the normal level. After an additional 100µs of transition time, the MAX77839 switches over to normal switching control (Skip mode). Note that the part switches in FPWM for the entire duration of $t_{SS}$.

The MAX77839 is equipped with a soft-start time out timer ($t_{SS}$ = 4ms (typ)), and if the output voltage does not reach the target regulation point (90% of $V_{TARGET}$), then the MAX77839 latches off and does not start up until EN or $V_{IN}$ is cycled.

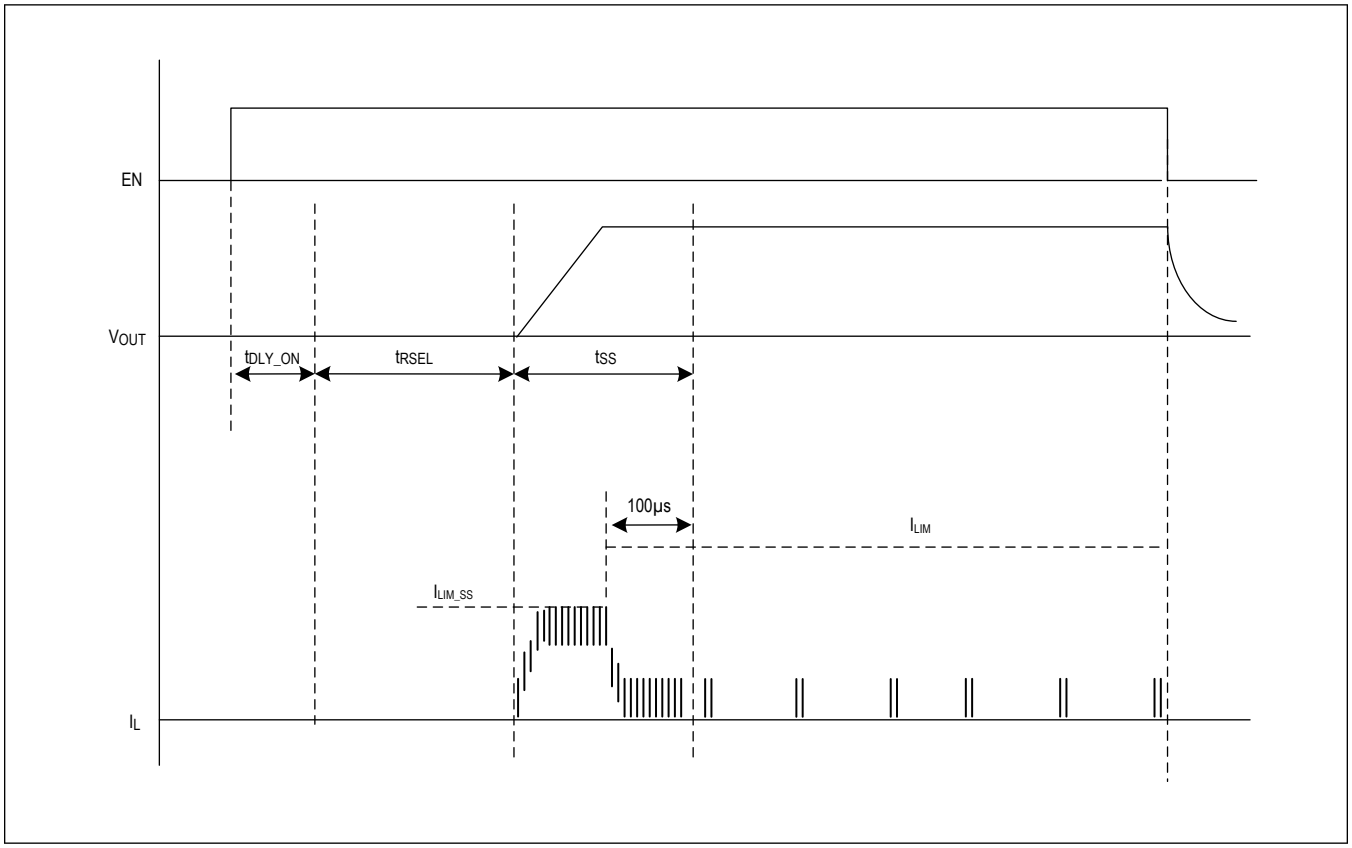



*Figure 1. Startup Waveform*

### Immediate Shutdown Conditions

The converter stops switching whenever the MAX77839 is disabled by EN control or is latched off by protections. After the converter stops switching, the MAX77839 turns on the active discharge switch between OUT and PGND to quickly discharge the output capacitor.

There are also several conditions that cause latch off, regardless of EN state:

- Thermal shutdown ($T_{SHDN}$)
- Soft-start timeout ($T_{SS}$)
- Continuous $I_{LIM}$ events for about 2ms (typ)
- Undervoltage Lockout (UVLO)

The events in this category shutdown the output. The converter can start up again once fault conditions are removed from the system and VIN or EN is toggled.

## Protections

### Thermal Shutdown

The device has an internal thermal-protection circuit which monitors die temperature. The buck-boost disables if the die temperature exceeds $T_{SHDN}$ (+150°C typ). The buck-boost enables again after the die temperature cools by approximately +15°C.

### Undervoltage Lockout

The device supports a UVLO feature that prevents operation in abnormal input voltage conditions when $V_{IN}$ falls below the $V_{UVLO\_Falling}$ threshold. Regardless of the EN pin status, the device disables until the input voltage $V_{IN}$ rises above the $V_{UVLO\_Rising}$ threshold.

### Overcurrent Protection

The device features a robust switching current-limit scheme that protects the device and the inductor during overload and fast transient conditions. The current-sense circuit takes current information from the high-side MOSFETs to determine the peak-switching current ($R_{DS(ON)}$ x $I_L$).

The IC provides two different cycle-by-cycle current limit levels (3.6A (typ) and 4.4A (typ)) for the high-side MOSFET. If the switching current ($I_{LIM}$) hits current limit for about 2ms, the IC shuts off the output.

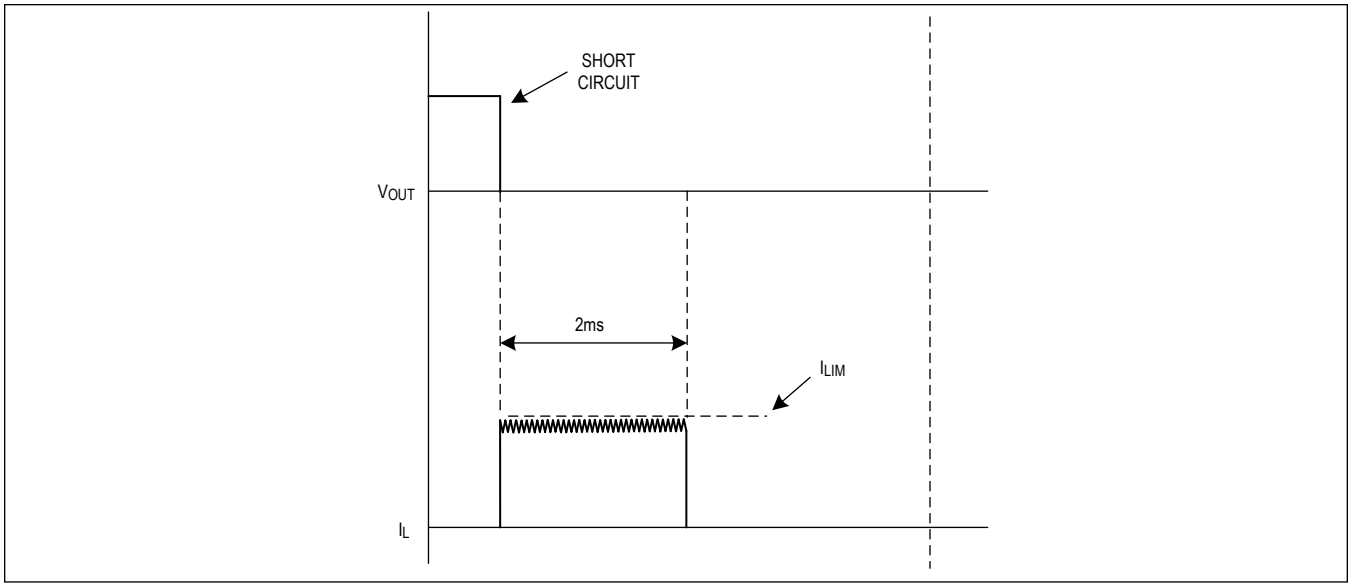



*Figure 2. Short-Circuit Waveform*

### Overvoltage Protection

The IC detects the voltage difference between OUT and OUTS, and if the voltage difference (OUT - OUTS) exceeds the OVP threshold voltage level (0.5V typ), then the device turns off all switches. This prevents OUTS = OPEN conditions from overdriving the output beyond safe operating ranges. Additionally, the device shuts off whenever OUTS detects a voltage over 20% of the target output value (10% when OUT target set above 5V).

## Control Scheme

The MAX77839 utilizes a four-switch H-bridge architecture to realize both buck and boost operating modes. It regulates the output voltage to a target value at any valid input voltage and provides great response to both line and load transient events. Fast switching frequency and a unique control algorithm allow for small external components, low output noise, and high-efficiency across the entire operating range.

The buck-boost converter operates using a 2.2MHz fixed-frequency pulse width modulation (PWM) control scheme with current-mode compensation. The architecture integrates four FETs operating as switches: an input high-side FET (HS1), input low-side FET (LS1), output high-side FET (HS2), and output low-side FET (HS2). A proprietary algorithm controls these switches in four different phases:

- Phase 1 (Φ1): HS1 and LS2 switch on to store energy in the inductor by ramping up inductor current at a rate determined by the input voltage and the inductance: $\frac{dI_L}{dt} = \frac{V_{IN}}{L}$
- Phase 2 (Φ2): HS1 and HS2 switch on to either charge or discharge the inductor, depending on the difference between the input and output voltage. In boost mode, $V_{OUT} > V_{IN}$ and the inductor current ramps down. In buck mode, $V_{IN} > V_{OUT}$ and the inductor current ramps up: $\frac{dI_L}{dt} = \frac{V_{IN} - V_{OUT}}{L}$
- Phase 3 (Φ3): LS1 and HS2 switch on to discharge the inductor by ramping down inductor current at a rate determined by the output voltage and the inductance: $\frac{dI_L}{dt} = \frac{-V_{OUT}}{L}$
- Phase 4 (Φ4): LS1 and LS2 switch on to disconnect the inductor from output and input voltages

Soft-start utilizes Φ1 and Φ3 to ramp the output voltage up.

Boost mode (VIN < VOUT) utilizes Φ1 and Φ2 within a single clock period. See Figure 3 for a graphical representation.

Buck mode (VIN > VOUT) utilizes Φ2 and Φ3 within a single clock period. See Figure 3 for a graphical representation.

Skip mode is initiated by consequent zero crossings of high side (HS2) switching current. In skip mode, device switching is controlled by output voltage. The converter increases the target regulation point to VOUT_SKIP_H (about 3% higher than regulation target), and continues switching to ramp up the output voltage until the output voltage reaches VOUT_SKIP_H. When the output voltage reaches VOUT_SKIP_H, Φ4 discharges the inductor current until output voltage drops to VOUT_SKIP_L (about 1% higher than regulation target) level. This cycle continues until the output voltage does not reach the target level for six switching cycles.

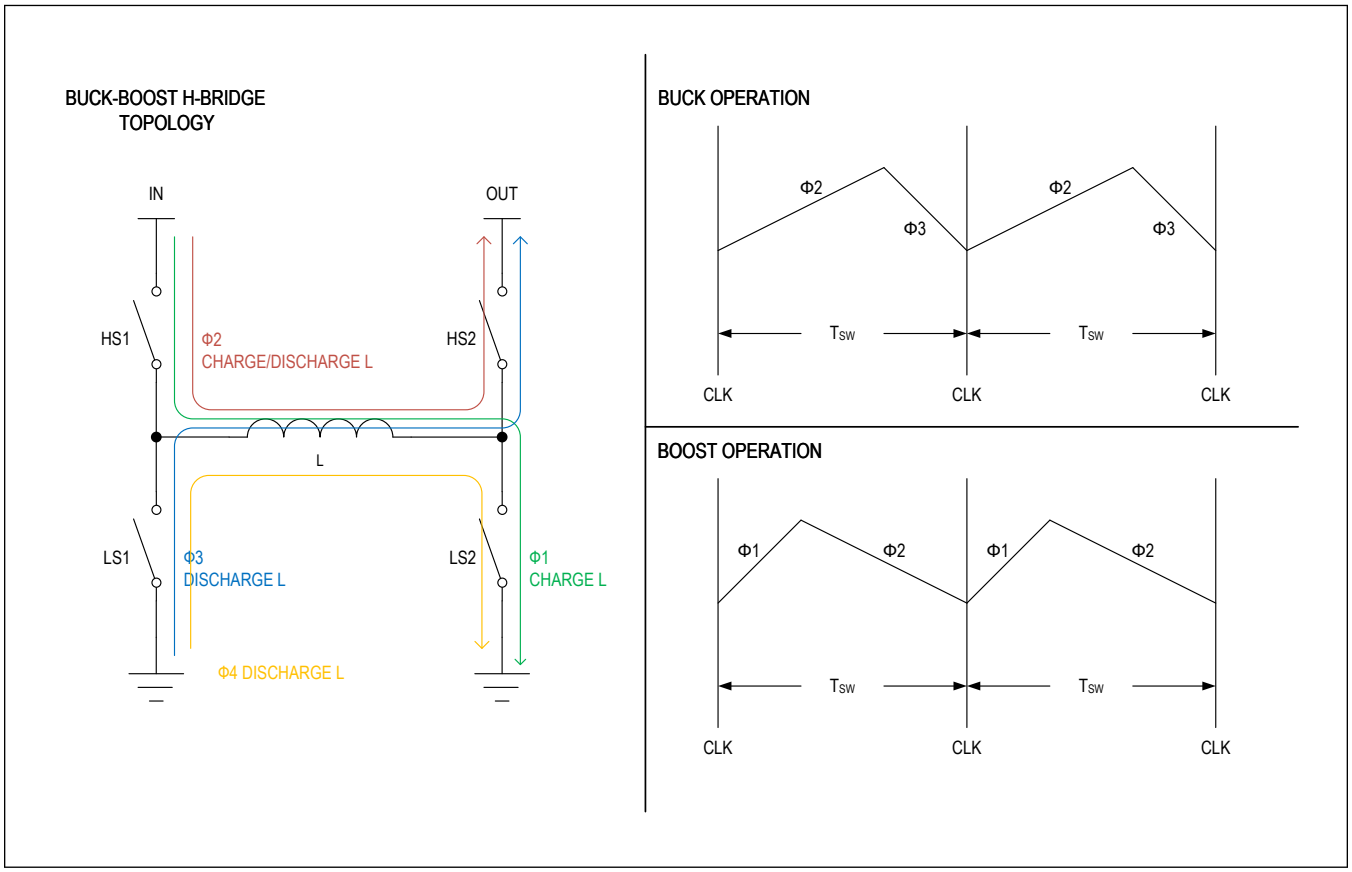



*Figure 3. Buck-Boost H-Bridge Topology*

## Output Voltage Configuration

Set the output voltage by connecting a resistor ($R_{SEL}$) to the SEL pin of the MAX77839. The device uses this resistance to calculate the target output voltage. Choose a resistor with 1% tolerance or better. Table 1 lists recommended values for $R_{SEL}$ to achieve different output voltages.

### Table 1. $R_{SEL}$ Selection Table

| $V_{OUT}$ (V) | $R_{SEL}$ (kΩ) |
|---|---|
| 3.3 | Short (0Ω) |
| 2.3 | 4.99 |
| 2.4 | 5.90 |
| 2.5 | 7.15 |
| 2.6 | 8.45 |
| 2.7 | 10.0 |

## Table 1. $R_{SEL}$ Selection Table (continued)

| $V_{OUT}$ (V) | $R_{SEL}$ (kΩ) |
|---|---|
| 2.8 | 11.8 |
| 2.9 | 14.0 |
| 3.0 | 16.9 |
| 3.1 | 20.0 |
| 3.2 | 23.7 |
| 3.4 | 28.0 |
| 3.5 | 34.0 |
| 3.6 | 40.2 |
| 3.7 | 47.5 |
| 3.8 | 56.2 |
| 3.9 | 66.5 |
| 4.0 | 80.6 |
| 4.1 | 95.3 |
| 4.2 | 113 |
| 4.3 | 133 |
| 4.4 | 162 |
| 4.5 | 191 |
| 4.6 | 226 |
| 4.7 | 267 |
| 4.8 | 324 |
| 4.9 | 383 |
| 5.0 | 452 |
| 5.1 | 536 |
| 5.2 | 634 |
| 5.3 | 768 |
| 2.85 | 909 or Open |

### Output Active Discharge

The buck-boost provides an internal 100Ω switch for the output active discharge function. The internal switch provides a path to discharge the energy stored in the output capacitor to PGND whenever the regulator is disabled by EN or any protections. While the regulator remains enabled, the internal switch is disconnected from the output.

### GPIO Pin

The MAX77839 includes two GPIO options which can be either a digital input pin for FPWM enable or an open drain output for $\overline{POK}$ signal. When FPWM is enabled, the converter operates in PWM mode regardless of load. When FPWM is disabled, the converter operates in auto skip mode and utilizes skip mode when it detects a zero crossing in switching current to reduce switching losses. Applications that require low output ripple and stiff transients at all conditions should consider the FPWM option. When the $\overline{POK}$ output pin is chosen as the GPIO option, the open drain output pin turns LOW if the output reaches within ±10% of the target voltage. Applications that require a POK signal for controlling the power-up sequence should consider the POK option.

## Applications Information

### Input Capacitor Selection

Bypass IN with a 10V, X7R, 10µF nominal input capacitor ($C_{IN}$). Larger values improve decoupling of the buck-boost regulator and filter the switching noise for the system. The maximum ripple current rating of the input capacitor needs to be higher than the maximum peak switching current in buck mode, otherwise, multiple capacitors need to be used.

### Output Capacitor Selection

The minimum effective capacitance of 4.7µF for the output capacitor is required for small output ripple and ensuring stable operation of the buck-boost regulator. Determine the expected effective $C_{OUT}$ carefully by considering the capacitor's initial tolerance, variation with temperature, and derating with DC bias voltage. The rated ripple current needs to be higher than the peak boost mode switching current, otherwise, multiple output capacitors need to be used.

A 10V, 22µF ceramic capacitor is recommended for most applications. Ceramic capacitors with X7R dielectrics are highly recommended for better effective capacitance, capacitance tolerance over bias voltage and temperature variations.

### Inductor Selection

The MAX77839's current sensing circuit and compensation loop is optimized for 1µH inductance. Choose an inductor with a saturation current that is greater than or equal to the maximum peak current limit setting ($I_{LIM}$), and an RMS current rating based off the expected continuous peak inductor current at given max load current. Lower DCR increases buck-boost efficiency. Recall that there are two different $I_{LIM}$ options for the MAX77839. Table 2 lists recommended inductors for each $I_{LIM}$ option. Note that this table was generated in 2019, and as inductor technology improves rapidly, may not be the most up-to-date at the time of reading.

## Table 2. Recommended Inductors

| MANUFACTURER | PART NUMBER | INDUC-TANCE (µH) | DC RESIS-TANCE (mΩ) | SATURATION CURRENT (A) | RMS CURRENT FOR 40ºC TEMPERATURE RISE (A) | DIMENSIONS L x W x H (mm) | OPTION |
|---|---|---|---|---|---|---|---|
| SAMSUNG | CIGT252010EH1R0MNE | 1.0 | 26 | 4.7 | 4.1 | 2.5 x 2.0 x 1.0 | B |
| Cyntec | HTEK20161T-1R0MSR | 1.0 | 35 | 4.2 | 4.1 | 2.0 x 1.6 x 1.0 | B |
| Coilcraft | XEL4020-102ME | 1.0 | 13.25 | 9.0 | 9.6 | 4.0 x 4.0 x 2.1 | A |

## PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. For the WLP package, a high density interconnect (HDI) PCB is not required. Figure 4 shows an example non-HDI PCB layout for the MAX77839 WLP package.

When designing the PCB, follow these guidelines:

1. Place the input capacitors $C_{IN}$ and output capacitors $C_{OUT}$ immediately next to the IN pin and OUT pin, respectively, of the IC. The trace between the capacitors' ground pin to the IC PGND pin needs to be routed through the component mounting layer to minimize trace parasitics. Additionally, the trace for these connections needs to be as short and wide as possible. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high voltage spikes and can damage the internal switching MOSFETs.
2. Place the inductor next to the LX bumps/pins (as close as possible), route inductor traces through vias, and make the traces between the LX bumps/pins and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer (as in the examples), make sure to include enough vias to minimize trace impedance. Routing LX traces on multiple layers is recommended to further reduce trace impedance. Furthermore, do not allow LX traces to take up an excessive amount of area. The voltage on this node switches very quickly and additional area creates more radiated emissions.
3. Prioritize the low-impedance ground plane of the PCB directly underneath the IC, $C_{OUT}$, $C_{IN}$, and the inductor. Cutting this ground plane risks interrupting the switching current loops.
4. AGND must carefully connect to PGND on the PCBs low-impedance ground plane. Connect AGND to the low-impedance ground plane on the PCB (the same net as PGND) away from any critical loops.
5. The IC requires a supply input (BIAS) which is often the same net as IN. Carefully bypass BIAS to PGND with a dedicated capacitor ($C_{BIAS}$) as close as possible to the IC. Route a dedicated trace between $C_{BIAS}$ and the BIAS bump/pin. Avoid connecting BIAS directly to the nearest IN bumps/pins without dedicated bypassing.
6. Connect the OUTS bump/pin to the regulating point with a dedicated trace away from noisy nets such as LX1 and LX2.
7. Keep the power traces and load connections short and wide. This is essential for high converter efficiency.
8. Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *Output Capacitor Selection* section and refer to *Tutorial 5527* for more information.

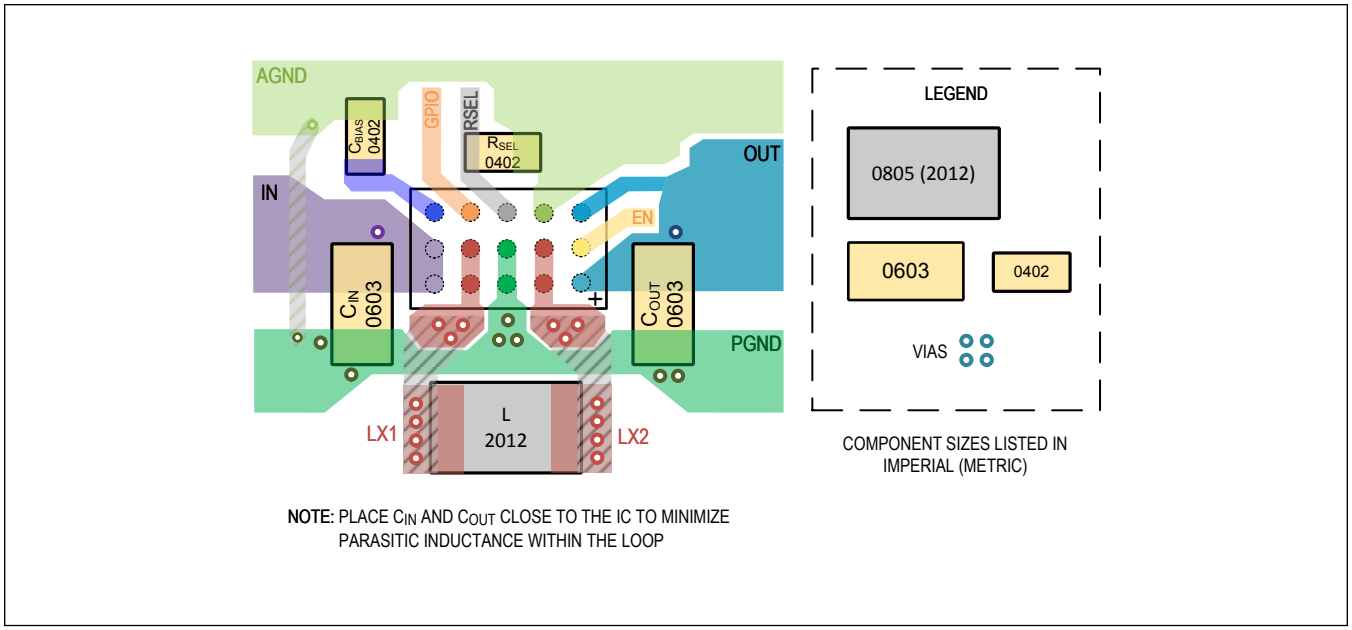



*Figure 4. PCB Layout Example (WLP)*

## Typical Application Circuits

### Typical Application Circuit

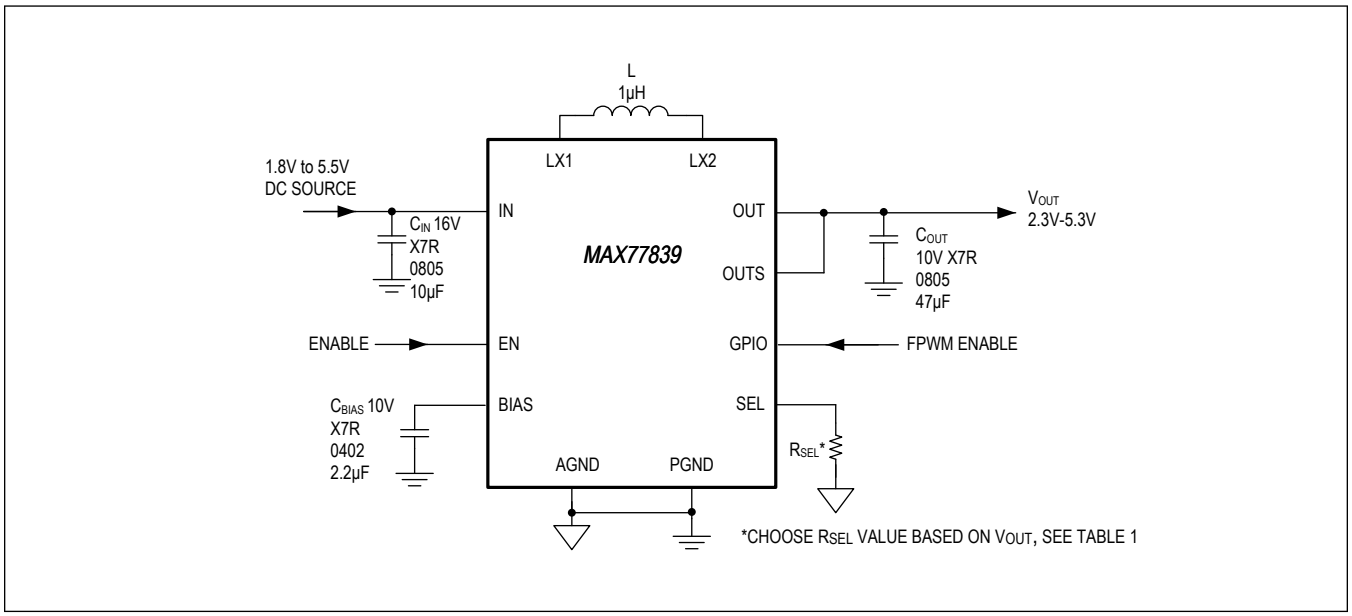



*Figure 5. Options A & C*

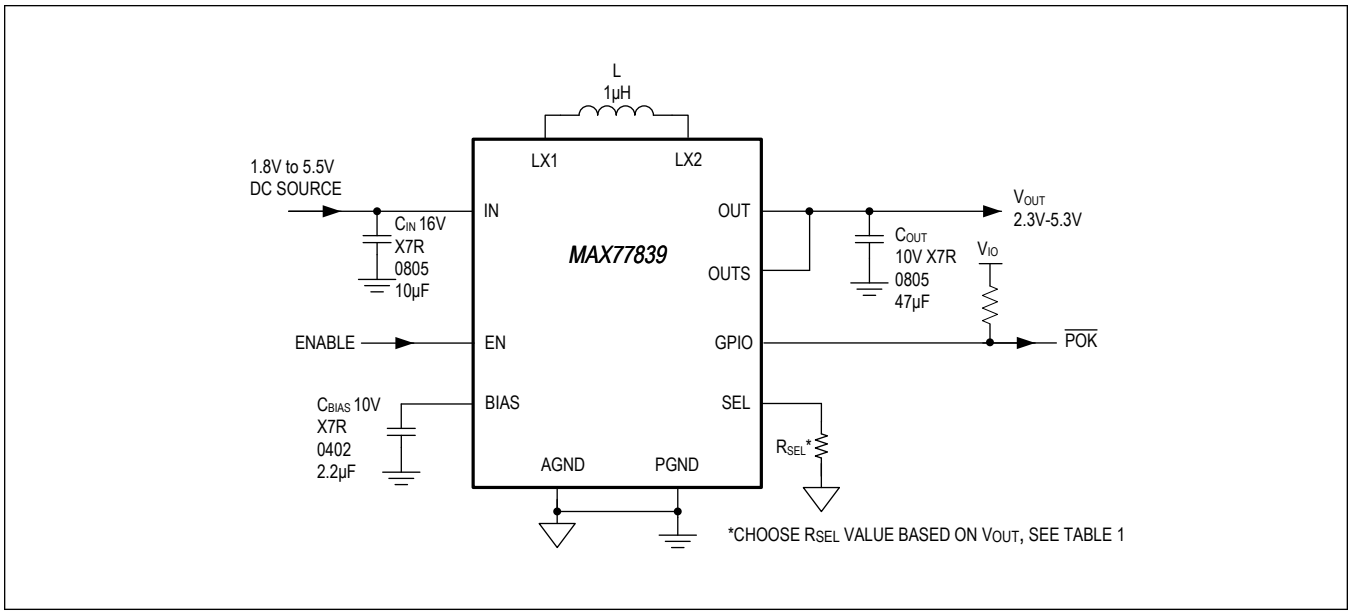



*Figure 6. Options B & D*

## Ordering Information

| PART NUMBER | $I_{LIM}$ OPTION (A) | GPIO FUNCTION | PIN-PACKAGE |
|---|---|---|---|
| MAX77839AEWL+T | 4.4 | FPWM | 15 WLP |
| MAX77839AEFQ+T* | | | 11 FC2QFN |
| MAX77839BEWL+T | | POK | 15 WLP |
| MAX77839BEFQ+T* | | | 11 FC2QFN |
| MAX77839CEWL+T | 3.6 | FPWM | 15 WLP |
| MAX77839CEFQ+T* | | | 11 FC2QFN |
| MAX77839DEWL+T | | POK | 15 WLP |
| MAX77839DEFQ+T* | | | 11 FC2QFN |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

*T = Tape and reel.*

**Future product—contact factory for availability*

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## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 12/20 | Initial release | — |