2.7 V to 36 V Input, 2 A Single Buck DC/DC Converter with Boost Function For Automotive

BD8P250MUF-C

General Description

BD8P250MUF-C is a synchronous rectification buck DC/DC converter with a boost control function. This DC/DC converter enables a common design that can meet a variety of demands, including the use as a buck DC/DC converter if a drop of the output voltage is acceptable during the input voltage drop such as a cold cranking, and the use as a buck-boost DC/DC with an exclusive boost-FET connected if the output voltage must be maintained. The Quick Buck Booster® technology realizes a high-speed response even during buck-boost operations, allowing reduction in the capacitance value of the output capacitor.

Key Specifications

- Input Voltage A: 3.5 V to 36 V
(Buck DC/DC Converter, Initial startup is over 4.8 V)
- Input Voltage B: 2.7 V to 36 V
(Buck-Boost DC/DC Converter, Initial startup is over 7.5 V)
- Output Voltage: 5.0 V(Typ)
- Output Current in Buck Operation: 2 A(Max)
- Output Current in Buck-Boost Operation: 0.8 A(Max)
- Switching Frequency: 2.2 MHz(Typ)
- Shutdown Circuit Current: 3.5 µA(Typ)
- Quiescent Current: 8 µA(Typ)
- Operating Temperature: -40 °C to +125 °C

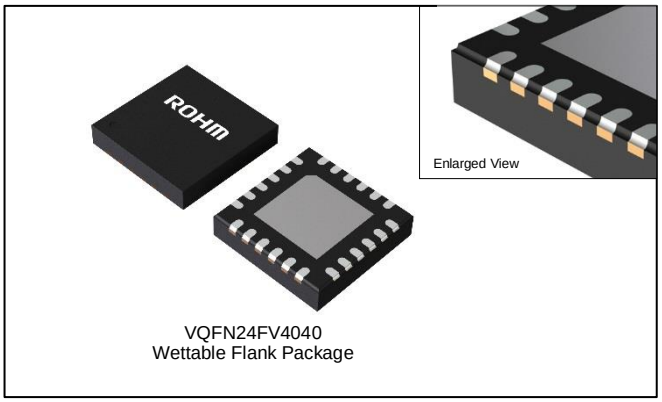
Features

- Quick Buck Booster®
- Nano Pulse Control™
- AEC-Q100 Qualified *(Note 1)*
- Boost Control Function
- LLM(Light Load Mode)
- Spread Spectrum Function
- Power Good Function
- Soft Start Function
- Current Mode Control
- Phase Compensation Included
- Over Current Protection
- Input Under Voltage Lockout Protection
- Thermal Shutdown Protection
- Output Over Voltage Protection
- Short Circuit Protection
- Wettable Flank QFN Package

(Note 1) Grade 1

Package

	W(Typ) x D(Typ) x H(Max)
VQFN24FV4040	4.00 mm x 4.00 mm x 1.00 mm

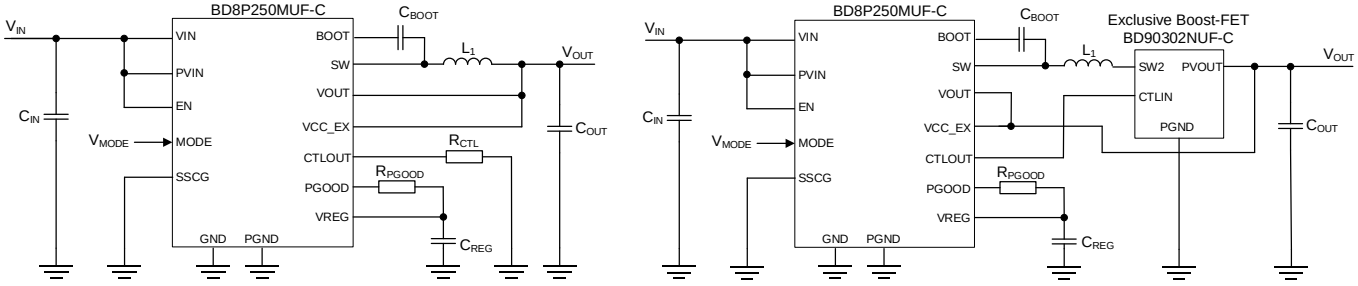


VQFN24FV4040
Wettable Flank Package

Applications

- Automotive Equipment
(Cluster Panel, Infotainment Systems)
- Other Electronic Equipment

Typical Application Circuit



A. Buck DC/DC Converter

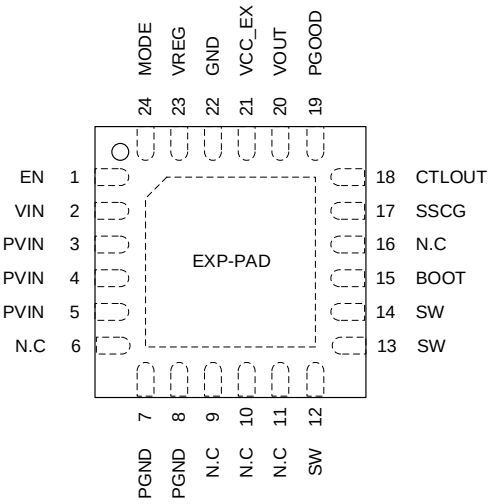
B. Buck-Boost DC/DC Converter (Use Exclusive Boost-FET)

Figure 1. Application Circuit

Quick Buck Booster® is a registered trademark of ROHM Co., Ltd.
Nano Pulse Control™ is a trademark of ROHM Co., Ltd.

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration



(TOP VIEW)
Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Function
1	EN	Enable pin. Apply Low-level (0.8 V or lower) to turn this device off. Apply High-level (2.0 V or higher) to turn this device on. This pin must be terminated.
2	VIN	Power supply input pin of the internal circuitry. Connect this pin to PVIN pin.
3to5	PVIN	Power supply input pins that are used for the output stage of the switching regulator. Connecting input ceramic capacitors with values of 4.7 µF(Typ) and 0.1 µF to this pin is recommended.
6	N.C	No connection pin. Leave these pins open, or connect to PVIN pin.
7,8	PGND	Ground pins for the output stage of the switching regulator.
9to10	N.C.	No connection pin. Leave these pins open, or connect to PGND pin.
11	N.C.	No connection pin. Leave this pin open.
12to14	SW	Switching node pins. These pins are connected to the source of the High Side FET and drain of the Low Side FET.
15	BOOT	Connect a bootstrap capacitor of 0.1 µF between this pin and the SW pins. The voltage of this capacitor is the gate drive voltage of the High Side FET.
16	N.C.	No connection pin. Leave this pin open.
17	SSCG	Pin to select Spread Spectrum function. Connect this pin to VREG pin or GND pin. Connect to VREG pin to enable Spread Spectrum function and connect to GND pin to disable Spread Spectrum function.
18	CTLOUT	Pin used to control the exclusive Boost-FET. When using the exclusive Boost-FET, connect this pin to CTLIN pin of the exclusive Boost-FET. Connect this pin to GND pin through a pull-down 1 kΩ resistor when not using the exclusive Boost-FET.
19	PGOOD	Power Good pin, an open drain output. Connect to VREG pin or suitable voltage supply through a pull-up resistor. Using a 10 kΩ to 100 kΩ resistance is recommended.
20	VOUT	Sense pin of output voltage. This pin is controlled to become 5.0 V(Typ).
21	VCC_EX	Internal power supply pin. Connect this pin to VOUT pin.
22	GND	Ground pin.
23	VREG	Internal power supply output pin. This node supplies power 5.0 V(Typ) to other blocks which are mainly responsible for the control function of the switching regulator. Connect a ceramic capacitor with value of 1.0 µF(Typ) to ground.
24	MODE	Pin for setting switching control mode. Turning this pin's signal to Low-level (0.8 V or lower) enables the LLM control and the mode is automatically switched between the LLM control and PWM (Pulse Wide Modulation) control. Turning this pin's signal to High-level (2.0 V or higher) enables the forced PWM control.This pin must be terminated.
-	EXP-PAD	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using via provides excellent heat dissipation characteristics.

Block Diagram

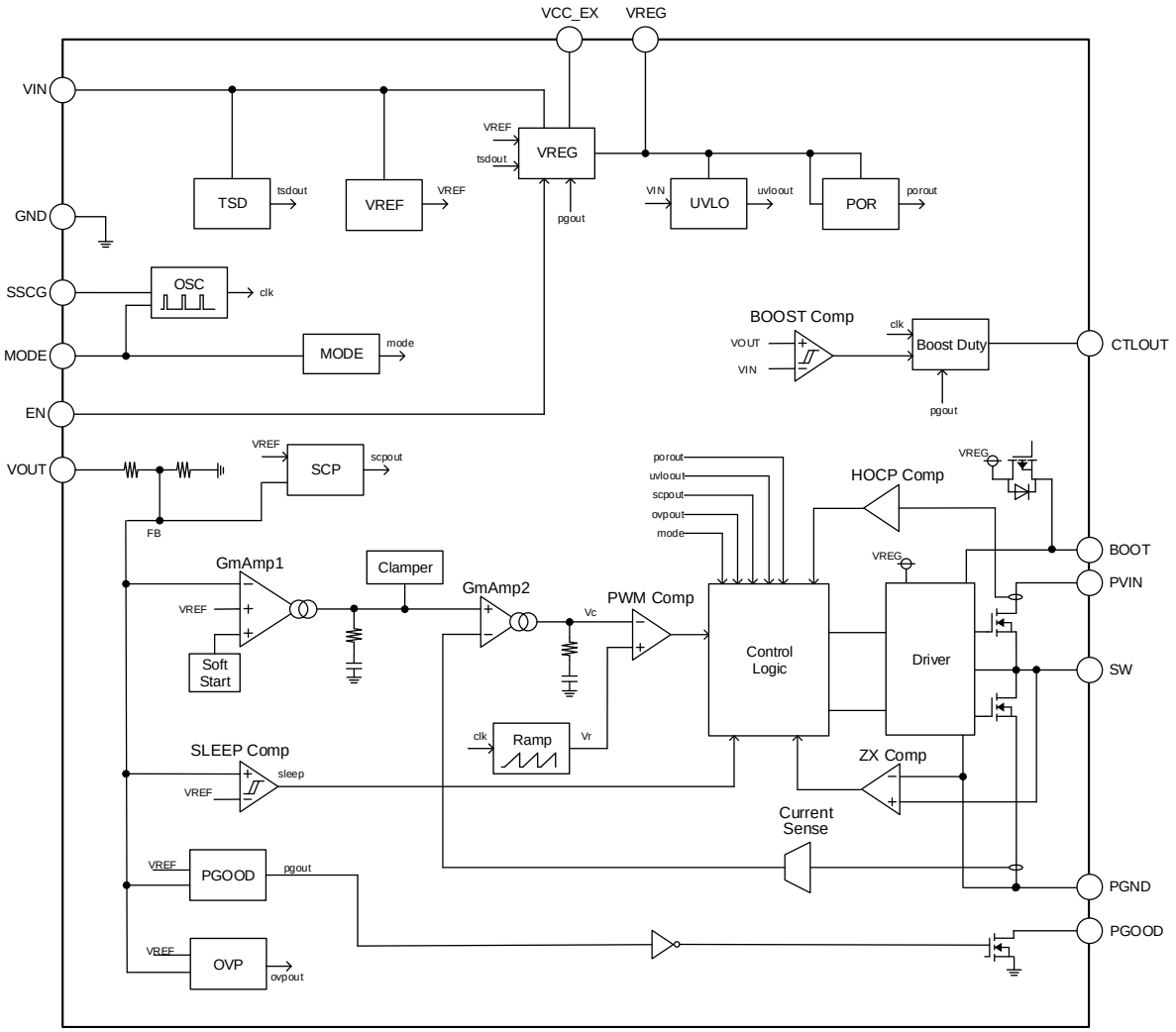


Figure 3. Block Diagram

Description of Blocks

•GmAmp1
This block is an error amplifier and its inputs are the reference voltage VREF and the division voltage FB of VOUT pin. It controls the GmAmp1 output such that the VREF voltage and the FB voltage equal.

•GmAmp2
This block sends the signal Vc which is composed of the GmAmp1 output and the current sense signal to PWM Comp.

•Soft Start
It is a function to prevent overshoot of inrush current and the output voltage by gradually raising the input reference voltage of GmAmp1 upon power supply ON. Soft start time is 1.0 ms(Typ).

•OSC
This block generates the clock frequency. Connect SSCG pin to GND pin to disable Spread Spectrum function and connect SSCG pin to VREG pin to enable it. This function becomes invalid when PGOOD output is Low or during Buck-Boost operation.

•Ramp
This block generates the saw tooth waveform Vr from the clock signal generated by OSC.

•Current Sense
This block detects the amount of change in inductor current through the Low Side FET and sends a current sense signal to GmAmp2.

•Clamper
This block clamps GmAmp1 output voltage and inductor current. It works as over current protection and LLM control current.

•PWM Comp
This block compares the saw tooth waveform Vr with the GmAmp2 output Vc and controls the duty cycle of the output switching pulse.

•Control Logic
This block receives the signal generated by the PWM Comp and outputs the control signal to the output MOSFET. In addition, it controls ON/OFF of the switching during light load and upon abnormal detection.

•TSD
This block is a thermal shutdown circuit. It will shut down the device to prevent thermal damage or a thermal-runaway of the device when the chip temperature reaches to approximately 175 °C(Typ) or more. When the chip temperature falls below the TSD threshold, the circuits are automatically restored to normal operation with hysteresis of 25 °C(Typ). Note that the thermal shutdown circuit is intended to prevent destruction of the device. Therefore, it is highly recommended to always keep the device temperature within Tjmax = 150 °C. Operation above operating temperature range will reduce the lifetime of the device. The restart need the input voltage like the startup. The regulator restarts the operation with soft start.

•SCP
This is the short circuit protection circuit. Turns OFF the output stage MOSFET for 15.4 ms (Typ) if it detects the VOUT pin voltage to be 55 % (Typ) or lower for 0.1 ms (Typ) or longer. Then, a restart is performed with the soft start. The SCP functions is masked for 1.4 ms (Typ) after the soft start. The input voltage required for the restoration is the same as that for the startup.

•OVP
This is the output over voltage protection circuit. When it detects the VOUT pin voltage is 120 % (Typ) or more for 1 µs (Typ) or longer, the output MOSFET are turned OFF. When it detects the VOUT pin voltage is less than 120 % (Typ) for 7 µs (Typ) or longer, it returns to normal operation.

•UVLO
The UVLO block is for under voltage lockout protection. It will shut down the device when the VIN falls to 2.4 V(Typ) or lower. The release voltage is 4.45 V(Typ) when the exclusive Boost-FET is not used, and is 7.15 V(Typ) when used with the exclusive Boost-FET. The regulator restarts the operation with soft start when the release voltage is satisfied.

•VREG
This block is the internal power supply circuit. It outputs 5.0 V(Typ) and is the power supply to the control circuit and driver. The input of this block during startup is the VIN pin voltage. When the PGOOD output becomes High, the VCC_EX pin voltage becomes its input supply, and consequently, high efficiency is achieved.

•VREF
The VREF block generates the internal reference voltage.

Description of Blocks – continued

•MODE
When MODE pin is 2.0 V or more, the device works by forced PWM control. When MODE pin is 0.8 V or less, the device enables the LLM control and the mode is automatically switched between the LLM control and PWM control. However, during Buck-Boost operation, the device works on forced PWM control.

•Driver
This circuit drives the gates of the output MOSFET.

•PGOOD
When the VOUT pin voltage reaches within ±5 %, the built-in Nch MOSFET turns OFF and the PGOOD output turns High. In addition, the PGOOD output turns Low when the VOUT pin voltage reaches outside ±10 %.

•POR
The POR block is the input under voltage lockout protection for the internal power supply. It will shut down the device when the VREG voltage falls to 2.85 V (Typ) or less. When the release voltage of 3.0 V (Typ) is satisfied, the regulator restarts the operation with soft start.

•SLEEP Comp
This block controls the VOUT pin voltage in PFM control from 101 % of PWM control to 102 % of PWM control.

•ZX Comp
This block stops the switching by detecting the reverse SW output current at LLM control.

•BOOST Comp, Boost Duty
This is the control circuit of the Boost signal. When used with the exclusive Boost-FET, PGOOD output is High and the VIN pin voltage becomes 140 % (Typ) or less of the VOUT pin voltage, an ON pulse with 70 % (Typ) duty is output by CTLOUT pin and putting the device in Buck-Boost operation. It returns to Buck operation with 10 % (Typ) of hysteresis.

•HOCP Comp
This block limits current of the High Side FET. When it detects current of 4 A (Min) or more, High Side FET is turned OFF. This function works only in abnormal situations such as when the SW pin is shorted to GND.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Input Voltage	V_{VIN}, V_{PVIN}	-0.3 to +42	V
EN Voltage	V_{EN}	-0.3 to +42	V
BOOT Voltage	V_{BOOT}	-0.3 to +49	V
Voltage from SW to BOOT	ΔV_{BOOT}	-0.3 to +7	V
MODE, SSCG, VOUT, VCC_EX, VREG, PGOOD, CTLOUT Voltage	V_{MODE}, V_{SSCG}, V_{VOUT}, V_{VCC_EX}, V_{VREG}, V_{PGOOD}, V_{CTLOUT}	-0.3 to +7	V
Maximum Junction Temperature	Tjmax	150	˚C
Storage Temperature Range	Tstg	-55 to +150	˚C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN24FV4040				
Junction to Ambient	θ_{JA}	107.4	32.6	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	9	4	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage A (Not use Exclusive Boost-FET)	V_{INA}	3.5	-	36	V
Input Voltage B (Use Exclusive Boost-FET)	V_{INB}	2.7	-	36	V
Operating Temperature	Topr	-40	-	+125	˚C
Output Current in Buck Operation	$I_{OUTBUCK}$	-	-	2.0	A
Output Current in Buck-Boost Operation	$I_{OUTBOOST}$	-	-	0.8	A
SW Minimum ON Time*(Note1)*	t_{ONMIN}	-	45	-	ns
Input Capacitor*(Note2)*	C_{IN}	2.3	4.7	-	µF
VREG Capacitor*(Note2)*	C_{REG}	0.48	1.0	2.1	µF

(Note 1) This parameter is for 1A output. Not 100 % tested.
(Note 2) Ceramic capacitor is recommended. The capacitor value including temperature change, DC bias change, and aging change must be considered.

Electrical Characteristics (Unless otherwise specified Ta = -40 ˚C to +125 ˚C, V_{IN} = 12 V, V_{EN} = 5 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
VIN						
Shutdown Circuit Current	I_{SDN}	-	3.5	7.0	µA	V_{EN}=0 V, Ta<105 °C
Quiescent Current (V_{IN})	I_{QVIN}	-	1.4	2.8	µA	V_{MODE}=0 V, V_{OUT}=V_{VCC_EX}=5.5 V, Ta<105 °C
Quiescent Current (V_{OUT})	I_{QVOUT}	-	16	32	µA	V_{MODE}=0 V, V_{OUT}=V_{VCC_EX}=5.5 V, Ta<105 °C
UVLO Detection Voltage	V_{UVLOL}	2.2	2.4	2.6	V	V_{IN} Falling
UVLO Release Voltage A	V_{UVLOHA}	4.25	4.45	4.65	V	V_{IN} Rising, CTLOUT Pin=0 V or 1 kΩ pull-down
UVLO Release Voltage B	V_{UVLOHB}	6.9	7.15	7.4	V	V_{IN} Rising, CTLOUT Pin=Open or CTLIN Pin*(Note 3)*
EN/MODE/SSCG						
EN Threshold Voltage High	V_{ENH}	2.0	-	V_{IN}	V	
EN Threshold Voltage Low	V_{ENL}	0	-	0.8	V	
EN Input Current	I_{EN}	-	0	1.0	µA	V_{EN}=5 V
MODE Threshold Voltage High	V_{MODEH}	2.0	-	5.5	V	
MODE Threshold Voltage Low	V_{MODEL}	0	-	0.8	V	
MODE Input Current	I_{MODE}	-	0	1.0	µA	V_{MODE}=5 V
SSCG Threshold Voltage High	V_{SSCGH}	2.0	-	5.5	V	
SSCG Threshold Voltage Low	V_{SSCGL}	0	-	0.8	V	
SSCG Input Current	I_{SSCG}	-	0	1.0	µA	V_{SSCG}=5 V
VREG						
VREG Voltage	V_{REG}	4.80	5.00	5.20	V	
POR Detection Voltage	V_{PORL}	2.70	2.85	3.00	V	V_{VREG} Falling

(Note 3) CTLIN is the pin of exclusive boost-FET.

Electrical Characteristics – continued
(Unless otherwise specified Ta = -40 ˚C to +125 ˚C, VIN = 12 V, VEN = 5 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
VOUT						
Output Voltage	V_{OUT1}	4.90	5.000	5.10	V	PWM Control
Output Voltage (LLM) *(Note 4)*	V_{OUT2}	4.90	5.075	5.25	V	LLM Control, V_{MODE}=0 V, Including output ripple
Soft Start Time	t_{SS}	0.5	1.0	1.5	ms	
SW						
High Side FET ON Resistance	R_{ONH}	-	110	220	mΩ	I_{SW}=-50 mA
Low Side FET ON Resistance	R_{ONL}	-	110	220	mΩ	I_{SW}=50 mA
High Side FET Leakage Current	$I_{LEAKSWH}$	-	0	10	µA	V_{IN}=36 V, V_{EN}=0 V, V_{SW}=0 V, Ta<105 ˚C
Low Side FET Leakage Current	$I_{LEAKSWL}$	-	0	10	µA	V_{IN}=36 V, V_{EN}=0 V, V_{SW}=36 V, Ta<105 ˚C
Switching Frequency	f_{SW}	2.0	2.2	2.4	MHz	
Over Current Protection*(Note 4)*	I_{OCP}	3.1	3.6	4.1	A	
Spread Spectrum	f_{SSCG}	-	f_{SW} x 110 %	-	MHz	V_{SSCG}=5 V
Spread Spectrum Modulation Cycle	$t_{SSCGCYCLE}$	-	220	-	µs	V_{SSCG}=5 V
PGOOD						
PGOOD Threshold Voltage 1	V_{PG1}	V_{OUT1} x 92 %	V_{OUT1} x 95 %	V_{OUT1} x 98 %	V	V_{OUT} Rising
PGOOD Hysteresis Voltage 1	V_{PGhys1}	-	V_{OUT1} x -5 %	-	V	V_{OUT} Falling
PGOOD Threshold Voltage 2	V_{PG2}	V_{OUT1} x 102 %	V_{OUT1} x 105 %	V_{OUT1} x 108 %	V	V_{OUT} Falling
PGOOD Hysteresis Voltage 2	V_{PGhys2}	-	V_{OUT1} x +5 %	-	V	V_{OUT} Rising
PGOOD Leakage Current	I_{PGLEAK}	-	0	1	µA	V_{PGOOD}=5 V, V_{OUT}=5.0 V
PGOOD ON Resistance	R_{PG}	-	250	500	Ω	I_{PGOOD}=1 mA, V_{EN}=0 V
SCP/OVP						
OVP Detection Voltage	V_{OVP}	V_{OUT1} x 115 %	V_{OUT1} x 120 %	V_{OUT1} x 125 %	V	
SCP Detection Voltage	V_{SCP}	V_{OUT1} x 50 %	V_{OUT1} x 55 %	V_{OUT1} x 60 %	V	
BOOST						
Buck-Boost Threshold Voltage	V_{BOOST}	V_{OUT} x 131 %	V_{OUT} x 140 %	V_{OUT} x 149 %	V	V_{IN} Falling, CTLOUT Pin=Open or CTLIN Pin*(Note 3)*
Buck-Boost Hysteresis Voltage	$V_{BOOSThys}$	-	V_{OUT} x +10 %	-	V	V_{IN} Rising, CTLOUT Pin=Open or CTLIN Pin*(Note 3)*
CTLOUT ON Duty	D_{CTLOUT}	66	70	74	%	V_{IN}=6.5 V, CTLOUT Pin=Open or CTLIN Pin*(Note 3)*

(Note 3) CTLIN is the pin of exclusive boost-FET.
(Note 4) This is design value. Not production tested.

Typical Performance Curves
(Unless otherwise specified $V_{IN} = V_{EN}$)

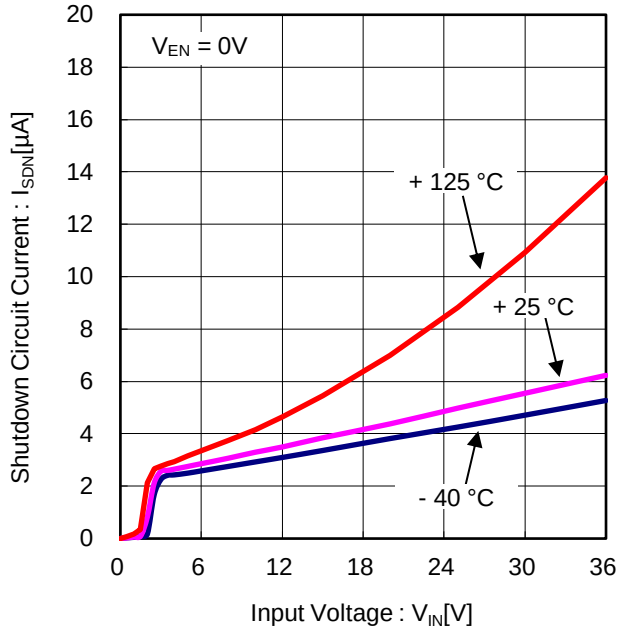


Figure 4. Shutdown Circuit Current vs Input Voltage

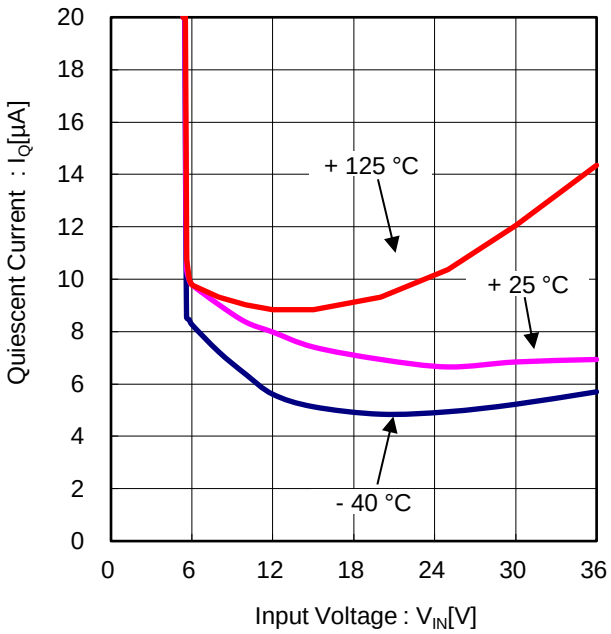


Figure 5. Quiescent Current at No Load vs Input Voltage

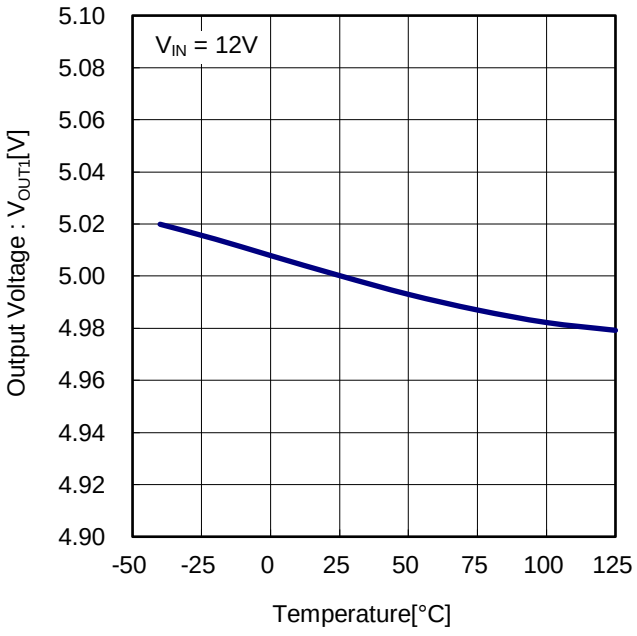


Figure 6. Output Voltage vs Temperature

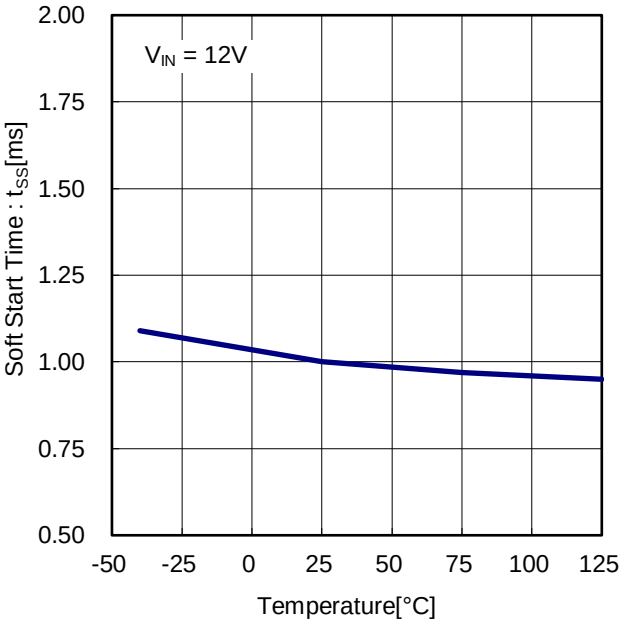


Figure 7. Soft Start Time vs Temperature

Typical Performance Curves – continued

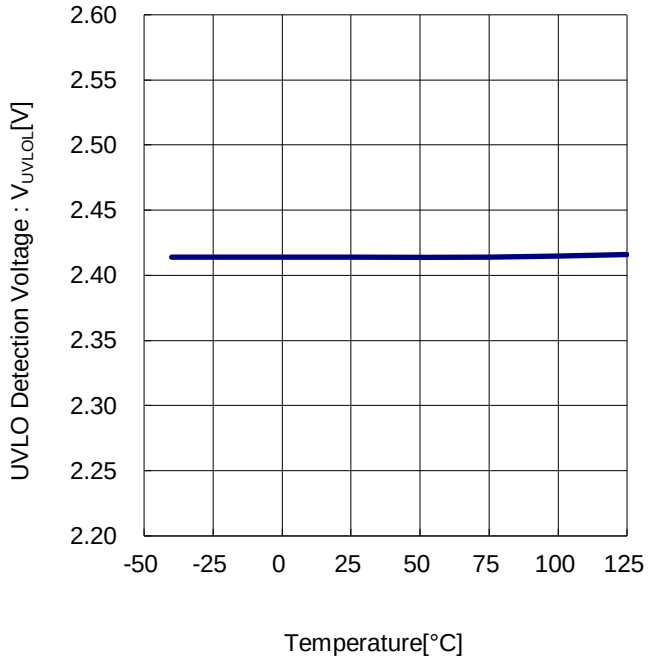


Figure 8. UVLO Detection Voltage vs Temperature

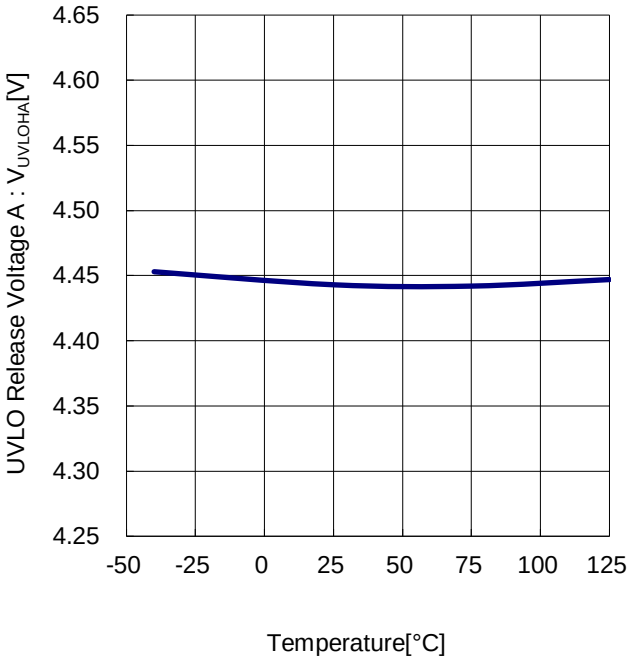


Figure 9. UVLO Release Voltage A vs Temperature

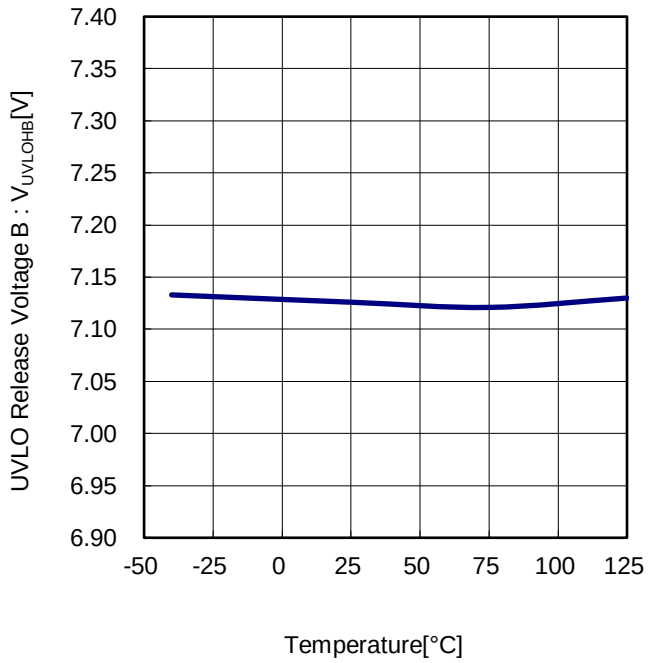


Figure 10. UVLO Release Voltage B vs Temperature

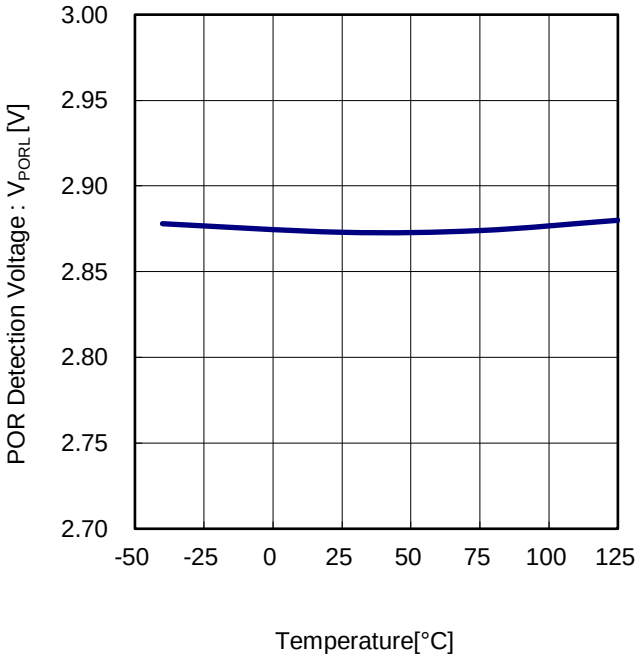


Figure 11. POR Detection Voltage vs Temperature

Typical Performance Curves – continued

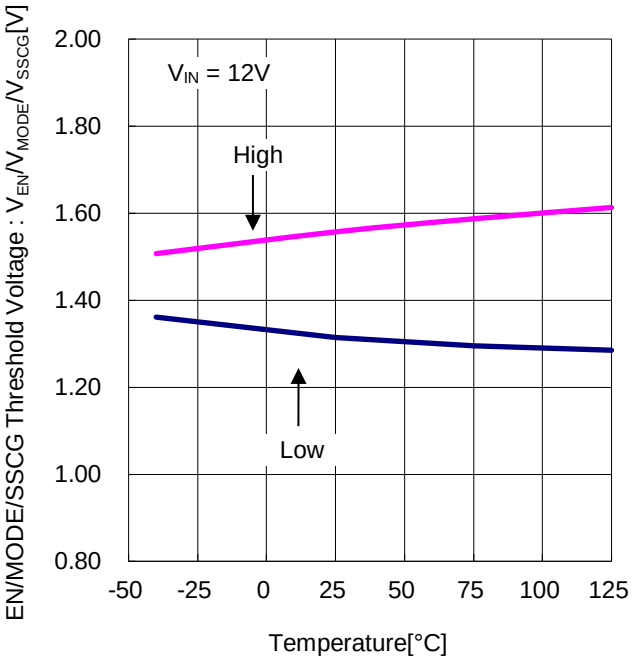


Figure 12. EN/MODE/SSCG Threshold Voltage vs Temperature

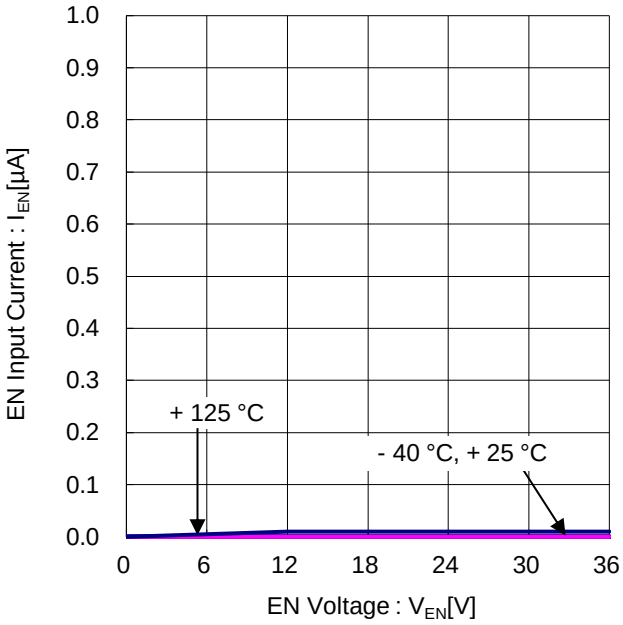


Figure 13.EN Input Current vs EN Voltage

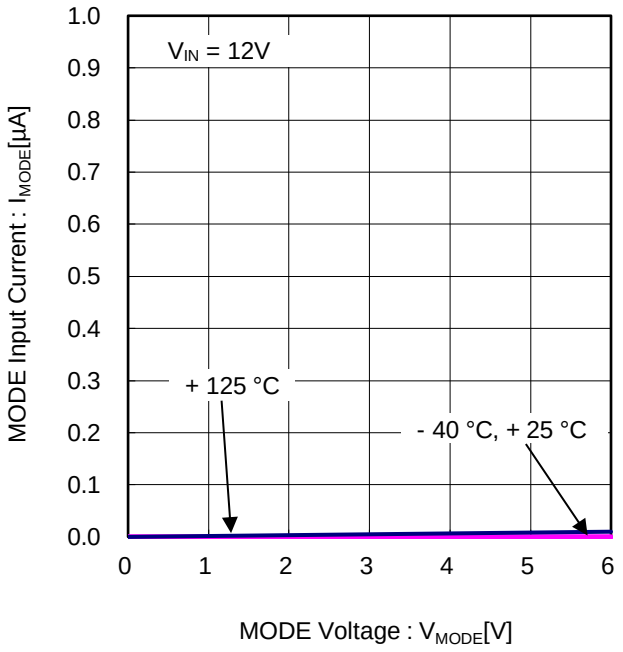


Figure 14. MODE Input Current vs MODE Voltage

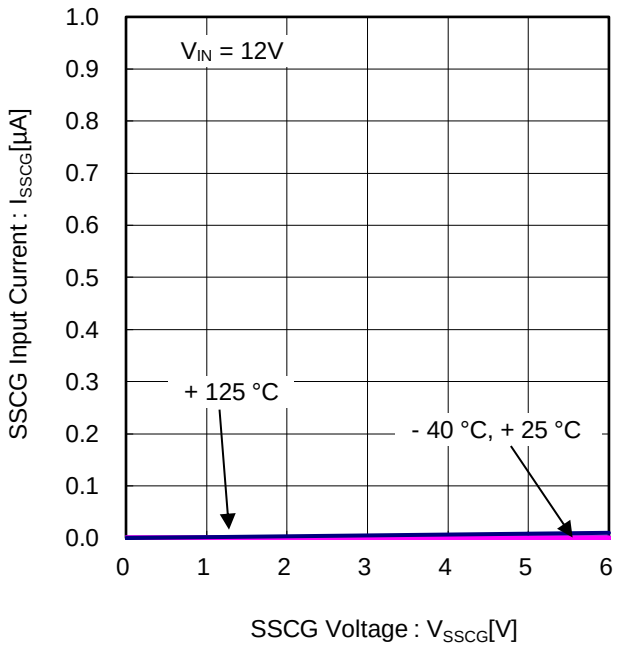


Figure 15. SSCG Input Current vs SSCG Voltage

Typical Performance Curves – continued

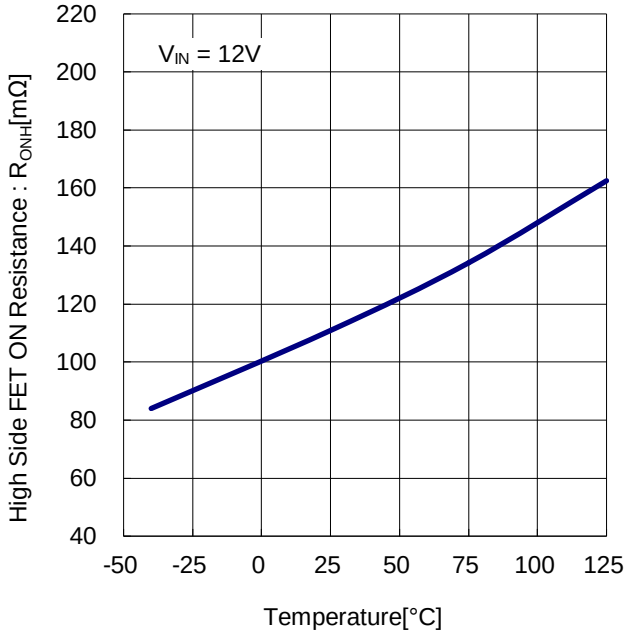


Figure 16. High Side FET ON Resistance vs Temperature

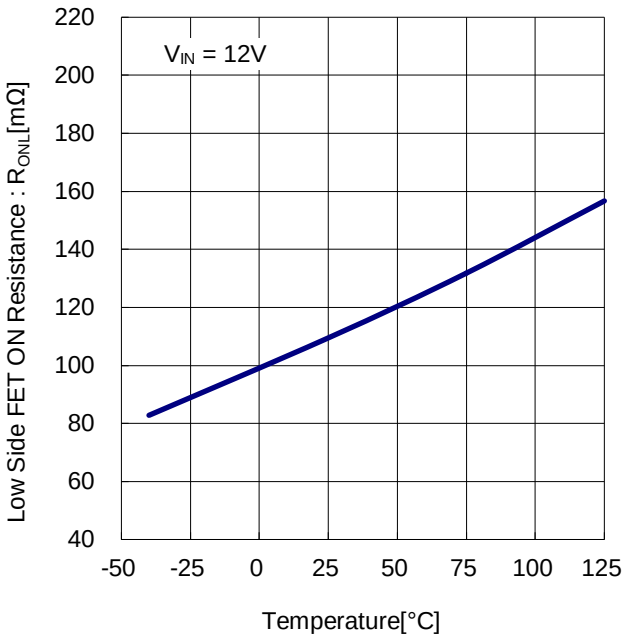


Figure 17. Low Side FET ON Resistance vs Temperature

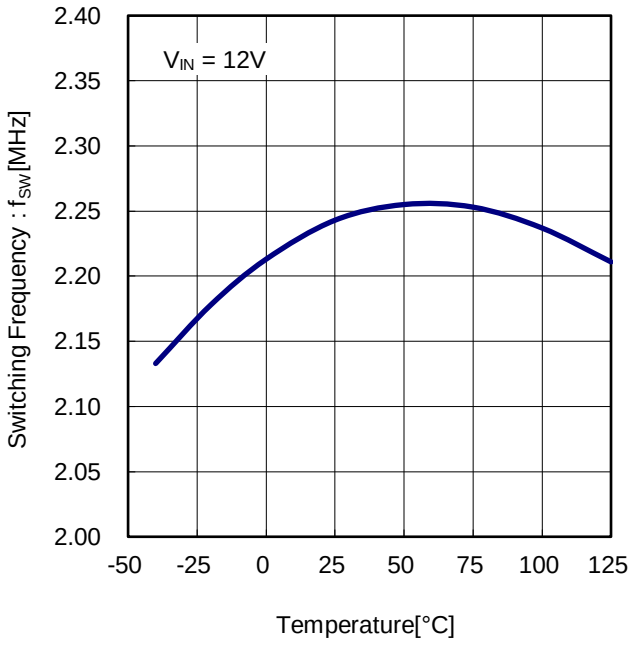


Figure 18.Switching Frequency vs Temperature

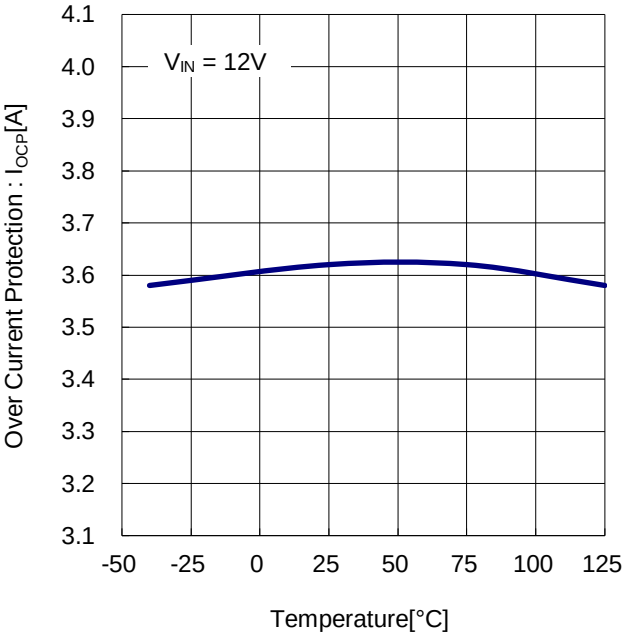


Figure 19. Over Current Protection vs Temperature

Typical Performance Curves – continued

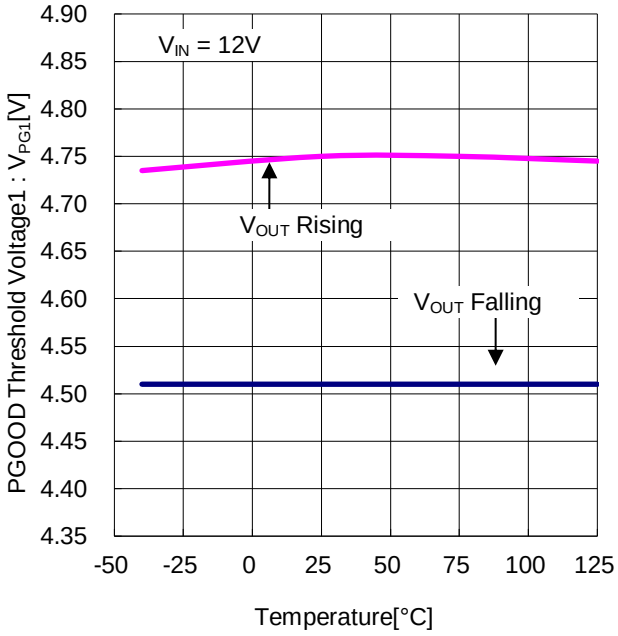


Figure 20. PGOOD Threshold Voltage 1 vs Temperature

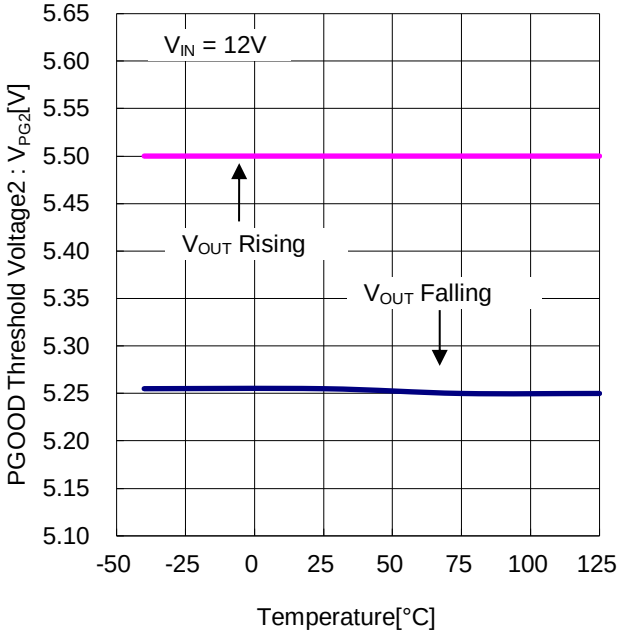


Figure 21. PGOOD Threshold Voltage 2 vs Temperature

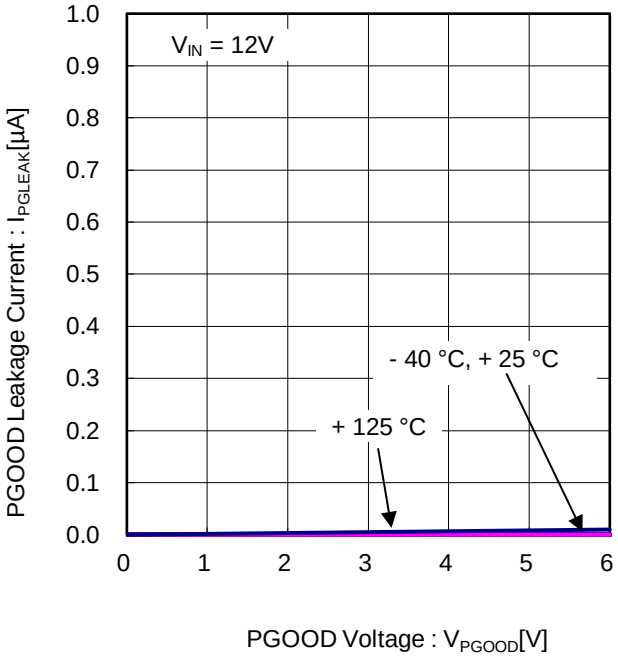


Figure 22. PGOOD Leakage Current vs PGOOD Voltage

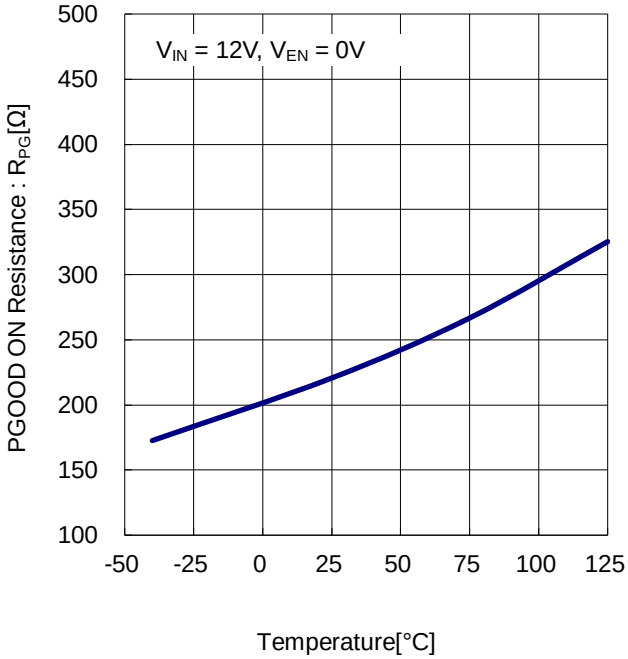


Figure 23. PGOOD ON Resistance vs Temperature

Typical Performance Curves – continued

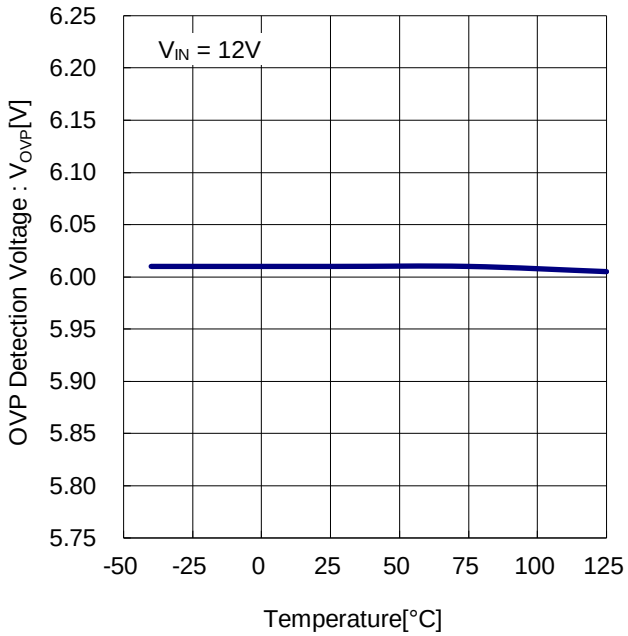


Figure 24. OVP Detection Voltage vs Temperature

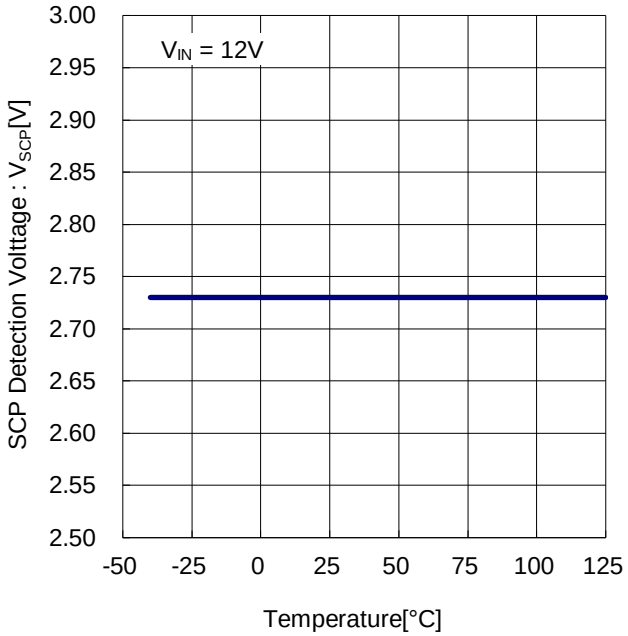


Figure 25. SCP Detection Voltage vs Temperature

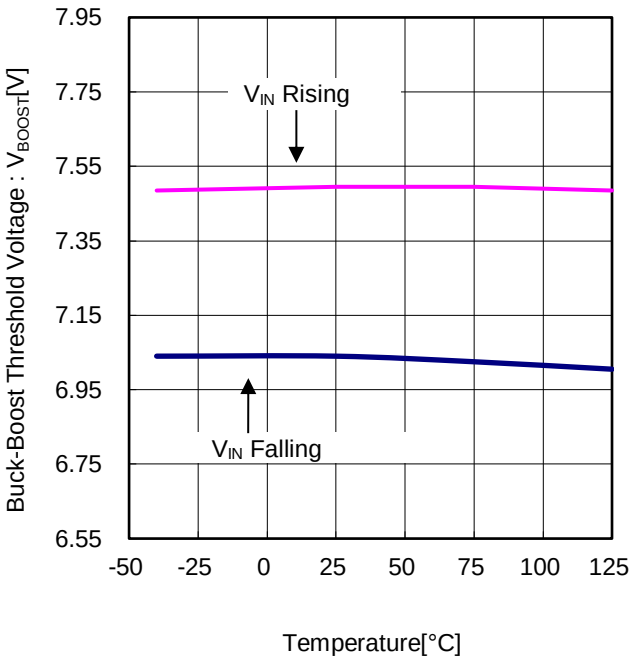


Figure 26. Buck-Boost Threshold Voltage vs Temperature

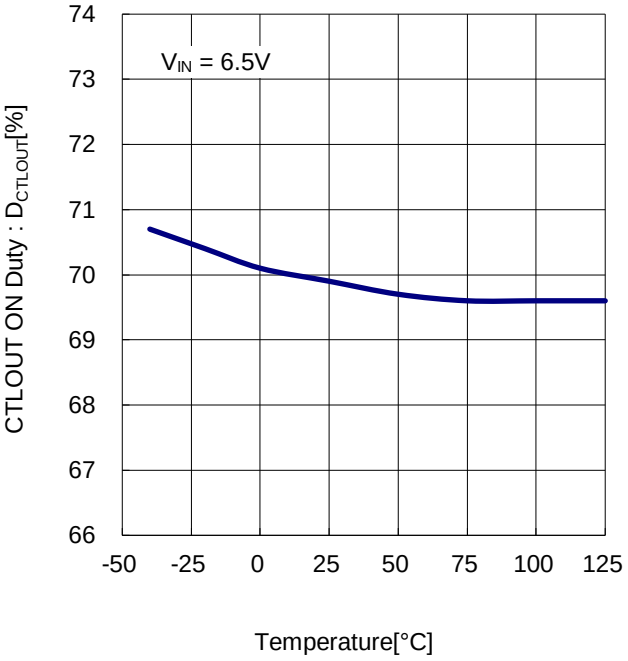


Figure 27. CTLOUT ON Duty vs Temperature

Function Explanations

1. Quick Buck Booster®
   Quick Buck Booster® is a buck-boost control technology to maintain a stable output voltage even when a significant drop of the supply voltage occurs in a short period of time such as the startup profile of ISO16750-2. Quick Buck Booster® controls the boost side switch in a fixed duty cycle to remove the Right-Half-Plane-Zero that may cause problems in buck-boost operations, and can achieve the transfer characteristics equivalent to those in the buck operation even in the buck-boost operation. This enables a facilitation of the phase compensation setting and a reduction in the output capacitance. In addition, it realizes a smooth switching of operations by performing a pulse width modulation with the buck side switch during both of the buck and buck-boost operations, enabling a high-speed transient response to a steep variation in the power supply or the load.

   (1) Frequency Characteristics
   Since Quick Buck Booster® enables to remove the Right-Half-Plane-Zero, the phase compensation for the buck-boost control will not involve the Right-Half-Plane-Zero.

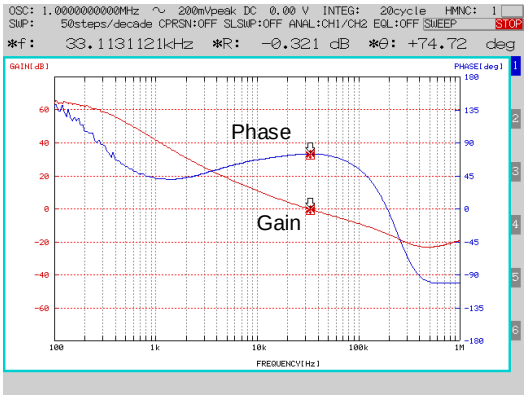


Figure 28. Frequency Characteristics at Buck Control

(V_{IN} = 12 V, I_{OUT} = 0.4 A, L_1 = 3.3 µH, C_{OUT} = 44 µF)

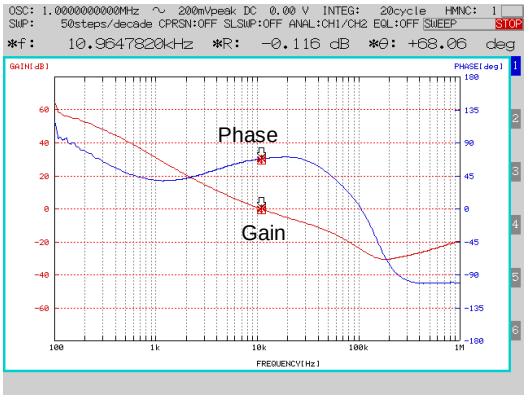


Figure 29. Frequency Characteristics at Buck-Boost Control

(V_{IN} = 4 V, I_{OUT} = 0.4 A, L_1 = 3.3 µH, C_{OUT} = 44 µF)

(2) Quick Buck Booster® Operation Wave Form
A decrease in VIN voltage drives the boost side switch in a fixed duty cycle, starting the boost operation. Correspondingly, the buck side duty cycle is automatically corrected to the optimum value to supply a stable output voltage.

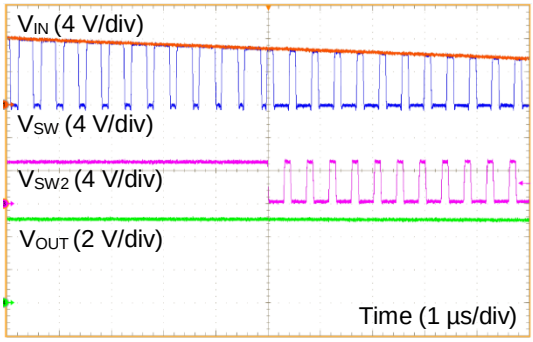


Figure 30. Change Wave Form
to Buck-Boost Control from Buck Control

(V_{IN} = Sweep Down, I_{OUT} = 0.4 A, L_1 = 3.3 µH, C_{OUT} = 44 µF)

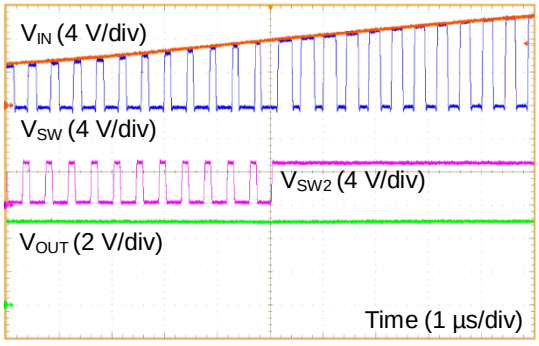


Figure 31.Change Wave Form
to Buck Control from Buck-Boost Control

(V_{IN} = Sweep Up, I_{OUT} = 0.4 A, L_1 = 3.3 µH, C_{OUT} = 44 µF)

Function Explanations – continued

2. Nano Pulse Control™
   Nano Pulse Control™ is an original technology developed by ROHM Co., Ltd. It enables to control voltage stably, which is difficult in the conventional technology, even in a narrow SW ON time such as less than 50 ns at typical condition.

3. Enable Control
   The shutdown of the device can be controlled by the voltage applied to the EN pin. When EN pin voltage reaches 2.0 V or higher, VREG starts up and the device operates. However, there is a delay time of 0.5 ms (Typ) before the beginning of the soft start. When EN pin voltage drops to 0.8 V or lower, the device is shut down.

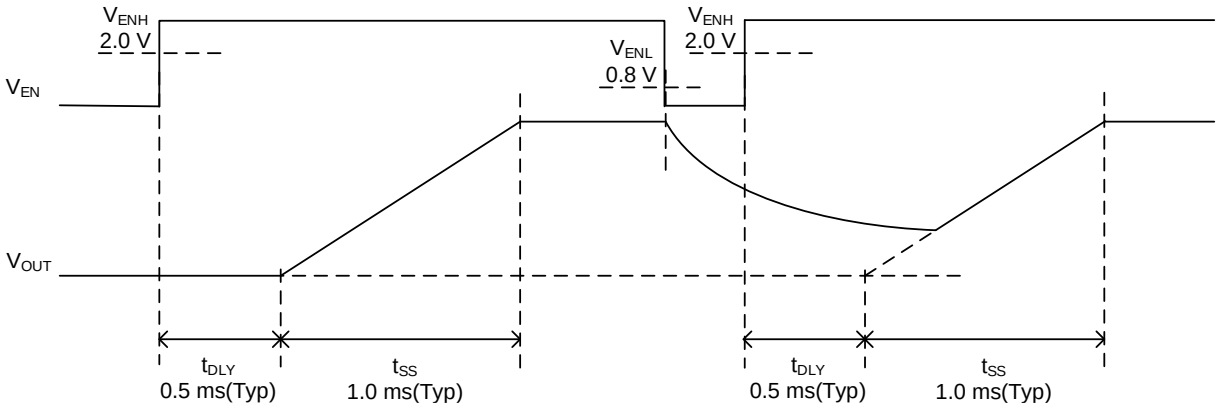


Figure 32. Enable ON/OFF Timing Chart

4. Power Good Function
   When the VOUT pin voltage reaches a voltage within ±5 % (Typ), the open drain MOSFET of the PGOOD pin is turned OFF and the output is switched to “High”. In addition, when the VOUT pin voltage varies beyond the ±10 % (Typ) range, the open drain MOSFET of the PGOOD pin is turned ON and the PGOOD pin is pulled down with an impedance of 250 Ω (Typ). Using a resistance of 10kΩ to 100kΩ, pull it up to the VREG pin or the power supply.

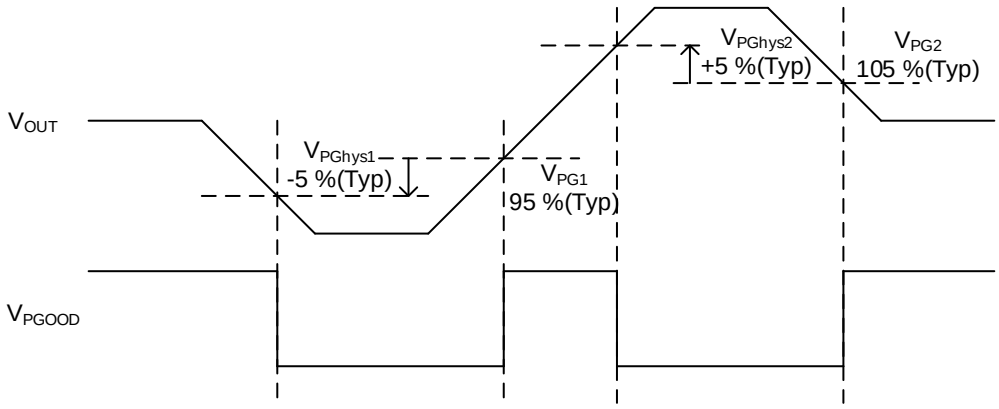


Figure 33. PGOOD Timing Chart

Function Explanations – continued

5. Under Voltage Lockout Protection (UVLO/POR)
   The input under voltage lockout protection circuit monitors the voltage of the VIN and VREG pins. UVLO and POR monitor the VIN and VREG voltages, respectively. The device is shut down when either of them is detected, and started up with the soft start when both are released. When an exclusive boost-FET is not used, VREG at 2.85 V(Typ) or lower brings the device to the standby state, and VIN at 4.45 V(Typ) or higher prompts the startup operation. When an exclusive boost-FET is used, VIN at 2.4 V(Typ) or lower brings the device to the standby state, and VIN at 7.15 V (Typ) or higher prompts the startup operation.

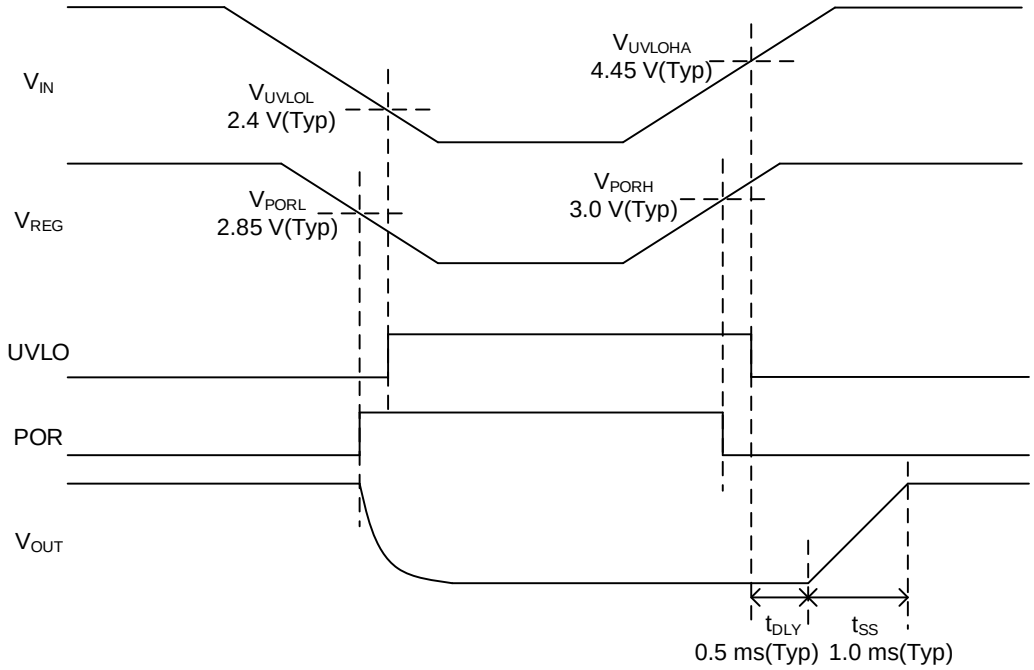


Figure 34. UVLO/POR Timing Chart (Not Use Exclusive Boost-FET)

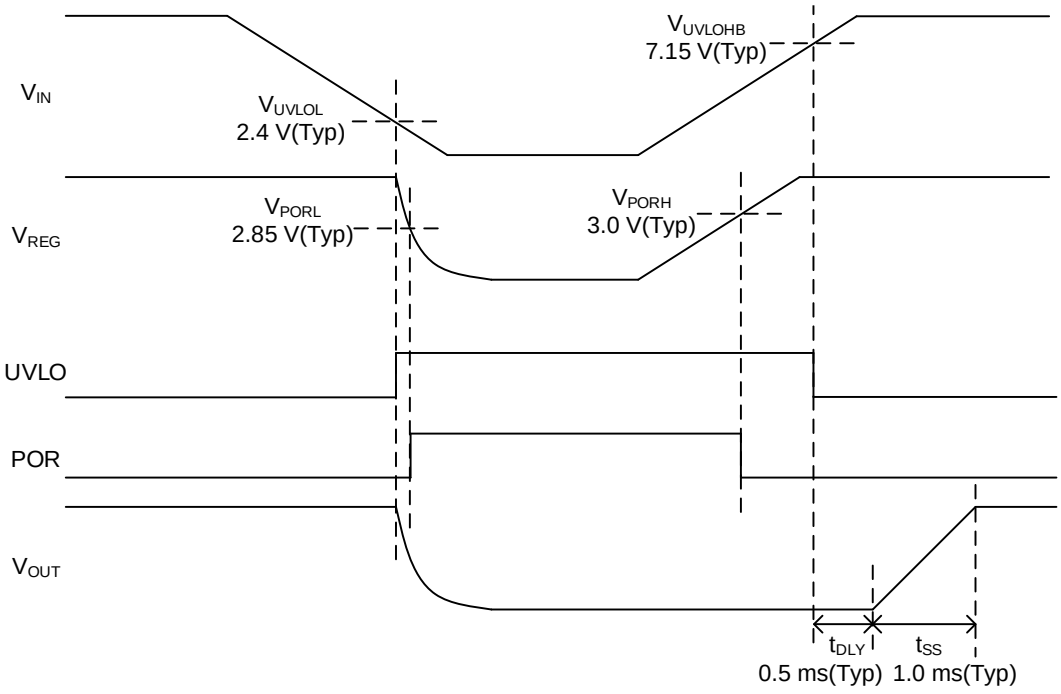


Figure 35. UVLO/POR Timing Chart (Use Exclusive Boost-FET)

Function Explanations – continued

6. LLM control and Forced PWM control
   Under a heavy load, the switching operation is performed with the Pulse Width Modulation (PWM) control at a fixed frequency. When the load is lighter, the operation is changed over to the Light Load Mode (LLM) control to improve the efficiency. However, the operation is forced into the PWM control when the MODE pin is “High” (2.0 V or higher), during the startup, or during the buck-boost operation. Although the efficiency under a light load is reduced under the forced PWM control compared with the LLM control, the operation is performed in the continuous current mode at a fixed frequency over the entire load range, enabling reduction in the output ripple voltage.

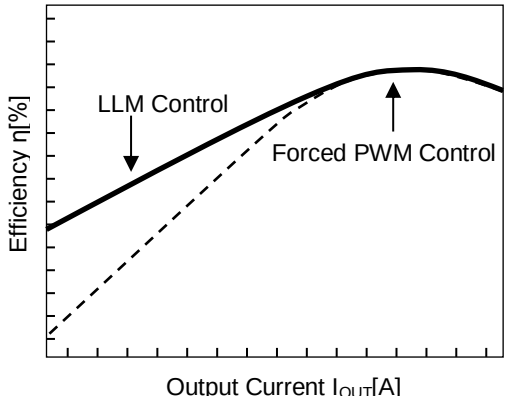


Figure 36. Efficiency (LLM Control and Forced PWM Control)

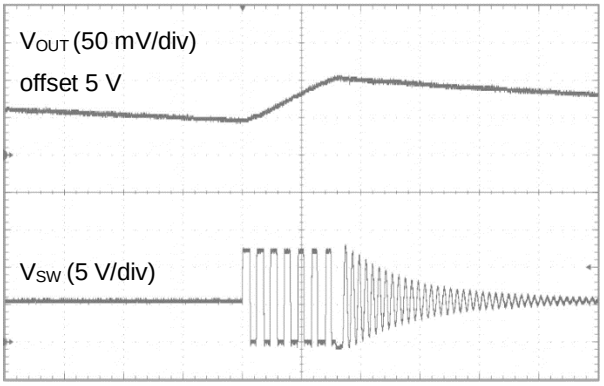


Figure 37. SW Waveform(LLM)
(V_{IN} = 12 V, I_{OUT} = 50 mA)

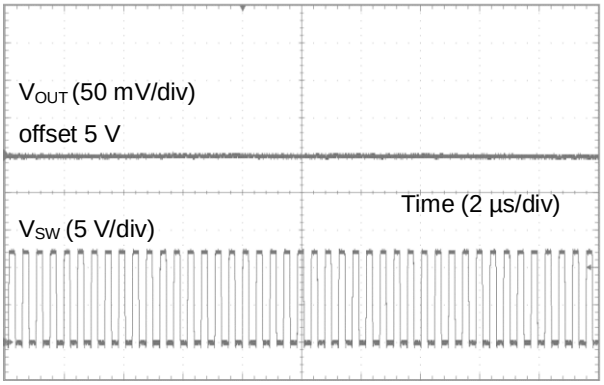


Figure 38. SW Waveform(PWM)
(V_{IN} = 12 V, I_{OUT} = 1 A)

For BD8P250MUF-C, the operation is changed over to the LLM control when the load current decreases to 0.4 A (Typ) or lower. Under the LLM control, the switching is stopped when the output voltage rises to 102 % (Typ) or higher. While the switching is stopped, the circuit current is reduced by stopping the circuits other than the output voltage monitor. When the load current decreases the output voltage to 101 % (Typ) of the specified voltage or lower, the switching resumes. Depending on the conditions, since the output ripple voltage may fall within the audible range in operations under the LLM control, use the device under the forced PWM control if it is necessary to avoid the audible range.

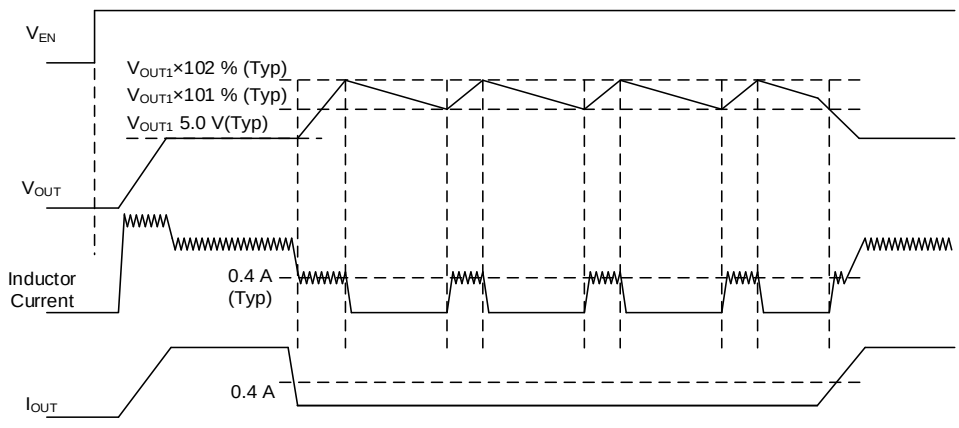


Figure 39. LLM Control Timing Chart

Function Explanations – continued

7. Frequency Division Function

BD8P250MUF-C drives the high side FET with a bootstrap and requires the ON time of the low side FET to charge the BOOT pin. Therefore, the minimum OFF time of the SW pin is specified, and the output voltage is limited by the minimum OFF time under the condition in which the input and output voltages are close. The prevent this situation, OFF pulses are skipped when the input and output voltages are small to keep the high side FET turned ON and increase the ON duty of the SW pin. Three consecutive OFF pulses are skipped at a maximum. In this case, the output voltage can be calculated with the following equation.

$$V_{OUT} = MaxDuty \times (V_{IN} - R_{ONH} \times I_{OUT}) - R_{DC} \times I_{OUT}$$
$$= \left(1 - t_{OFF} \times \frac{f_{SW}}{4}\right) \times (V_{IN} - R_{ONH} \times I_{OUT}) - R_{DC} \times I_{OUT} \text{ [V]}$$

$MaxDuty$	is the SW pin Maximum ON Duty [%]
V_{IN}	is the Input Voltage [V]
R_{ONH}	is the High Side FET ON Resistance (Refer to Page.8) [Ω]
I_{OUT}	is the Output Current [A]
R_{DC}	is the DCR of Inductor [Ω]
t_{OFF}	is the SW pin Minimum OFF Time [s] (Typ : 100 ns)
f_{SW}	is the Switching Frequency (Refer to Page.8) [Hz]

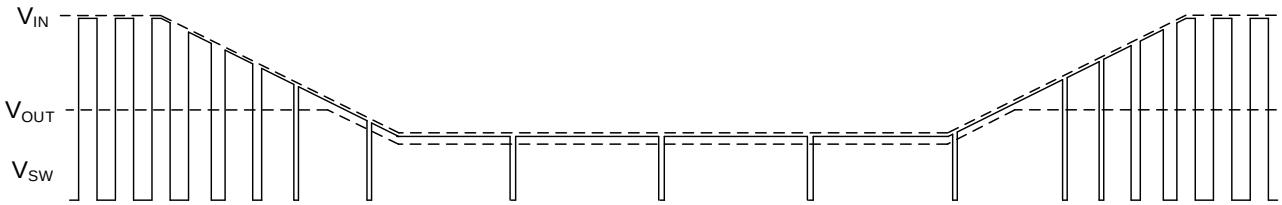


Figure 40. Frequency Division Function

8. Buck-Boost Control

When BD8P250MUF-C is used with BD90302NUF-C, an exclusive boost-FET, a drop of the output voltage can be prevented by the buck-boost operation even when the input voltage is decreased due to a cold cranking, etc. The buck operation is performed if the input voltage is 140 %(Typ) of the output voltage or higher. If not, the buck-boost operation is performed. During the buck-boost operation, an ON pulse at 70 %(Typ) duty is outputted from the CTLOUT pin to control the exclusive boost-FET. The buck operation is restored with a hysteresis of 10 %(Typ) or when the PGOOD output is changed over to “Low”. In addition, the maximum output current is 2.0 A and 0.8 A during the buck and buck-boost operations, respectively.

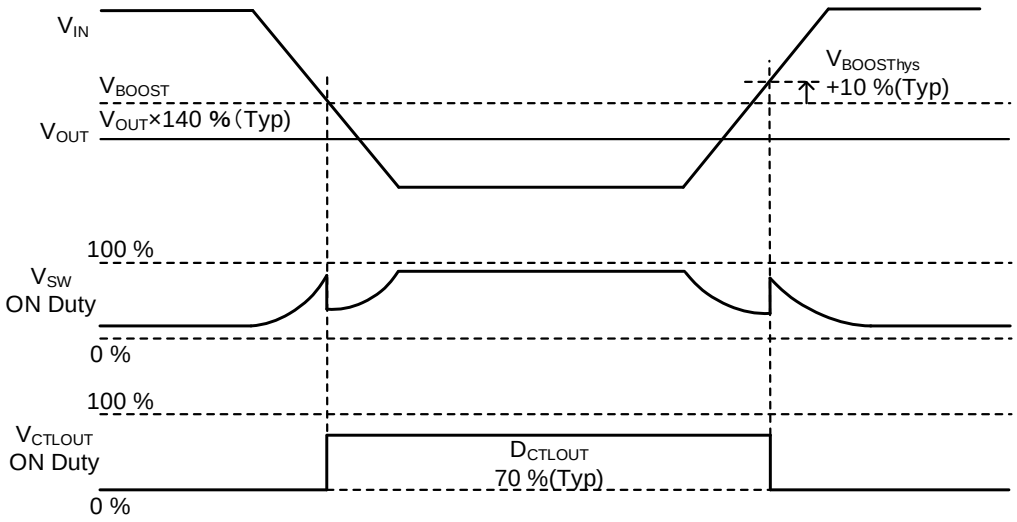


Figure 41. Buck-Boost Control

Function Explanations – continued

9. Spread Spectrum Function

Connecting the SSCG pin with VREG pin activates the Spread Spectrum function, reducing the EMI noise level. When the Spread Spectrum function is activated, the switching frequency alternates between 2.2 MHz(Typ) and its +10 %(Typ) with a ramp. The period of the ramp is 220 µs(Typ). However, this function is masked when the PGOOD output is “Low” or during the buck-boost operation. This function is disabled when the SSCG pin is connected with the ground.

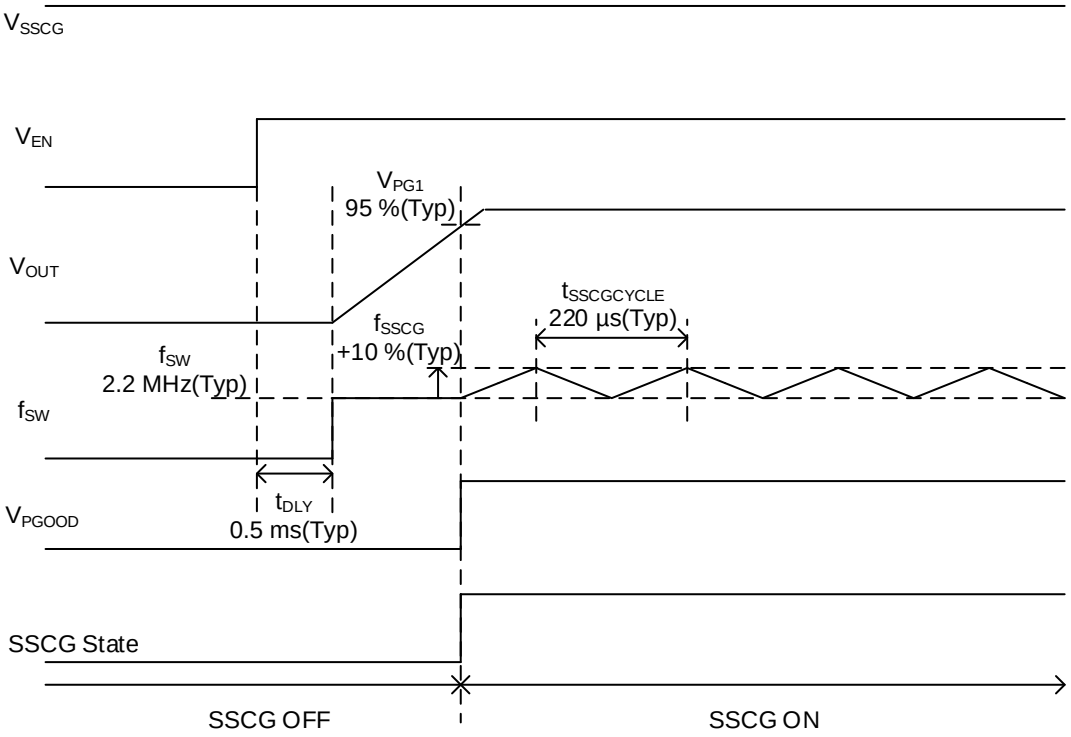


Figure 42. Spread Spectrum Function Timing Chart

Protection

1. Over Current Protection (OCP)
   The over current protection (OCP) function is realized through the detection of the inductor current. The over current limit is designed to be 3.6 A(Typ). The output voltage is decreased when the OCP detection occurs. It should be noted that the OCP detection current for the output current is decreased during the buck-boost operation.

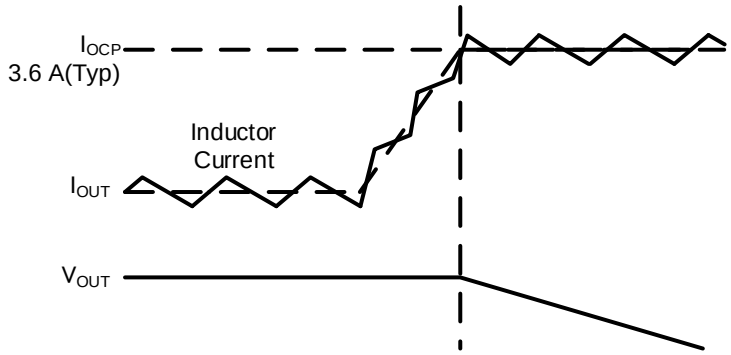


Figure 43. Over Current Protection

2. Short Circuit Protection (SCP)
   The short circuit protection (SCP) function compares the VOUT pin voltage with the internal reference voltage and turns OFF the output stage MOSFET for 15.4 ms(Typ) if it detects the VOUT pin voltage to be 55 %(Typ) or lower for 0.1 ms (Typ) or longer. Then, a restart is performed with the soft start. The SCP function is masked for 1.4 ms(Typ) after the soft start. The input voltage required for the restoration is the same as that for the startup.

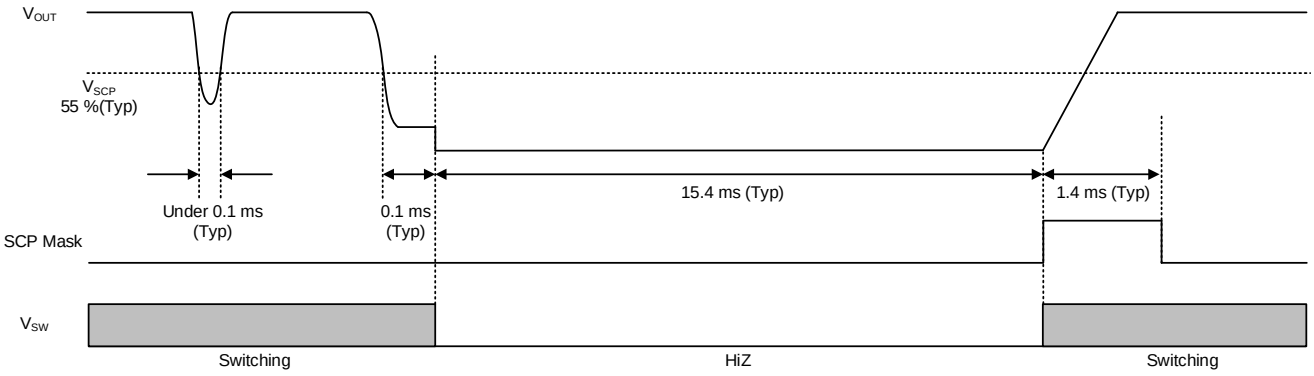


Figure 44. SCP Timing Chart (Short Circuit Devision)

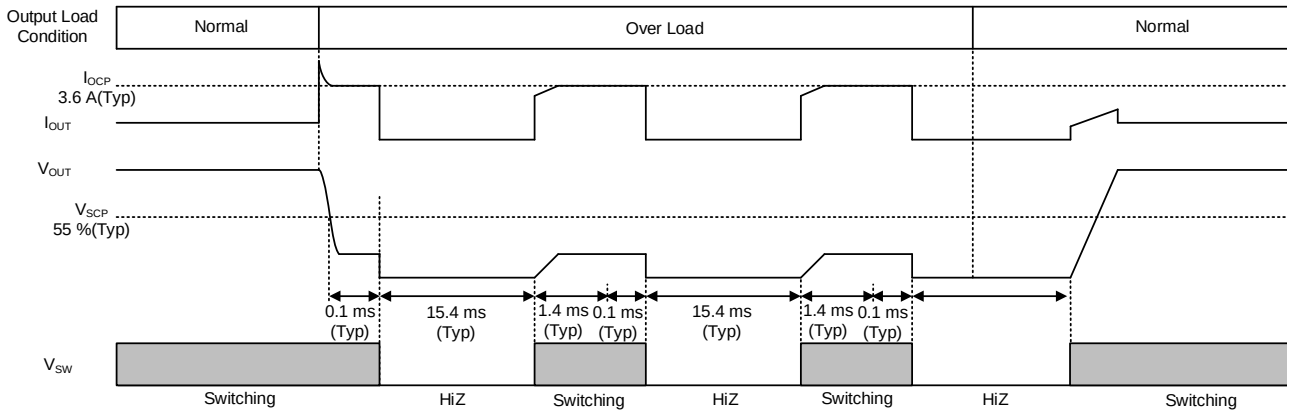


Figure 45. SCP Tinimg Chart (Self Return)

Protection – continued

3. Thermal shutdown (TSD)
The device is shutdown when the chip temperature exceeds Tj = 175 °C (Typ). The thermal cutoff circuit is exclusively for the purpose of cutting off the device from a thermal runaway under an abnormal condition exceeding Tjmax = 150 °C. It is not intended for the protection or guarantee of the set. Therefore, do not design a set protection utilizing the function of this circuit. The input voltage required for the restoration is the same as that for the startup. A restart is performed with the soft start.

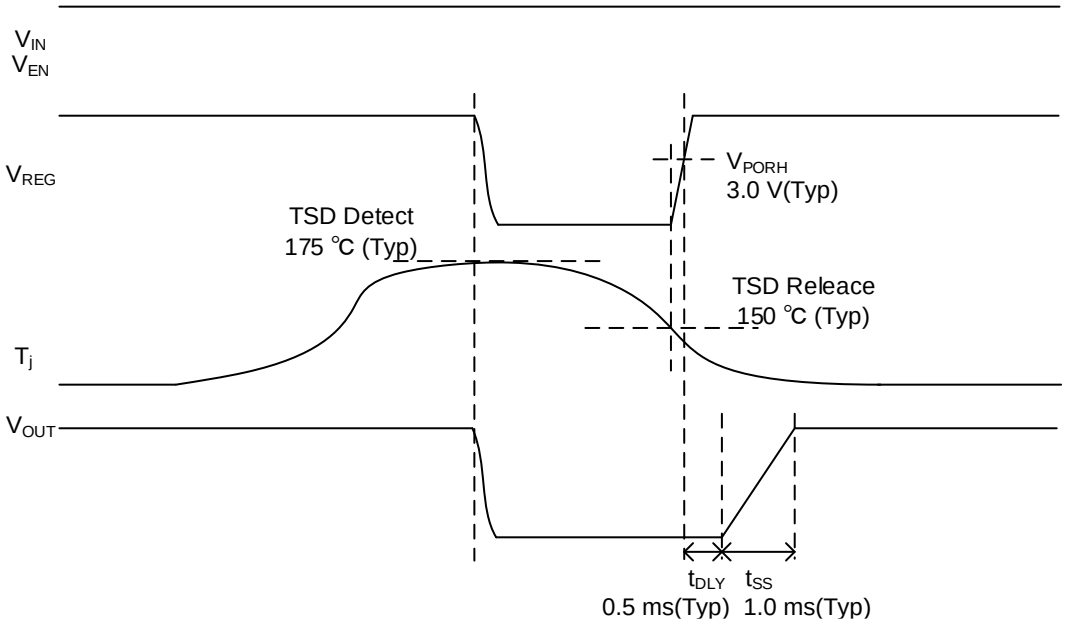


Figure 46. TSD Timing Chart

4. Over Voltage Protection (OVP)
The over voltage protection (OVP) function compares the VOUT pin voltage with the internal reference voltage and turns OFF the output stage MOSFET if the VOUT pin voltage exceeds 120 % (Typ) of the internal reference voltage for 1 µs (Typ) or longer. It is restored when VOUT pin voltage falls below the threshold for 7 µs (Typ) or longer.

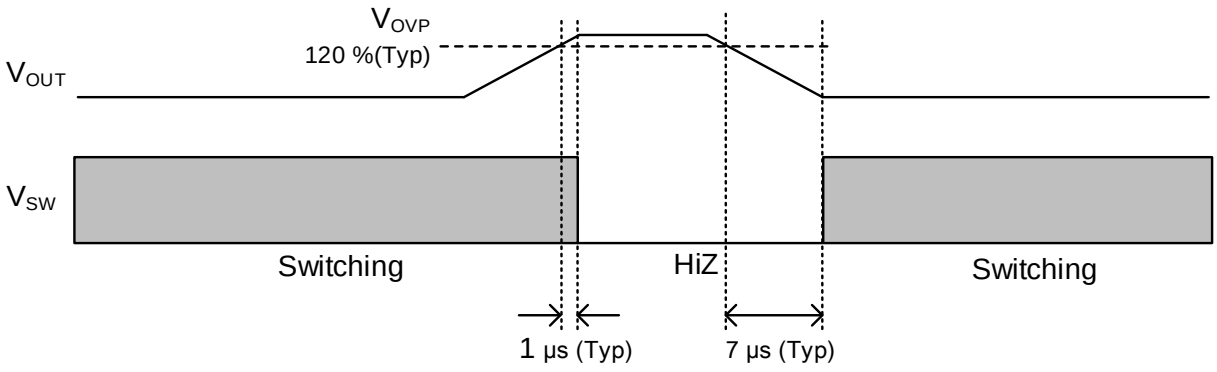


Figure 47. OVP Timing Chart

Selection of Components Externally Connected

Contact us if not use the recommended constant in this section.

The figure below is the application sample circuit.

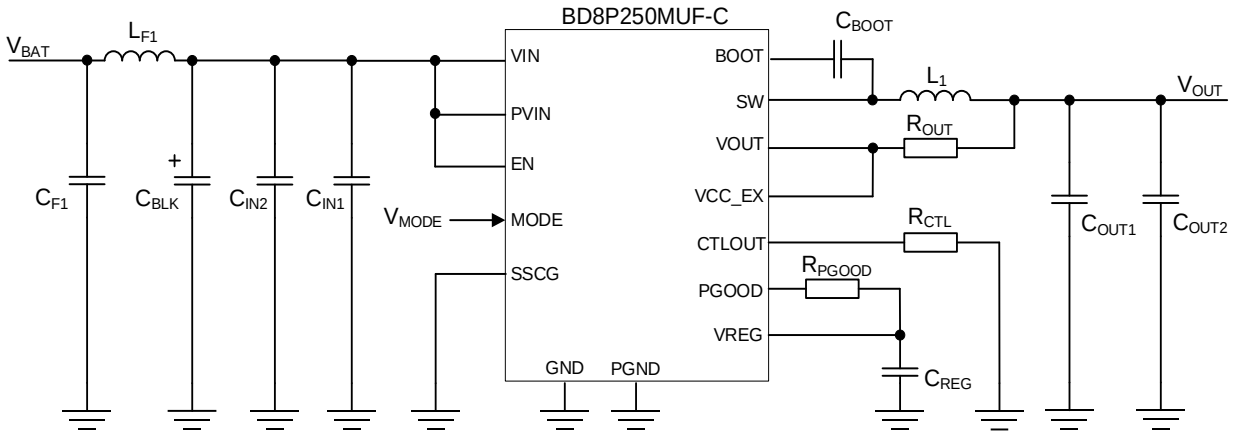


Figure 48. Application Sample Circuit 1

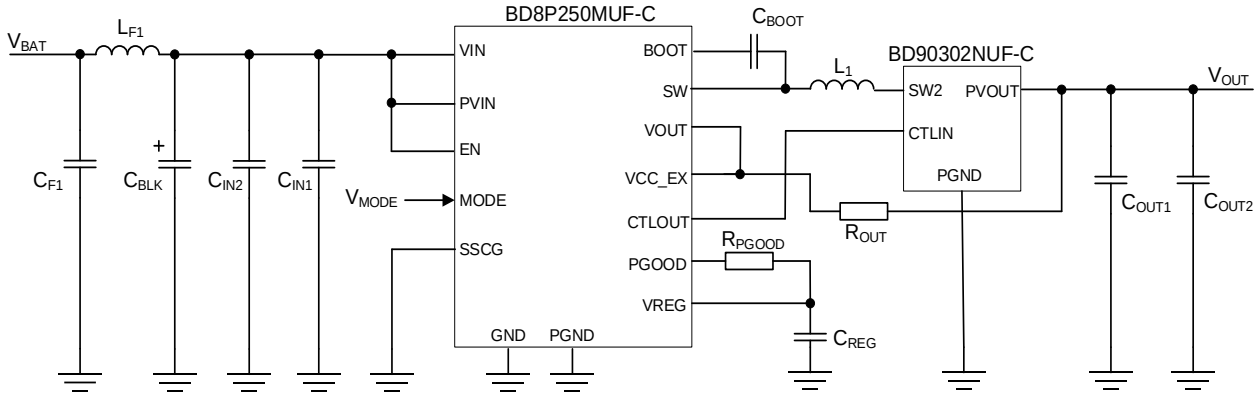


Figure 49. Application Sample Circuit 2

Selection of Components Externally Connected - continued

1. Selection of the inductor L_1 value
Role of the inductor in the switching regulator is that it also serves as a filter for smoothing the output voltage to supply a continuous current to the load. The Inductor ripple current ΔI_L that flows to the inductor becomes small when an inductor with a large inductance value is selected. Consequently, the voltage of the output ripple ΔV_{P-P} also becomes small. It is the trade-off between the size and the cost of the inductor.

The inductance of the inductor is shown in the following equation:

$$L = \frac{(V_{IN(Max)} - V_{OUT}) \times V_{OUT}}{V_{IN(Max)} \times f_{SW} \times \Delta I_L} \quad [\mathrm{H}]$$

Where:

$V_{IN\ (Max)}$	is the maximum input voltage
V_{OUT}	is the output voltage
f_{SW}	is the switching frequency
ΔI_L	is the peak to peak inductor current

In current mode control, sub-harmonic oscillation may happen. The slope compensation circuit is integrated into the IC in order to prevent sub-harmonic oscillation. The sub-harmonic oscillation depends on the rate of increase of output switch current. If the inductor value is too small, the sub-harmonic oscillation may happen because the inductor ripple current ΔI_L is increased. And if the inductor value is too large, the feedback loop may not achieve stability because the inductor ripple current ΔI_L is decreased. Therefore, use an inductor value of the inductor within the range of 2.2 µH to 10 µH.
The smaller the ΔI_L, the smaller the Inductor core loss (iron loss), and the smaller is the loss due to ESR of the output capacitor. In effect, ΔV_{P-P} (Output peak-to-peak ripple voltage) will be reduced. ΔV_{P-P} is shown in the following equation.

$$\Delta V_{P-P} = \Delta I_L \times ESR + \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}} \quad [\mathrm{V}] \qquad \text{(a)}$$

Where:

ESR	is the equivalent series resistance of the output capacitor
C_{OUT}	is the output capacitance
ΔI_L	is the peak to peak inductor current
f_{SW}	is the switching frequency

Generally, even if ΔI_L is somewhat large, the ΔV_{P-P} target is satisfied because the ceramic capacitor has a very-low ESR. It also contributes to the miniaturization of the application board. Also, because of the lower rated current, smaller inductor is possible since the inductance is small. The disadvantages are increase in core losses in the inductor and the decrease in maximum output current. When other capacitors (electrolytic capacitor, tantalum capacitor, and electro conductive polymer etc.) are used for output capacitor C_{OUT}, check the ESR from the manufacturer's data sheet and determine the ΔI_L to fit within the acceptable range of ΔV_{P-P}. Especially in the case of electrolytic capacitor, because the decrease in capacitance at low temperatures is significantly large, this will make ΔV_{P-P} increase. When using capacitor at low temperature, this is an important consideration.

The shielded type (closed magnetic circuit type) is the recommended type of inductor to be used. Please note that magnetic saturation may occur. It is important not to saturate the core in all cases. Precautions must be taken into account on the given provisions of the current rating because it differs on every manufacturer. Please confirm the rated current at maximum ambient temperature of application to the manufacturer.

Selection of Components Externally Connected - continued

2. Selection of Output Capacitor C_{OUT}

The output capacitor is selected based on the ESR that is required from the equation (a). ΔV_{P-P} can be reduced by using a capacitor with a small ESR. The ceramic capacitor is the best option that meets this requirement. It is because not only does it has a small ESR but the ceramic capacitor also contributes to the size reduction of the application circuit. Please confirm the frequency characteristics of ESR from the datasheet of the manufacturer, and consider a low ESR value for the switching frequency being used. It is necessary to consider the ceramic capacitor because the DC biasing characteristic is important. For the voltage rating of the ceramic capacitor, twice or more than the maximum output voltage is usually required. By selecting a high voltage rating, it is possible to reduce the influence of DC bias characteristics. Moreover, in order to maintain good temperature characteristics, the one with the characteristics of X7R or better is recommended. Because the voltage rating of a large ceramic capacitor is low, the selection becomes difficult for an application with high output voltage. In that case, please connect multiple ceramic capacitors in series or select electrolytic capacitor. Consider having a voltage rating of 1.2 times or more of the output voltage when using electrolytic capacitor. Electrolytic capacitors have a high voltage rating, large capacitance, small amount of DC biasing characteristics, and are generally reasonable. Since the electrolytic capacitor is usually OPEN when it fails, it is effective to use for applications when reliability is required such as automotive. But there are disadvantages such as, ESR is relatively high, and decreases capacitance value at low temperatures. In this case, please take note that ΔV_{P-P} may increase at low temperature conditions. Moreover, consider the lifetime characteristic of this capacitor because it has a possibility to dry up. A tantalum capacitor and a conductive polymer hybrid capacitor have excellent temperature characteristics unlike the electrolytic capacitor. Moreover, since their ESR is smaller than an electrolytic capacitor, the ripple voltage is relatively-small over a wide temperature range. Since these capacitors have almost no DC bias characteristics, design will be easier. Regarding voltage rating, the tantalum capacitor is selected such that its capacitance is twice the value of the output voltage, and for the conductive polymer hybrid capacitor, it is selected such that the voltage rating is 1.2 times the value of the output voltage. The disadvantage of a tantalum capacitor is that it is SHORTED when it is destroyed, and its breakdown voltage is low. It is not generally selected in an application that reliability is a demand such as in automotive. An electro conductive polymer hybrid capacitor is OPEN when destroyed. Though it is effective for reliability, its disadvantage is that it is generally expensive.

To improve the performance of ripple voltage in this condition, following is recommended:

1. Use low ESR capacitor like ceramic or conductive polymer hybrid capacitor.
2. Use a capacitor C_{OUT} with a higher capacitance value.

These capacitors are rated in ripple current. The RMS values of the ripple current that can be obtained in the following equation must not exceed the ripple current rating.

$$I_{CO(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \quad [\text{A}]$$

Where:

$I_{CO(RMS)}$	is the value of the ripple electric current
ΔI_L	is the peak to peak inductor current

In addition, for the total value of capacitance in the output line C_{OUT}(Max), choose a capacitance value less than the value obtained by the following equation:

$$C_{OUT(Max)} < \frac{t_{SS(Min)} \times (I_{SW(Min)} - I_{SWSTART(Max)})}{V_{OUT}} \quad [\text{F}]$$

Where:

$I_{SW(Min)}$	is the OCP operation switch current (Min)
$t_{SS(Min)}$	is the Soft Start Time (Min)
$I_{SWSTART(Max)}$	is the maximum output current during startup
V_{OUT}	is the output voltage

Startup failure may happen if the limits from the above-mentioned are exceeded. Especially if the capacitance value is extremely large, over-current protection may be activated by the inrush current at startup preventing the output to turn on. Please confirm this on the actual application. For stable transient response, the loop is dependent to C_{OUT}. Please select after confirming the setting of the phase compensation circuit.

Also, in case of large changing input voltage and load current, select the capacitance accordingly by verifying that the actual application setup meets the required specification.

Selection of Components Externally Connected - continued

3. Selection of Input Capacitor C_{IN}, C_{BLK}
   The input capacitor is usually required for two types of decoupling: capacitors C_{IN} and bulk capacitors C_{BLK}.
   For the decoupling capacitors, two ceramic capacitors are required: C_{IN1} with a small capacitance and C_{IN2} with a large capacitance. C_{IN1} and C_{IN2} can reduce the switching noise and ripple noise, respectively. The effects of these ceramic capacitors are obtained by placing them as close as possible to the PVIN and VIN pins. For C_{IN2}, it is recommended to use a capacitor with the capacitance value of 2.3 µF or more, also, with the voltage rating that is 1.2 times or more of the maximum input voltage and 2 times or more of the normal input voltage.
   The capacitor value including device variation, temperature change, DC bias change, and aging change must be larger than minimum value. Also, the IC might not operate properly when the PCB layout or the position of the capacitor is not good. Please check “Notes on the PCB Layout Design” on page 34, 35.

   The bulk capacitor is optional. The bulk capacitor prevents the decrease in the line voltage and serves as a backup power supply to keep the input voltage constant. A low ESR electrolytic capacitor with large capacitance is suitable for the bulk capacitor. It is necessary to select the best capacitance value for each set of application. In that case, please take note not to exceed the rated ripple current of the capacitor.

   The RMS value of the input ripple current $I_{CIN(RMS)}$ is obtained in the following equation:

$$I_{CIN(RMS)} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad [A]$$

   Where:
   $I_{OUT(MAX)}$ is the maximum output current.

   In addition, in automotive and other applications requiring high reliability, it is recommended to connect the capacitors in parallel to accommodate multiple electrolytic capacitors and minimize the chances of drying up. For ceramic capacitors, it is recommended to make two series + two parallel structures to decrease the risk of capacitor destruction due to short circuit conditions.

   When the impedance on the input side is high for some reason (because the wiring from the power supply to VIN is long, etc.), then high capacitance is needed. In actual conditions, it is necessary to verify that there are no problems like IC turns off, or the output overshoots due to the change in V_{IN} at transient response.

4. Selection of the Bootstrap Capacitor
   Bootstrap capacitor C_{BOOT} value shall be 0.1 µF. Connect the bootstrap capacitor between SW pin and BOOT pin. Recommended products are described in Application Examples1 on page 27.

5. Selection of the VREG Capacitor.
   VREG capacitor C_{REG} shall be 1.0 µF(Typ) ceramic capacitor. Connect the VREG capacitor between VREG pin and GND. Recommended products are described in Application Examples1 on page 27.

Application Examples 1

Table1. Specification Example 1

Parameter	Symbol	Specification Case
Product Name	IC	BD8P250MUF-C
Input Voltage	V_{IN}	8 V to 18 V
Output Voltage	V_{OUT}	5.0 V
Output Current	I_{OUT}	Typ 1.0 A / Max 1.5 A
Switching Frequency	f_{SW}	2.2 MHz
Operation Temperature	Ta	-40°C to +105 °C

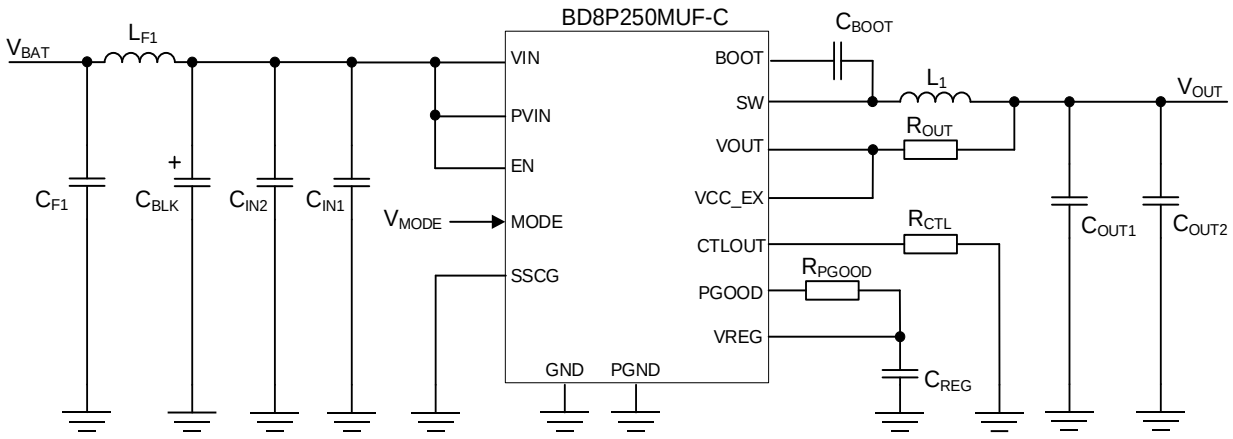


Figure 50. Reference Circuit 1

Table 2. Parts List 1

No	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{BLK}	φ10 mm×L10 mm	220 µF, 50 V	UCD1H221MNL1GS	Electrolytic capacitor	NICHICON
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{IN2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475K	Ceramic	MURATA
C_{BOOT}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{REG}	1608	1.0 µF, X7R, 16 V	GCM188R71C105K	Ceramic	MURATA
R_{OUT}	-	Short	-	-	-
R_{CTL}	1005	1 kΩ, 1 %, 1/16 W	MCR01MZPF1001	Chip resistor	ROHM
R_{PGOOD}	1005	100 kΩ, 1 %, 1/16 W	MCR01MZPF1003	Chip resistor	ROHM
L_1	W6.0×H4.5×L6.3 mm^3	3.3 µH	CLF6045NIT-3R3N-D	Inductor	TDK
C_{OUT1}	3225	22 µF, R, 10 V	GCM32ER11A226K	Ceramic	MURATA
C_{OUT2}	3225	22 µF, R, 10 V	GCM32ER11A226K	Ceramic	MURATA
C_{F1}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475K	Ceramic	MURATA
L_{F1}	W6.0×H4.5×L6.3 mm^3	2.2 µH	CLF6045NIT-2R2N-D	Inductor	TDK

Application Examples 1 – continued

(V_{IN} = V_{EN}, Ta = 25°C)

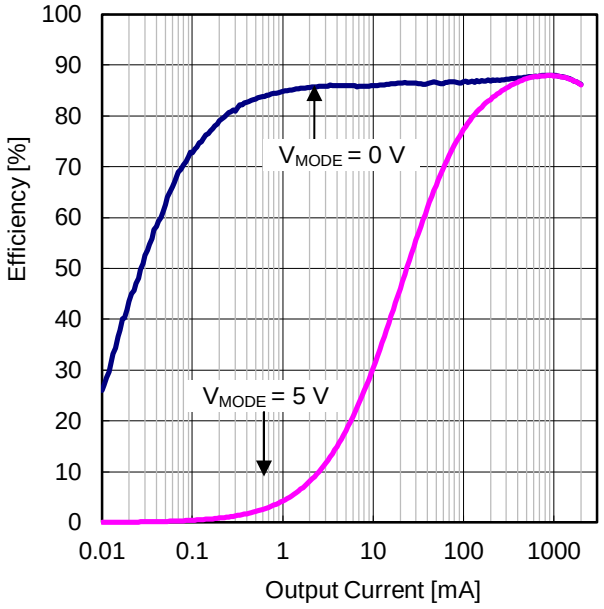


Figure 51. Efficiency vs Output Current
(V_{IN} = 12 V)

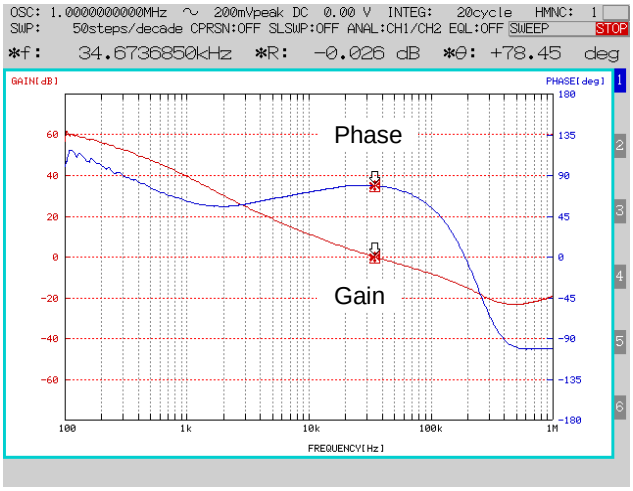


Figure 52. Frequency Characteristic
(V_{IN} = 12 V, I_{OUT} = 1 A)

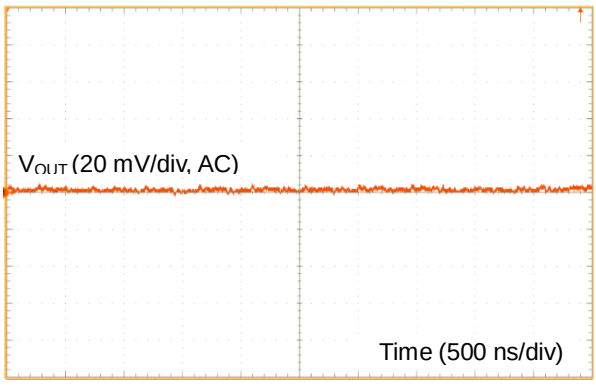


Figure 53. Output Ripple Voltage
(V_{IN} = 12 V, I_{OUT} = 1 A)

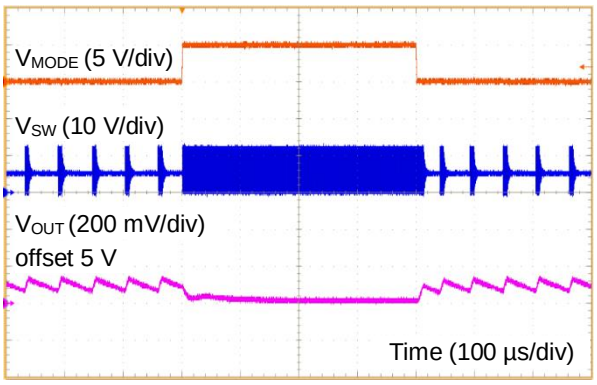


Figure 54. MODE ON/OFF Response
(V_{IN} = 12 V, I_{OUT} = 50 mA)

Application Examples 1 – continued

（V_{IN} = V_{EN}, Ta = 25°C）

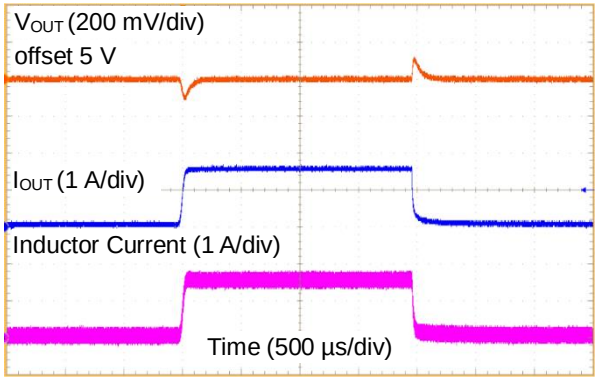


Figure 55. Load Response 1
(V_{IN} = 12 V, V_{MODE} = 5 V, I_{OUT} = 0 A to 1.5 A)

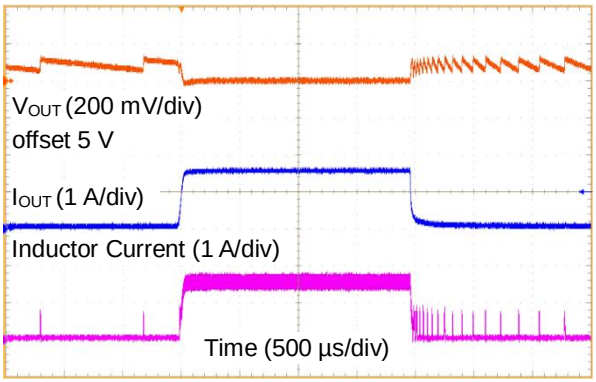


Figure 56. Load Response 2
(V_{IN} = 12 V, V_{MODE} = 0 V, I_{OUT} = 0 A to 1.5 A)

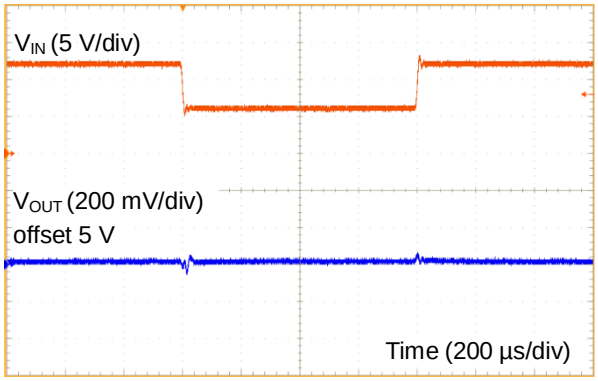


Figure 57. Line Response 1
(V_{IN} = 12 V to 6 V, I_{OUT} = 1 A)

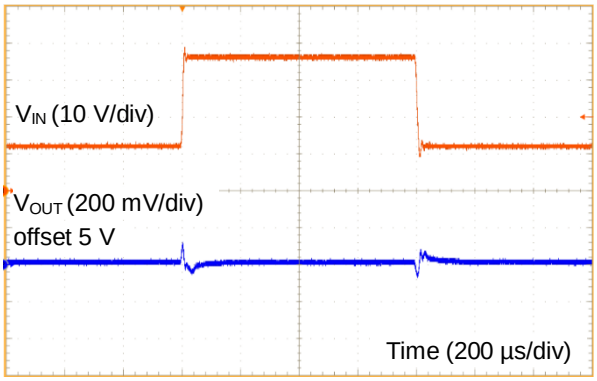


Figure 58. Line Response 2
(V_{IN} = 12 V to 36 V, I_{OUT} = 1 A)

Application Examples 2

Table 3. Specification Example 2

Parameter	Symbol	Specification Case
Product Name 1	IC_1	BD8P250MUF-C
Product Name 2	IC_2	BD90302NUF-C
Input Voltage	V_{IN}	4 V to 18 V
Output Voltage	V_{OUT}	5.0 V
Output Current	I_{OUT}	Typ 0.4 A / Max 0.6 A
Switching Frequency	f_{SW}	2.2 MHz
Operation Temperature	Ta	-40 °C to +105 °C

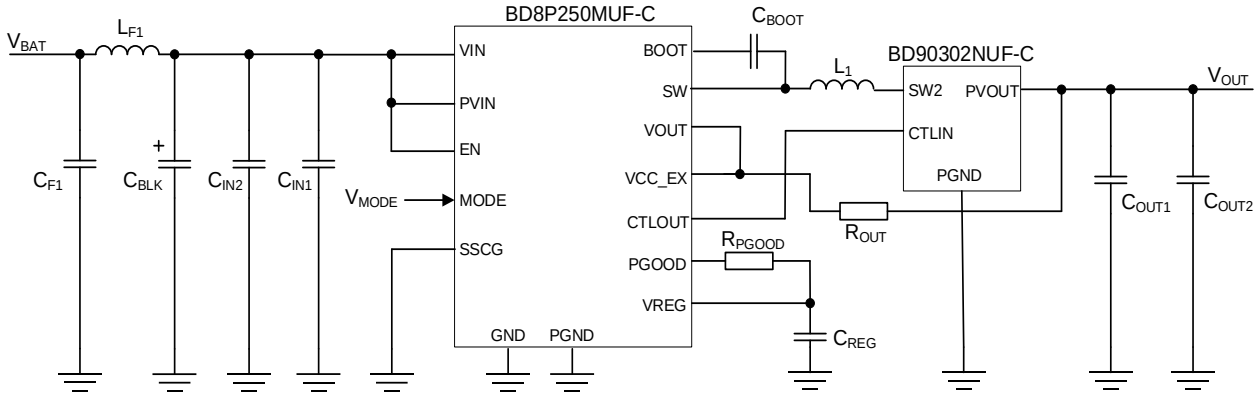


Figure 59. Reference Circuit 2

Table 4. Parts List 2

No	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{BLK}	φ10 mm×L10 mm	220 µF, 50 V	UCD1H221MNL1GS	Electrolytic capacitor	NICHICON
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{IN2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475K	Ceramic	MURATA
C_{BOOT}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{REG}	1608	1.0 µF, X7R, 16 V	GCM188R71C105K	Ceramic	MURATA
R_{OUT}	-	Short	-	-	-
R_{PGOOD}	1005	100 kΩ, 1 %, 1/16 W	MCR01MZPF1003	Chip resistor	ROHM
L_1	W6.0×H4.5×L6.3 mm^3	3.3 µH	CLF6045NIT-3R3N-D	Inductor	TDK
C_{OUT1}	3225	22 µF, R, 10 V	GCM32ER11A226K	Ceramic	MURATA
C_{OUT2}	3225	22 µF, R, 10 V	GCM32ER11A226K	Ceramic	MURATA
C_{F1}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475K	Ceramic	MURATA
L_{F1}	W6.0×H4.5×L6.3 mm^3	2.2 µH	CLF6045NIT-2R2N-D	Inductor	TDK

Application Examples 2 – continued

(V_{IN} = V_{EN}, Ta = 25°C)

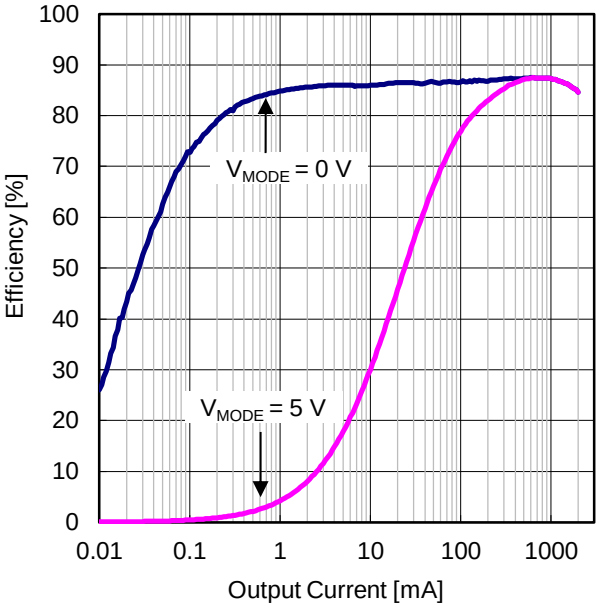


Figure 60. Efficiency vs Output Current
(V_{IN} = 12 V)

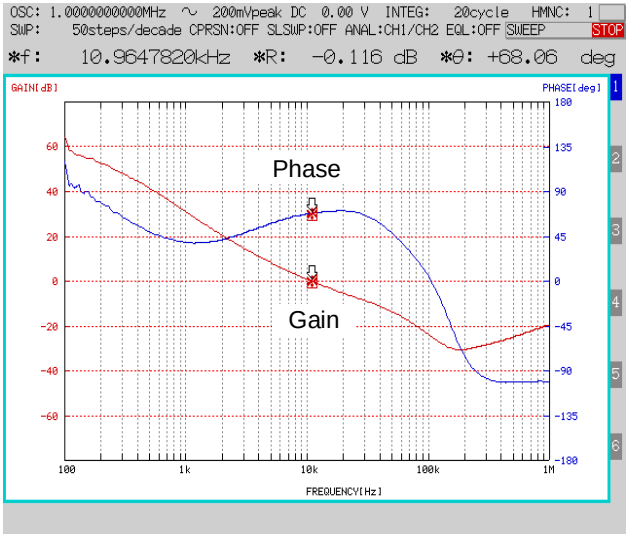


Figure 61. Frequency characteristic
(V_{IN} = 4 V, I_{OUT} = 0.4 A)

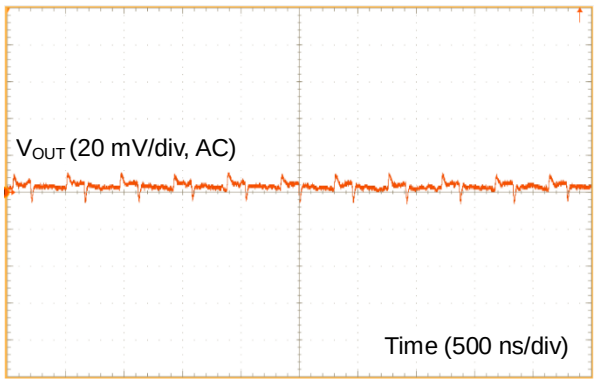


Figure 62. Output Ripple Voltage
(V_{IN} = 4 V, I_{OUT} = 0.4 A)

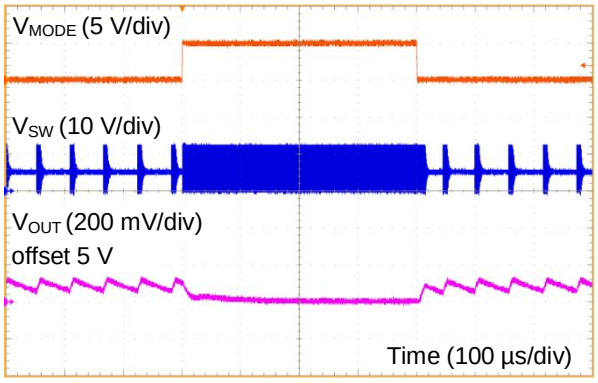


Figure 63. MODE ON/OFF Response
(V_{IN} = 12 V, I_{OUT} = 50 mA)

Application Examples 2 – continued

(V_{IN} = V_{EN}, Ta = 25°C)

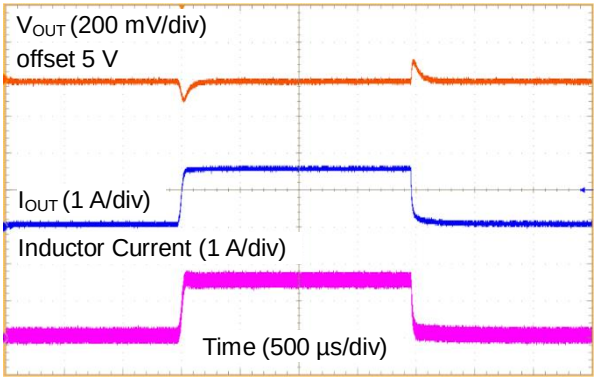


Figure 64. Load Response 1
(V_{IN} = 12 V, V_{MODE} = 5 V, I_{OUT} = 0 A to 1.5 A)

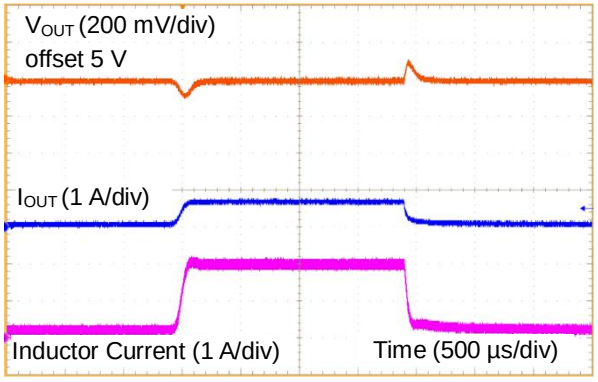


Figure 65. Load Response 2
(V_{IN} = 4 V, I_{OUT} = 0 A to 0.6 A)

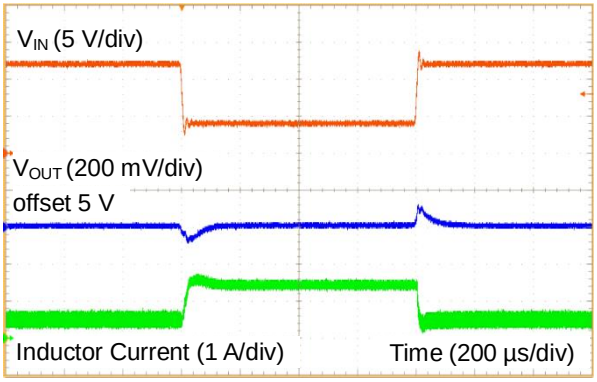


Figure 66. Line Response 1
(V_{IN} = 12 V to 4 V, I_{OUT} = 0.4 A)

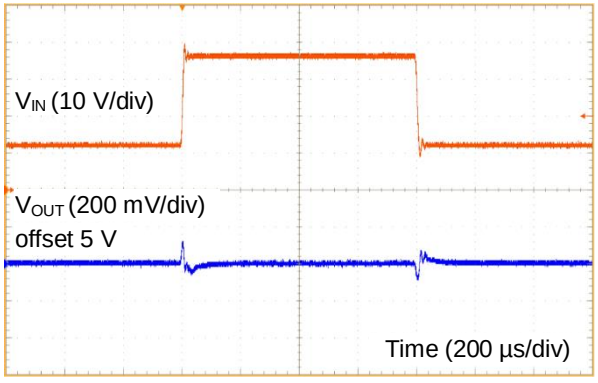


Figure 67. Line Response 2
(V_{IN} = 12 V to 36 V, I_{OUT} = 1 A)

Automotive Power Supply Line Circuit

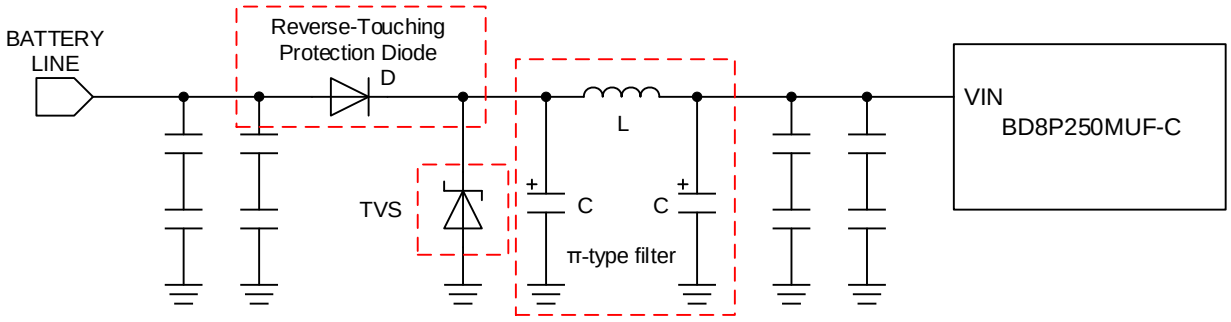


Figure 68. Automotive Power Supply Line Circuit

As a reference, the automotive power supply line circuit example is given in Figure 68.
π-type filter is a third-order LC filter. In general, it is used in combination with decoupling capacitors for high frequency. Large attenuation characteristics can be obtained and thus excellent characteristic as a EMI filter. Devices used for π-type filters should be placed close to each other.
TVS (Transient Voltage Suppressors) is used for primary protection of the automotive power supply line. Since it is necessary to withstand high energy of load dump surge, a general zener diode is insufficient. Recommended device is shown in the following table.
In addition, a reverse polarity protection diode is needed considering if a power supply such as BATTERY is accidentally connected in the opposite direction.

Table 5. Reference Parts of Automotive Power Supply Line Circuit

Device	Part name (series)	Manufacturer	Device	Part name (series)	Manufacturer
L	CLF series	TDK	TVS	SMB series	Vishay
L	XAL series	Coilcraft	D	S3A to S3M series	Vishay
C	CJ series / CZ series	NICHICON			

Recommended Parts Manufacturer List

Shown below is the list of the recommended parts manufacturers for reference.

Type	Manufacturer	URL
Electrolytic Capacitor	NICHICON	www.nichicon.co.jp
Ceramic Capacitor	Murata	www.murata.com
Hybrid Capacitor	Suncon	www.sunelec.co.jp
Inductor	TDK	product.tdk.com
Inductor	Coilcraft	www.coilcraft.com
Inductor	SUMIDA	www.sumida.com
Diode	Vishay	www.vishay.com
Diode/Resistor	ROHM	www.rohm.com

PCB Layout Design

PCB layout design for DC/DC converter power supply IC is as important as the circuit design. Appropriate layout can avoid various problems caused by power supply circuit. Figure 69-a to 69-c figure show the current path in a buck converter circuit. The Loop 1 in Figure 69-a is a current path when H-side switch is ON and L-side switch is OFF, the Loop 2 in Figure 69-b is when H-side switch is OFF and L-side switch is ON. The thick line in Figure 69-c shows the difference between Loop1 and Loop2. The current in thick line change sharply each time the switching element H-side and L-side switch change from OFF to ON, and vice versa. These sharp changes induce several harmonics in the waveform. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more detail refer to application note of switching regulator series “PCB Layout Techniques of Buck Converter”.

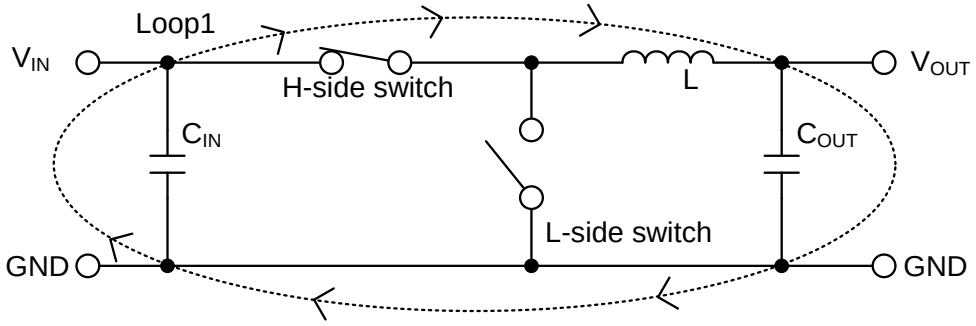


Figure 69-a. Current path when H-side switch = ON, L-side switch = OFF

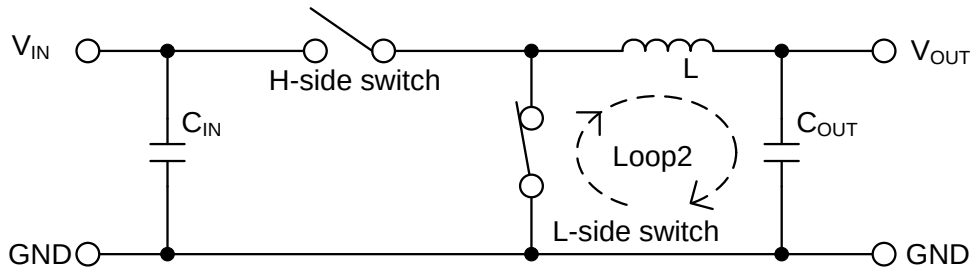


Figure 69-b. Current path when H-side switch = OFF, L-side switch = ON

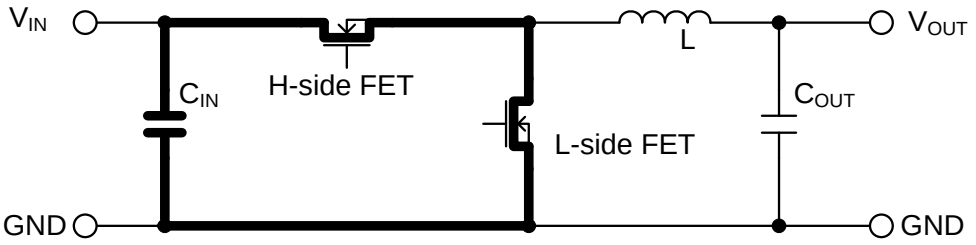


Figure 69-c. Difference of current and critical area in layout

PCB Layout Design – continued

When designing the PCB layout, please pay extra attention to the following points.

1. Place the input decoupling capacitors of 4.7 µF (C_{IN2}) for the VIN pin (2-pin) and 0.1 µF (C_{IN1}) for the PVIN pin (3-, 4-, and 5-pin) so that the distance of the route between the PVIN and PGND (7-, 8-pin) pins is as short as possible. The reduction in high-frequency noise is more effective when the capacitor with the smaller capacitance of 0.1 µF (C_{IN1}) is placed closer to the PVIN pin than the capacitor of 4.7 µF (C_{IN2}).
2. Place the IC, input capacitor, output inductor, and output capacitor on the same surface layer of the board, and connect the parts on the same layer.
3. Place the ground plane on the layer nearest to the surface layer on which the IC is placed.
4. The GND pin (22-pin) is the reference ground and the PGND pin is the power ground. These pins may be connected via the back surface of the IC. However, since the power ground on the input capacitor side contains the noise component of the switching frequency, it is recommended to separate the power ground from the adjacent reference ground pattern. Connect the separated power ground to the ground plane using as many vias as possible.
5. Place the bypass capacitor between the VREG (23-pin) and GND pins at a position as close as possible to the pin.
6. Place the capacitors connected between the SW pin (12-, 13-, and 14-pin) and the BOOT (15-pin) at positions as close as possible to each pin.
7. To minimize the radiated noise from the switching node, keep the distance from the SW pin to the inductor short, and do not extend the area of copper foil pattern more than necessary.
8. Place the output capacitor near the inductor and the power ground.
9. Place the wire for the feedback line from the output away from the inductor and the switching node. If the wire is affected by the external noise, an error can occur in the output voltage or the operation can be destabilized. Therefore, move the feedback line to the back surface through a via, and connect the line to the VOUT pin (20-pin).
10. R_{OUT} (optional) is for measuring the frequency characteristics of the feedback. By inserting a resistor in R_{OUT}, the frequency characteristics (phase margin) of the feedback can be measured. R_{OUT} should be short-circuited for the normal use.

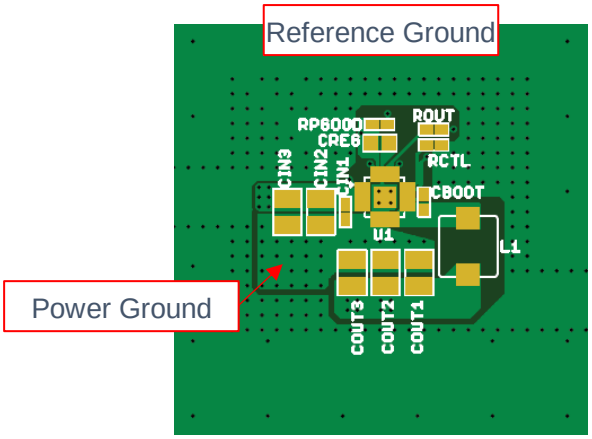


Figure 70. Evaluation Board Layout Example
(Buck DC/DC Converter)

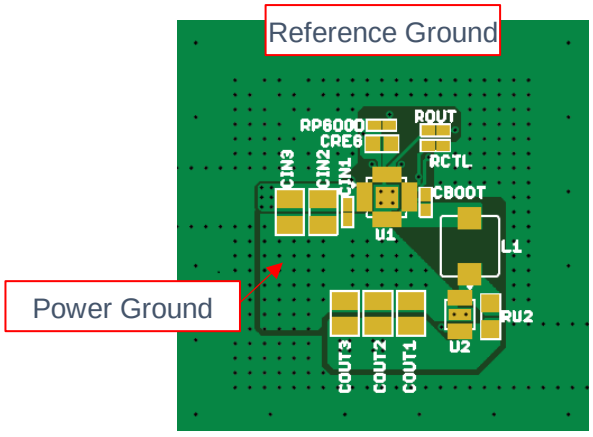


Figure 71. Evaluation Board Layout Example
(Buck-Boost DC/DC Converter)

Power Dissipation

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. The ambient temperature Ta is to be 125 °C or less.
2. The chip junction temperature Tj is to be 150 °C or less.

The chip junction temperature Tj can be considered in the following two patterns:

1. To obtain Tj from the package surface center temperature Tt in actual use

$$Tj = Tt + \psi_{JT} \times W \ [°C]$$

2. To obtain Tj from the ambient temperature Ta

$$Tj = Ta + \theta_{JA} \times W \ [°C]$$

Where:

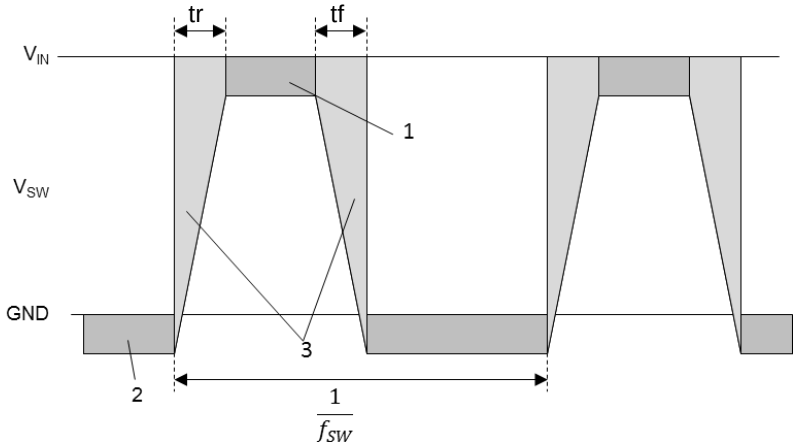
ψ_{JT}	is junction to top characterization parameter (Refer to page 6)
θ_{JA}	is junction to ambient (Refer to page 6)

The heat loss W of the IC can be obtained by the formula shown below:

$$W = R_{ONH} \times {I_{OUT}}^2 \times \frac{V_{OUT}}{V_{IN}} + R_{ONL} \times {I_{OUT}}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + V_{IN} \times I_{CC} + \frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW} \ [W]$$

Where:

R_{ONH}	is the High Side FET ON Resistance (Refer to page 8) [Ω]
R_{ONL}	is the Low Side FET ON Resistance (Refer to page 8) [Ω]
I_{OUT}	is the Load Current [A]
V_{OUT}	is the Output Voltage [V]
V_{IN}	is the Input Voltage [V]
I_{CC}	is the Circuit Current [A] (Typ : 50 µA)
tr	is the Switching Rise Time [s] (Typ : 5 ns)
tf	is the Switching Fall Time [s] (Typ : 5 ns)
f_{SW}	is the Switching Frequency (Refer to page 8) [Hz]

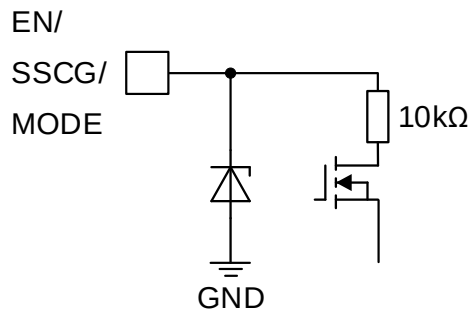


1. $R_{ONH} \times {I_{OUT}}^2$
2. $R_{ONL} \times {I_{OUT}}^2$
3. $\frac{1}{2} \times (tr + tf) \times V_{IN} \times I_O \times f_{SW}$

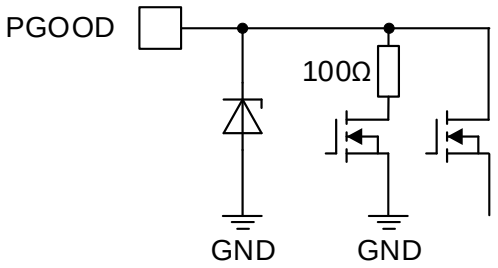
Figure 72. SW Waveform

I/O Equivalence Circuits

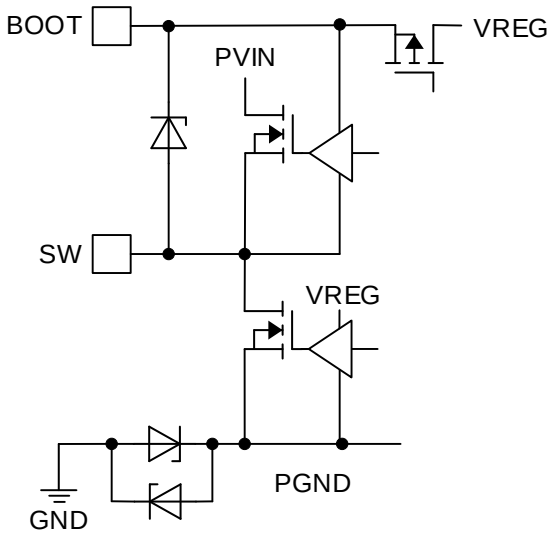
1.EN, 17.SSCG, 24.MODE



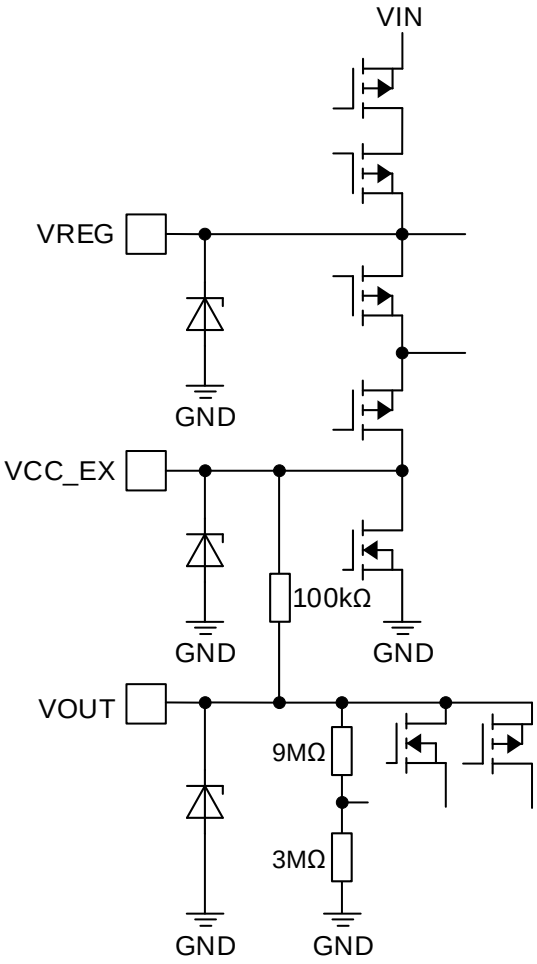
19. PGOOD



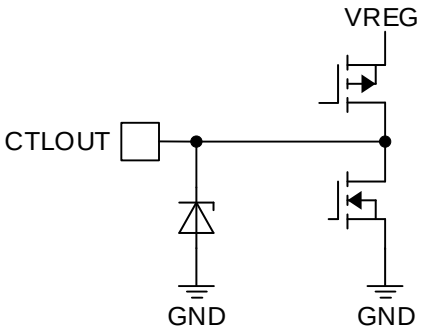
12,13,14.SW, 15.BOOT



20.VOUT, 21.VCC_EX, 23.VREG



18. CTLOUT



*Resistance value is Typ.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

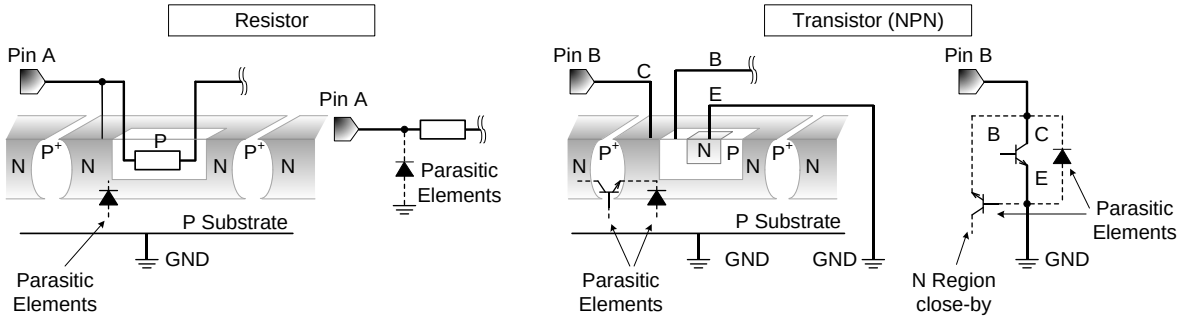


Figure 73. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B	D	8	P	2	5	0	M	U	F	-	CE 2

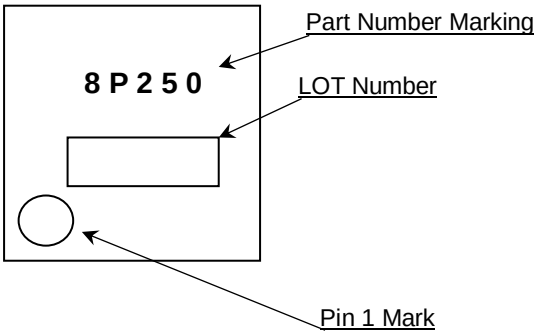
Part Number

Package
MUF: VQFN024FV4040

Product class
C for Automotive applications
Packaging and forming specification
E2: Embossed tape and reel

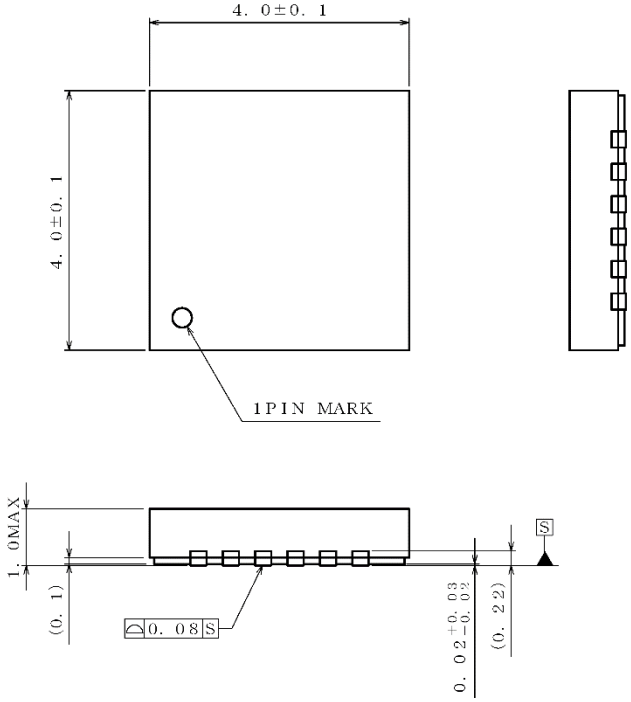
Marking Diagram

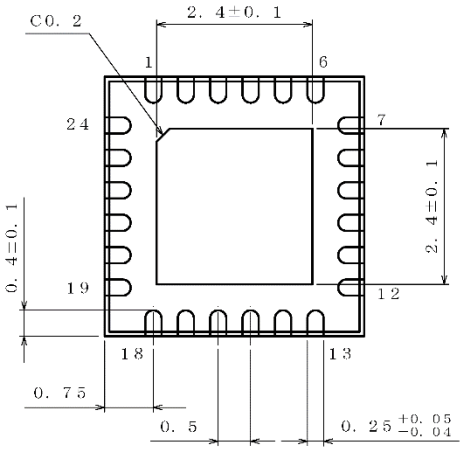
VQFN24FV4040 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VQFN24FV4040





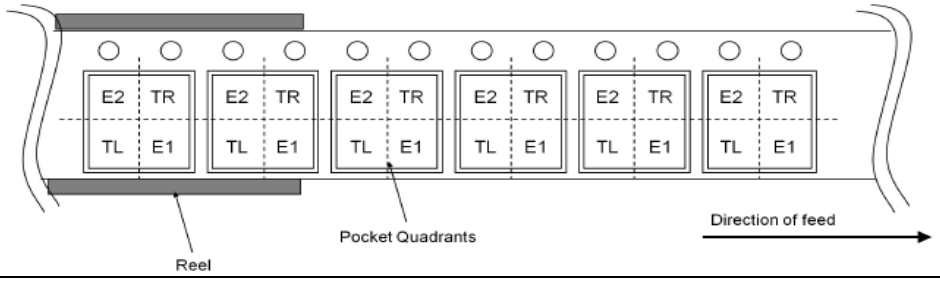
(UNIT:mm)

PKG:VQFN24FV4040
Drawing No. EX394-5001

NOTE: Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
11.Sep.2018	001	New Release

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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