



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.19.2005
Rev. 1.1	Revised I _{SB1} /I _{DR} Revised Test Condition of I _{CC}	Oct.31.2005
Rev. 1.2	Added -45ns Spec.	Sep.20.2006
Rev. 1.3	Added P-DIP PKG	Jan.12.2007
Rev. 1.4	Revised Test Condition of I _{SB1} /I _{DR}	May.14.2007
Rev. 1.5	Adding PKG type : 44 TSOP-II	Jun.4.2007
Rev. 2.0	Adding SL Spec. Revised <u>ABSOLUTE MAXIMUM RATINGS</u>	Jul.11.2007

FEATURES

- Fast access time : 35/45/55/70ns
- Low power consumption:
Operating current : 50/45/40/30mA (TYP.)
Standby current : 5 μ A (TYP.)
- Single 4.5V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Lead free and green package available**
- Package : 32-pin 450 mil SOP
 - 32-pin 8mm x 20mm TSOP-I
 - 32-pin 8mm x 13.4mm STSOP
 - 36-ball 6mm x 8mm TFBGA
 - 32-pin 600 mil P-DIP
 - 44-pin 400 mil TSOP-II

GENERAL DESCRIPTION

The LY625128 is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

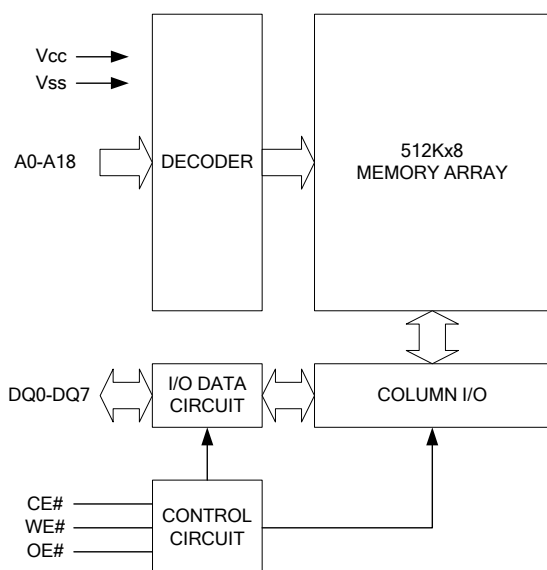
The LY625128 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY625128 operates from a single power supply of 4.5V ~ 5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} TYP.)	Operating(I _{CC} ,TYP.)
LY625128(SL)	0 ~ 70°C	4.5 ~ 5.5V	35/45/55/70ns	5 μ A (LL)	50/45/40/30mA
LY625128(SLE)	-20 ~ 80°C	4.5 ~ 5.5V	35/45/55/70ns	5 μ A (LL)	50/45/40/30mA
LY625128(LL)	0 ~ 70°C	4.5 ~ 5.5V	35/45/55/70ns	5 μ A (LL)	50/45/40/30mA
LY625128(LLE)	-20 ~ 80°C	4.5 ~ 5.5V	35/45/55/70ns	5 μ A (LL)	50/45/40/30mA
LY625128(LLI)	-40 ~ 85°C	4.5 ~ 5.5V	35/45/55/70ns	5 μ A (LL)	50/45/40/30mA

FUNCTIONAL BLOCK DIAGRAM

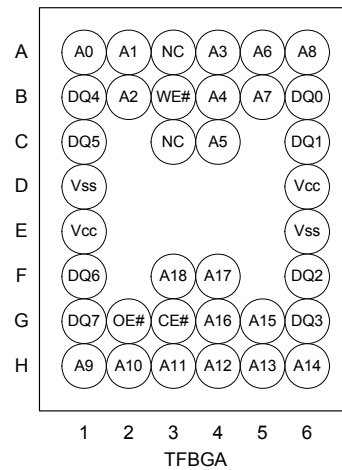
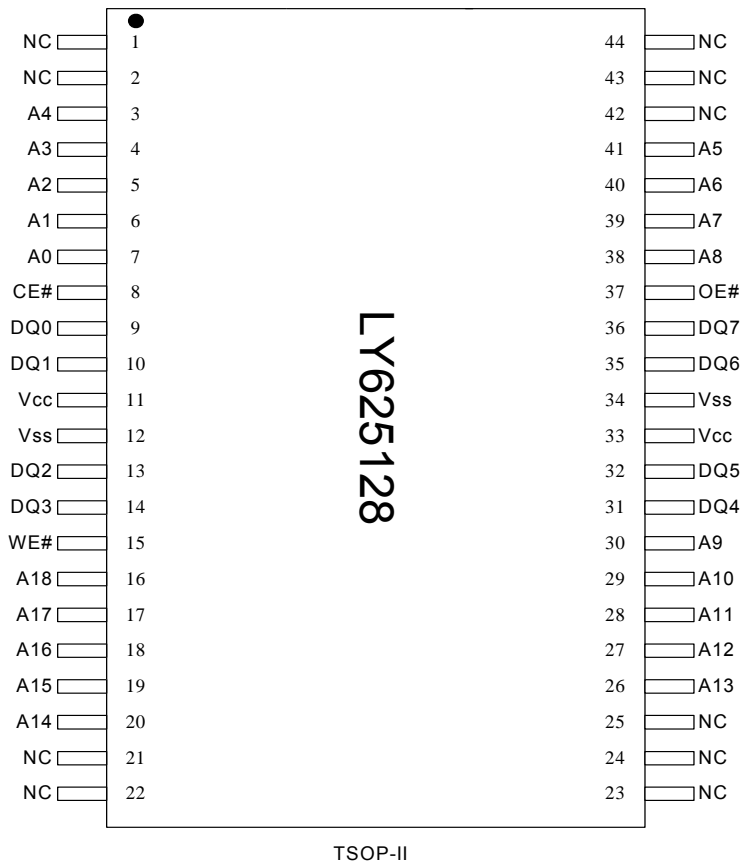
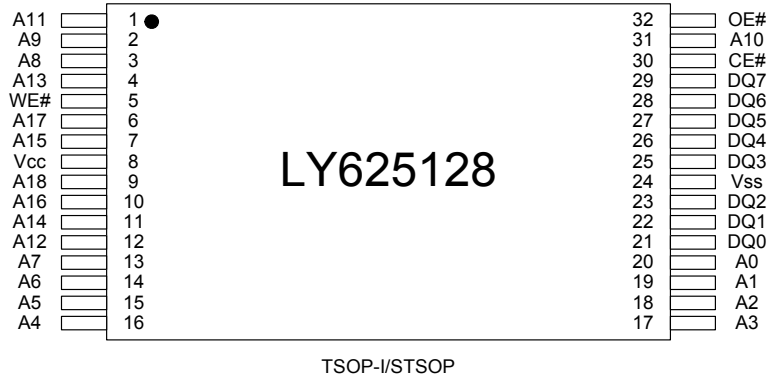
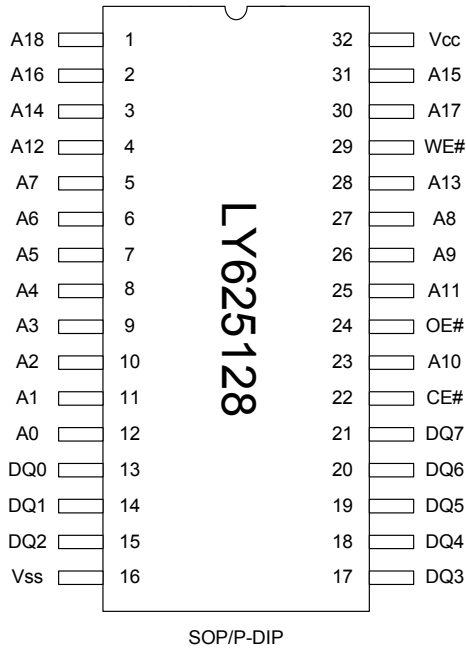


PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection



PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA
Soldering Temperature (under 10 sec)	T _{SOLDER}	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB1}
Output Disable	L	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ³	MAX.	UNIT
Supply Voltage	V _{CC}		4.5	5.0	5.5	V
Input High Voltage	V _{IH} ¹		2.4	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL} ¹		-0.2	-	0.6	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = 0.2V, I _{I/O} = 0mA other pins at 0.2V or V _{CC} - 0.2V	-35	50	80	mA
			-45	45	70	mA
			-55	40	60	mA
			-70	30	50	mA
	I _{CC1}	Cycle time = 1μs CE# = 0.2V, I _{I/O} = 0mA other pins at 0.2V or V _{CC} - 0.2V	-	4	10	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V	-SL	5	25	μA
		Other pins at 0.2V or V _{CC} -0.2V	-LL	5	50	μA

Notes: 1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.

2. Over/Undershoot specifications are characterized, not 100% tested.

3. Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

**CAPACITANCE (TA = 25°C, f = 1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -2mA/4mA

AC ELECTRICAL CHARACTERISTICS**(1) READ CYCLE**

PARAMETER	SYM.	LY625128-35		LY625128-45		LY625128-55		LY625128-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	35	-	45	-	55	-	70	-	ns
Address Access Time	t _{AA}	-	35	-	45	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	35	-	45	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	25	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	15	-	20	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	15	-	20	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	10	-	10	-	ns

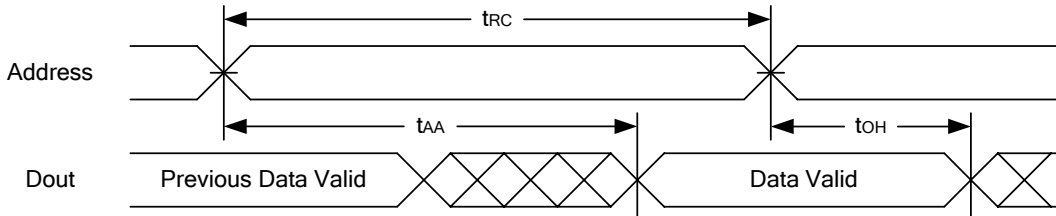
(2) WRITE CYCLE

PARAMETER	SYM.	LY625128-35		LY625128-45		LY625128-55		LY625128-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	35	-	45	-	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	30	-	40	-	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	30	-	40	-	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	25	-	35	-	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	15	-	20	-	20	-	25	ns

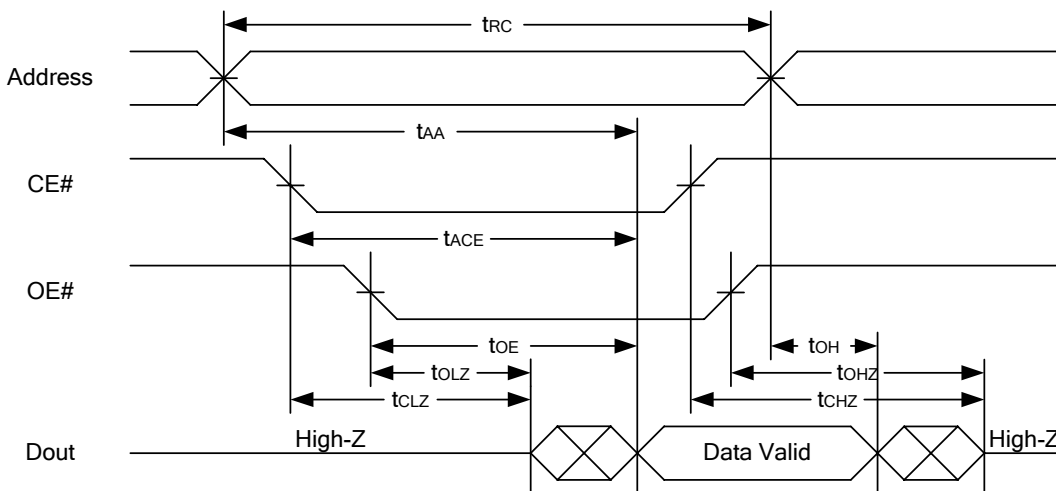
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

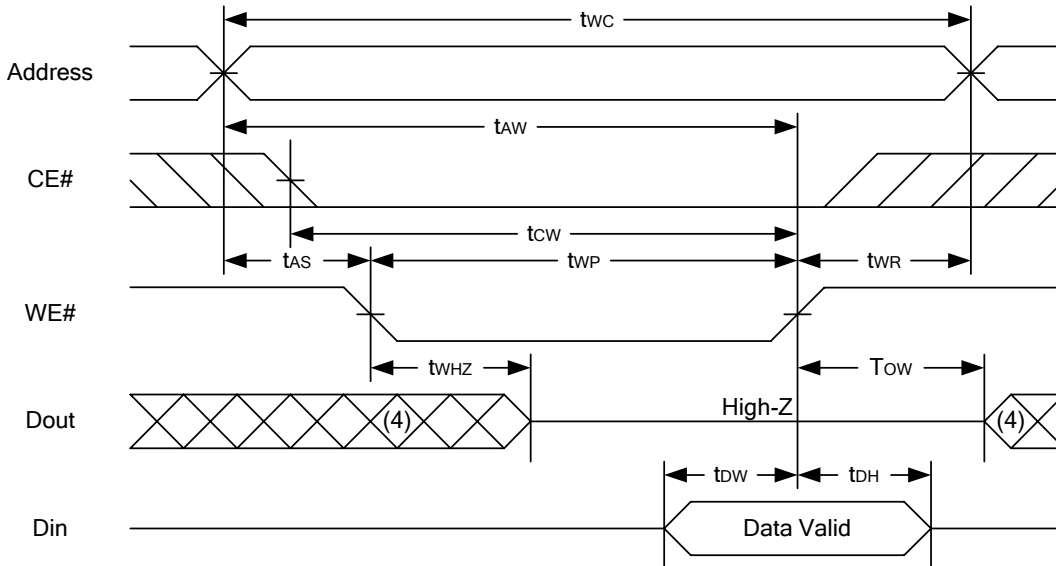
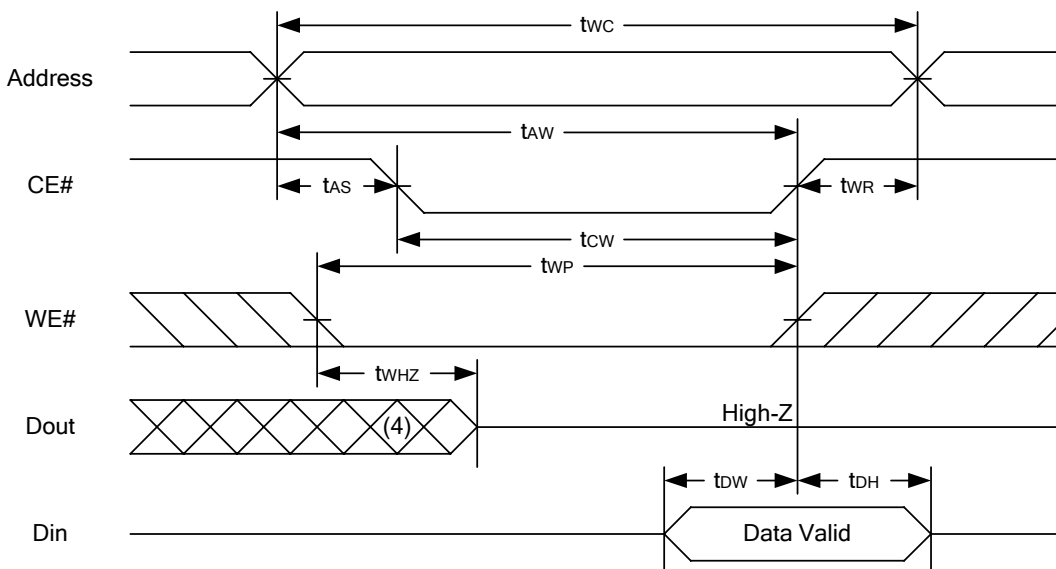


READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.

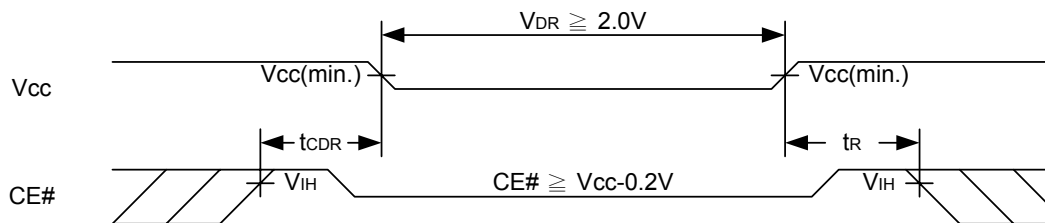
WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)

WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)

Notes :

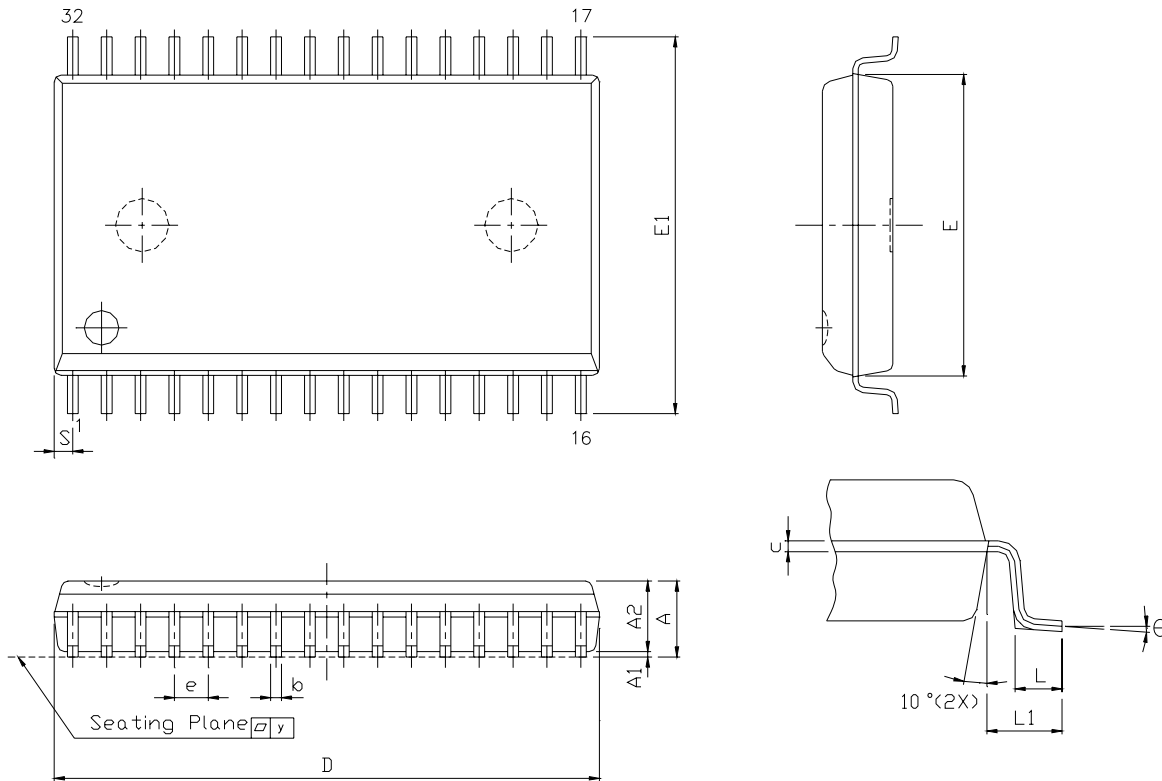
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than t_{WHZ} + t_{DW} to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS

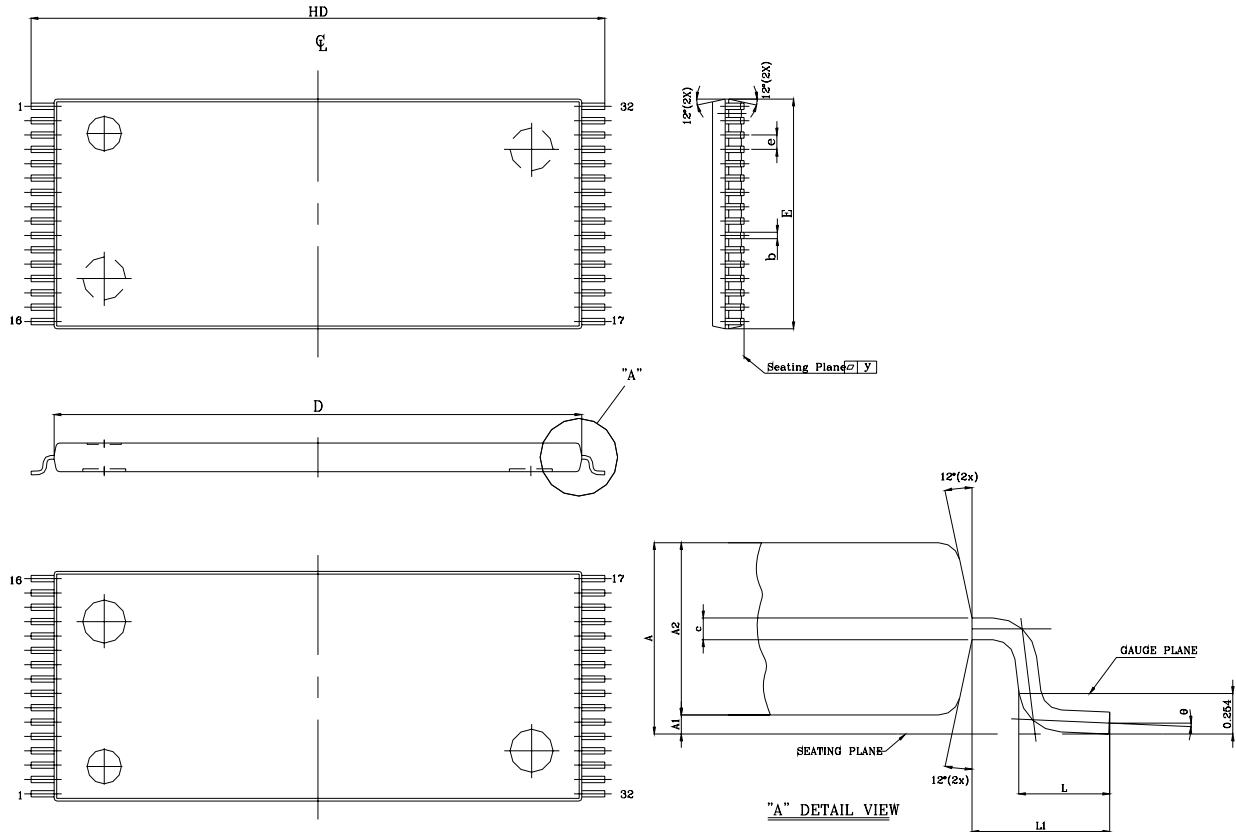
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
V _{CC} for Data Retention	V _{DR}	CE# \geq V _{CC} - 0.2V	2.0	-	5.5	V	
Data Retention Current	I _{DR}	V _{CC} = 2.0V CE# \geq V _{CC} - 0.2V other pins at 0.2V or V _{CC} -0.2V	-SL	-	2	23	μ A
			-LL	-	2	30	μ A
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t _R		t _{RC*}	-	-	ns	

 t_{RC*} = Read Cycle Time

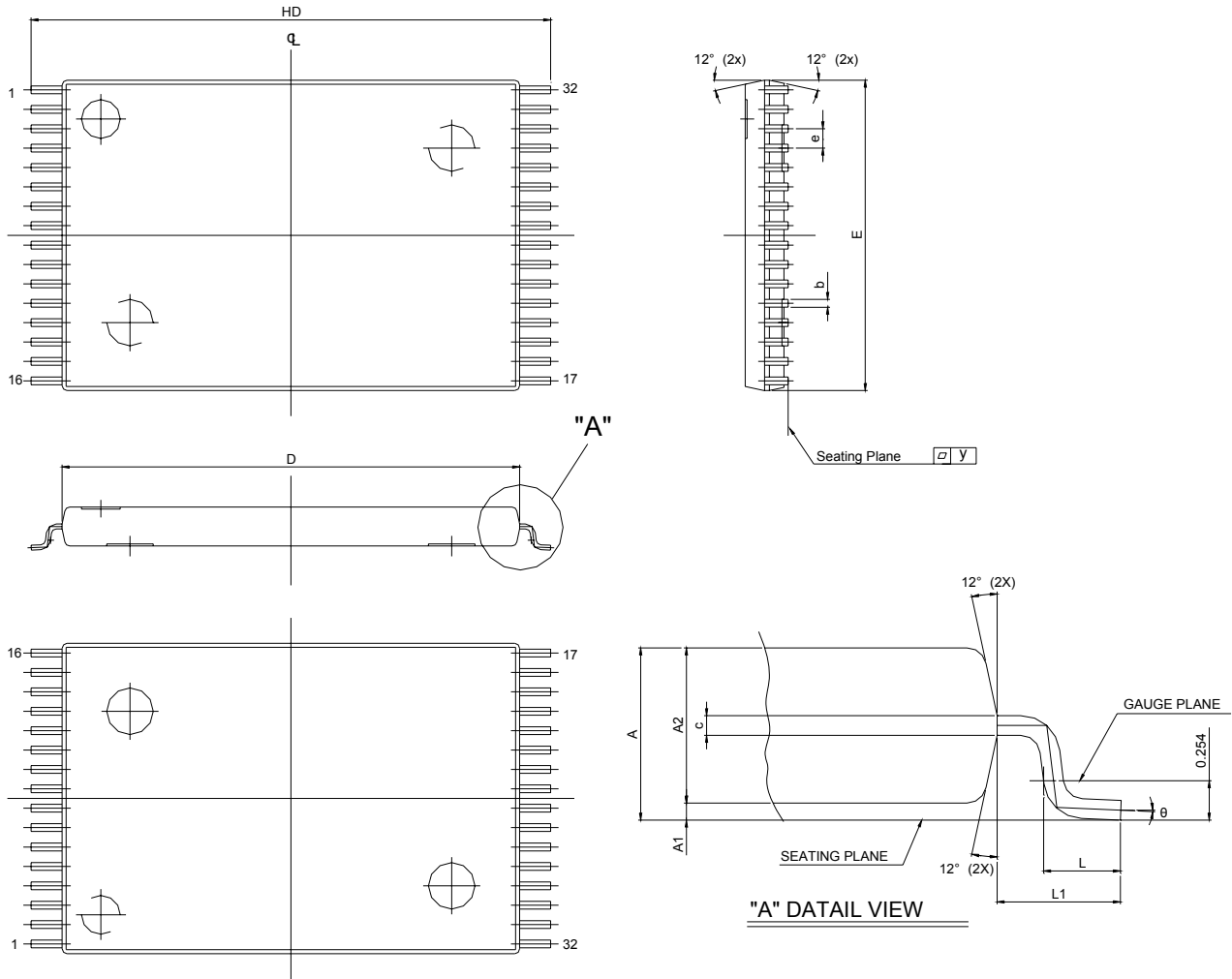
DATA RETENTION WAVEFORM


PACKAGE OUTLINE DIMENSION
32 pin 450 mil SOP Package Outline Dimension


SYM.	UNIT	INCH.(BASE)	MM(REF)
	A		0.118 (MAX)
A1		0.004(MIN)	0.102(MIN)
A2		0.111(MAX)	2.82(MAX)
b		0.016(TYP)	0.406(TYP)
c		0.008(TYP)	0.203(TYP)
D		0.817(MAX)	20.75(MAX)
E		0.445 ±0.005	11.303 ±0.127
E1		0.555 ±0.012	14.097 ±0.305
e		0.050(TYP)	1.270(TYP)
L		0.0347 ±0.008	0.881 ±0.203
L1		0.055 ±0.008	1.397 ±0.203
S		0.026(MAX)	0.660 (MAX)
y		0.004(MAX)	0.101(MAX)
Θ		0° -10°	0° -10°

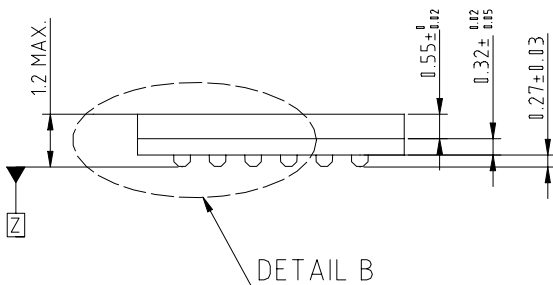
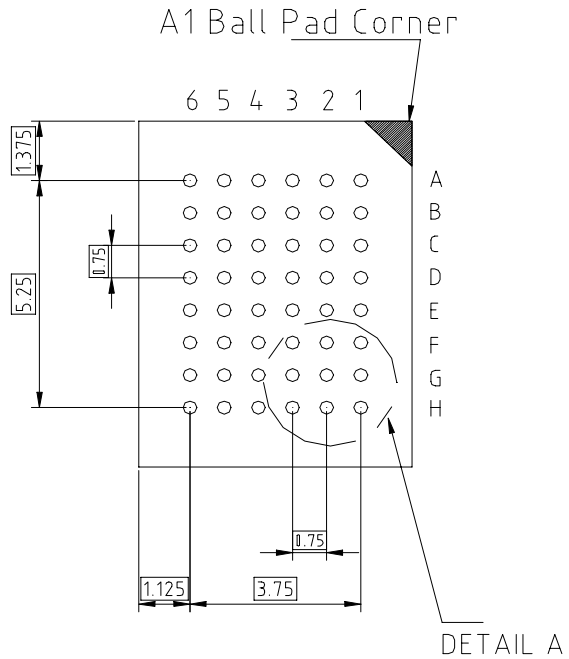
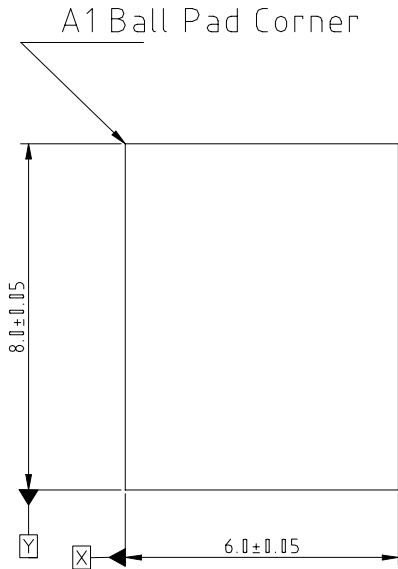
32 pin 8mm x 20mm TSOP-I Package Outline Dimension


SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 \pm 0.002	0.10 \pm 0.05
A2		0.039 \pm 0.002	1.00 \pm 0.05
b		0.008 + 0.002 - 0.001	0.20 + 0.05 - 0.03
c		0.005 (TYP)	0.127 (TYP)
D		0.724 \pm 0.004	18.40 \pm 0.10
E		0.315 \pm 0.004	8.00 \pm 0.10
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 \pm 0.008	20.00 \pm 0.20
L		0.0197 \pm 0.004	0.50 \pm 0.10
L1		0.0315 \pm 0.004	0.08 \pm 0.10
y		0.003 (MAX)	0.076 (MAX)
θ		0° ~ 5°	0° ~ 5°

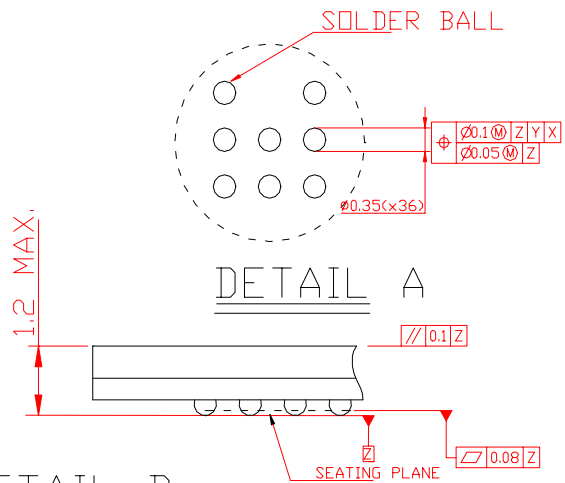
32 pin 8mm x 13.4mm STSOP Package Outline Dimension


SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.049 (MAX)	1.25 (MAX)
A1		0.005 ±0.002	0.130 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.008 ±0.01	0.20±0.025
c		0.005 (TYP)	0.127 (TYP)
D		0.465 ±0.004	11.80 ±0.10
E		0.315 ±0.004	8.00 ±0.10
e		0.020 (TYP)	0.50 (TYP)
HD		0.528±0.008	13.40 ±0.20.
L		0.0197 ±0.004	0.50 ±0.10
L1		0.0315 ±0.004	0.8 ±0.10
y		0.003 (MAX)	0.076 (MAX)
Θ		0°~5°	0°~5°

36 ball 6mm x 8mm TFBGA Package Outline Dimension



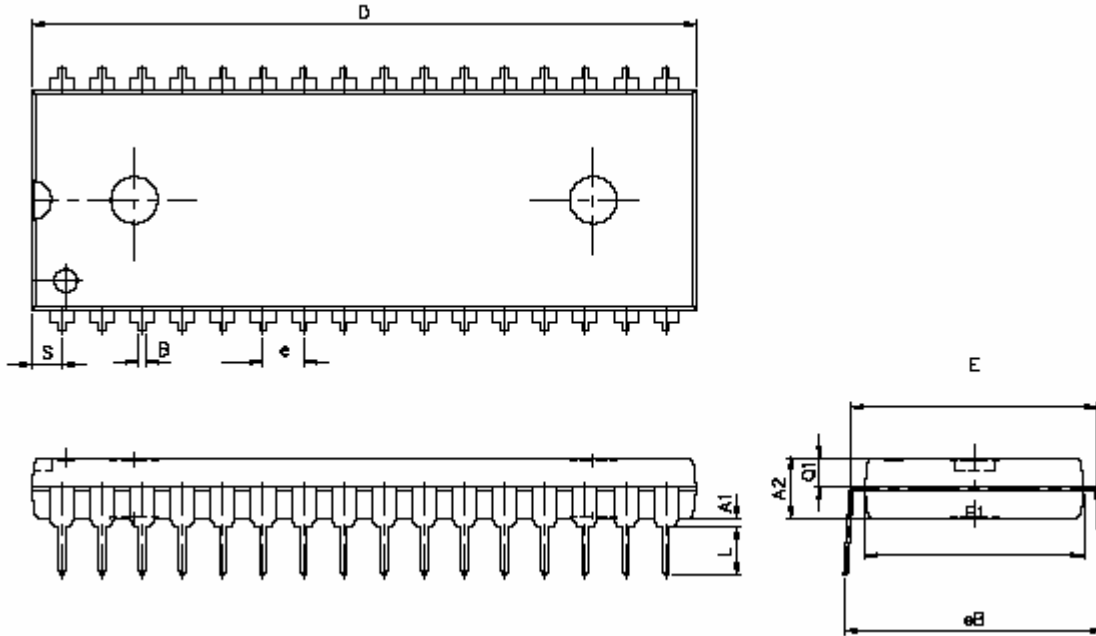
SIDE VIEW



DETAIL B

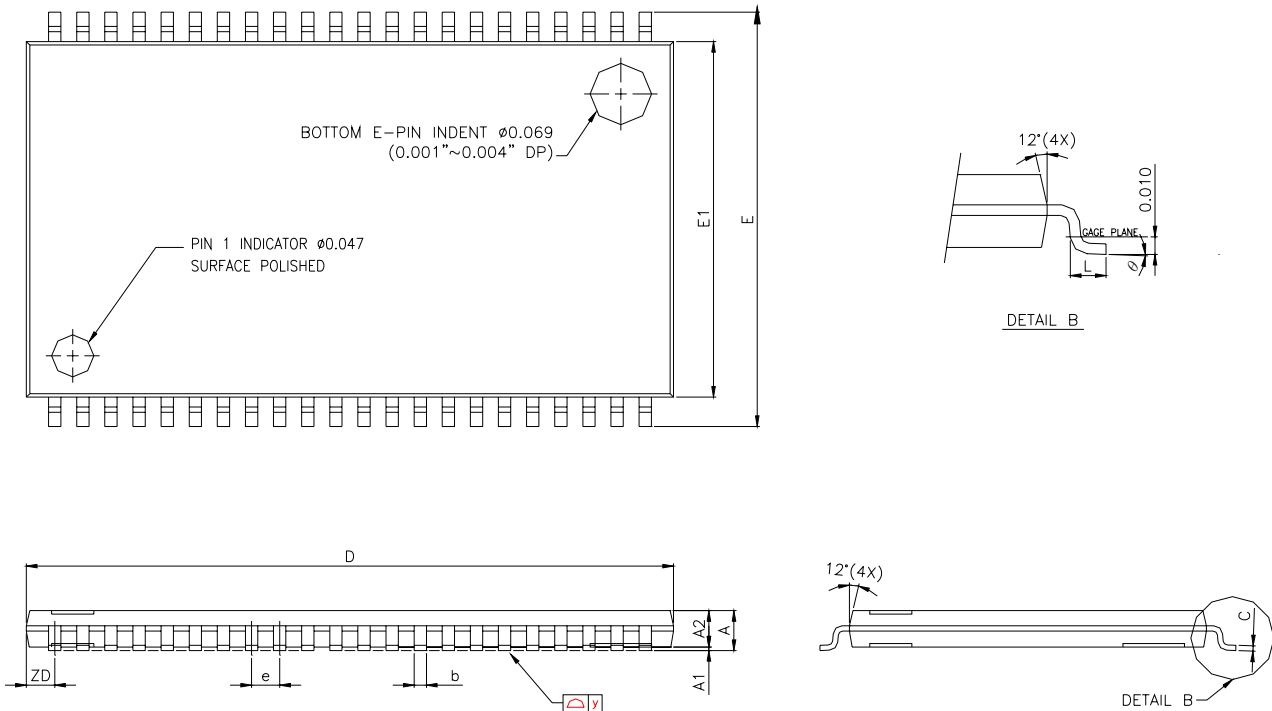


32 pin 600 mil P-DIP Package Outline Dimension



SYM.	UNIT	INCH(BASE)	MM(REF)
A1		0.001 (MIN)	0.254 (MIN)
A2		0.150 ± 0.005	3.810 ± 0.127
B		0.018 ± 0.005	0.457 ± 0.127
D		1.650 ± 0.005	41.910 ± 0.127
E		0.600 ± 0.010	15.240 ± 0.254
E1		0.544 ± 0.004	13.818 ± 0.102
e		0.100 (TYP)	2.540 (TYP)
eB		0.640 ± 0.020	16.256 ± 0.508.
L		0.130 ± 0.010	3.302 ± 0.254
S		0.075 ± 0.010	1.905 ± 0.254
Q1		0.070 ± 0.005	1.778 ± 0.127

Note : D/E1/S dimension do not include mold flash.

44-pin 400mil TSOP-II Package Outline Dimension


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°



ORDERING INFORMATION

LY625128 V W - XX YY Z

Z : Temperature Range
Blank : (Commercial) 0°C ~ 70°C
E : (Extended) -20°C ~ +80°C
I : (Industrial) -40°C ~ +85°C

YY : Power Type
LL : Ultra Low Power
SL : Special Ultra Low Power

XX : Access Time(Speed)

W : Lead Information
N : Normal
L : Lead Free

V : Package Type
S : 32-pin 450 mil SOP
L : 32-pin 8 mm x 20 mm TSOP-I
R : 32-pin 8 mm x 13.4 mm STSOP
G : 36-ball 6 mm x 8 mm TFBGA
P : 32-pin 600 mil P-DIP
M : 44-pin 400 mil TSOP-II



®

Lyontek Inc.

LY625128

Rev. 2.0

512K X 8 BIT LOW POWER CMOS SRAM

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