TSV7721, TSV7722, TSV7723

Datasheet

High bandwidth (22 MHz) low offset (200 µV) 5 V op amp

TSV7721
SOT23 -5

TSV7722
DFN8 2x2 mm

TSV7722
MiniSO8

TSV7723
MiniSO10

TSV7722
SO8

Features

- Gain bandwidth product 22 MHz, unity gain stable
- High accuracy input offset voltage: 50 µV typ., 200 µV max.
- Low input bias current: 2 pA typ.
- Low input voltage noise density: 7 nV/√Hz
- Wide supply voltage range: 1.8 V to 5.5 V
- Output rail-to-rail
- Input common-mode range includes low rail
- Automotive grade and shutdown versions available
- Benefits:
  - High frequency signal conditioning
  - Optimized accuracy for low-side current sensing

Applications

- Low-side current measurement
- Photodiode amplifiers
- Automotive current measurement and sensor signal conditioning
- Strain gauges signal conditioning

Description

The TSV7721, TSV7722 and TSV7723 are single and dual 22 MHz-bandwidth unity-gain-stable amplifiers. The input offset voltage of 200 µV max. (50 µV typ.) at room temperature, optimized for common-mode close to ground makes the TSV772x ideal for low-side current measurements.

The TSV772x can operate from 1.8 V to 5.5 V single supply and it is fully specified on a load of 47 pF, therefore allowing easy usage as A/D converters input buffer.

The TSV772x series offers rail-to-rail output, excellent speed/power consumption ratio, and 22 MHz gain bandwidth product, while consuming just 1.7 mA at 5 V.

The devices also feature an ultra-low input bias current that enables connection to photodiodes and other sensors where current is the key value to be measured.

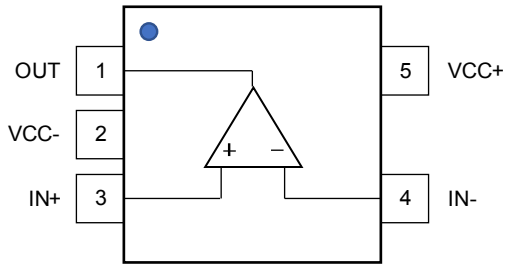
These features make the TSV772x series ideal for high-accuracy, high-bandwidth sensor interfaces.

Maturity status link	Channel	Automotive	Package
TSV7721	1		SOT23-5
	1	•	SOT23-5
TSV7722	2		DFN8
	2		MiniSO8
	2		SO8
	2	•	MiniSO8
	2	•	SO8
TSV7723	2		MiniSO10

Related products	
TSV792	Rail-to-rail amplifier with higher GBW 50 MHz
TSV7192	20 MHz amplifier with 36 V supply voltage

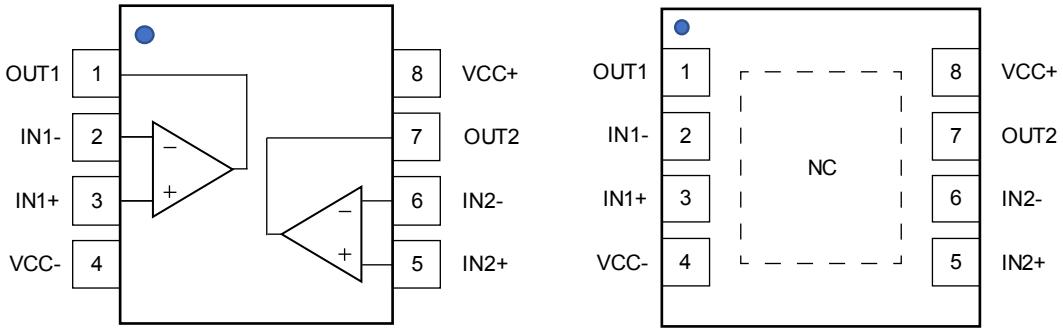
1 Pin connections

Figure 1. TSV7721 single operational amplifier



SOT23-5

Figure 2. TSV7722 dual operational amplifier

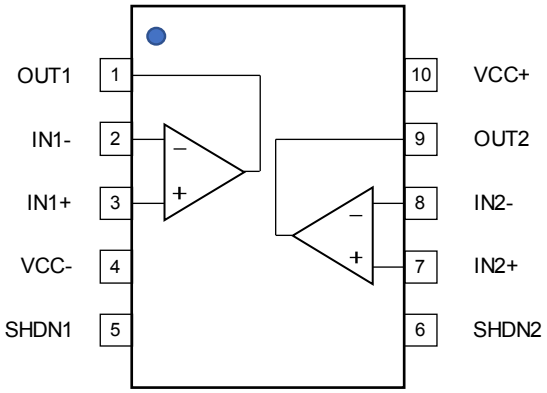


MiniSO8 and SO8

DFN8 2 x 2 mm(1)

1. The exposed pad of the DFN8 2x2 can be connected to VCC- or left floating.

Figure 3. TSV7723 dual operational amplifier with shutdown option



MiniSO10

2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (referred to VCC- pin) (1)	-0.3 to 6.0	V
V_{id}	Differential input voltage (2)	± VCC	V
V_{IN}	Input pins input voltage (3)	V_{CC-} - 0.3 V to V_{CC+} + 0.3 V	V
I_{IN}	Input pins input current (4)	± 10	mA
T_{stg}	Storage temperature	-65 to 150	°C
R_{th-ja}	Thermal resistance junction-to-ambient (5)		°C / W
	SOT23-5	250	
	DFN8 (2 mm x 2 mm)	76	
	MiniSO8	127	
	MiniSO10	113	
	SO8	113	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model (6)	4	kV
	CDM: charged device model (7)	1.5	kV

1. *All voltage values, except differential voltage, are with respect to VCC- pin.*
2. *The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.*
3. *Vcc - Vin must not exceed 6 V, Vin must not exceed 6 V.*
4. *Input current must be limited by a resistor in series with the inputs.*
5. *Rth are typical values.*
6. *Human body model: the test HBM is done in accordance with the standards ESDA-JS-001-2017 and Q100-002*
7. *Charged device model: the test CDM is done in accordance with the standards ESDA-JS-002-2018 and Q100-011*

Table 2. Operating conditions

Symbol	Parameter	Min.	Max.	Value
V_{CC}	Supply voltage	1.8	5.5	V
V_{icm}	Common-mode input voltage range	V_{CC-} – 0.1	V_{CC+} – 1.1	V
T_{oper}	Operating free air temperature range	-40	125	°C

3 Electrical characteristics

Table 3. Electrical characteristics at V_{CC+} = 5 V, with V_{CC-} = 0 V, V_{icm} = V_{CC} / 2, T = 25°C, and OUT pin connected to V_{CC} / 2 through R_L = 10 kΩ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC Performance						
V_{io}	Input offset voltage (V_{icm} = 0 V)	T = 25°C		±50	±250	µV
		-40°C < T < 125°C			±650	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (V_{icm} = 0 V)	-40°C < T < 125°C			±4	µV/°C
I_{ib}	Input bias current (V_{OUT} = V_{CC}/2)	T = 25°C		2		pA
		-40°C < T < 125°C		75		
I_{io}	Input offset current (V_{OUT} = V_{CC}/2)	T = 25°C		1		pA
		-40°C < T < 125°C		20		
CMR1	Common-mode rejection ratio 20.log($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 V to V_{CC-} 1.1 V, R_L > 1 MΩ	T = 25°C	76	99		dB
		-40°C < T < 125°C	74			
CMR2	Common-mode rejection ratio 20.log($\Delta V_{icm}/\Delta$Vio), V_{icm} = -0.1 V to V_{CC}- 1.1 V, R_L > 1 MΩ	T = 25°C	75			dB
		-40°C < T < 125°C	60			
SVR	Supply voltage rejection ratio 20.log($\Delta V_{CC}/\Delta V_{io}$), V_{CC} = 1.8 V to 5.5 V, V_{icm} = 0 V, R_L > 1 MΩ	T = 25°C	85	108		dB
		-40°C < T < 125°C	80			
A_{VD}	Large signal voltage gain V_{OUT} = 0.3 V to (V_{CC}- 0.3 V)	T = 25°C	111	130		dB
		-40°C < T < 125°C	106			
V_{OH}	High level output voltage (V_{OH} = V_{CC} - V_{OUT})	T = 25°C			15	mV
		-40°C < T < 125°C			25	
V_{OL}	Low level output voltage	T = 25°C			15	
		-40°C < T < 125°C			25	
I_{OUT}	I_{sink} (V_{OUT} = V_{CC})	T = 25°C	50	70		mA
		-40°C < T < 125°C	45			
	I_{source} (V_{OUT} = 0 V)	T = 25°C	45	65		
		-40°C < T < 125°C	40			
I_{CC}	Supply current (per channel, V_{OUT} = V_{CC}/2, R_L > 1 MΩ)	T = 25°C		1.7	2.2	mA
		-40°C < T < 125°C			2.5	
AC Performance						
GBW	Gain bandwidth product	C_L = 47 pF	15	22		MHz
F_u	Unity gain frequency			19.5		
Φ_m	Phase margin			44		degrees
G_m	Gain margin			8		dB
SR	Slew rate (1)		8	11		V/µs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{rec}	Overload recovery time: trec is defined as delay between input voltage edge and V_{OUT} reaching 100 mV from initial value			70		ns
t_s	Settling time	To 0.1%, V_{in} = 1 V_{p-p}		270		ns
e_n	Equivalent input noise voltage	f = 1 kHz		13		nV/√Hz
		f = 10 kHz		7		
C_S	Channel separation (for TSV7722 and TSV7723)	f = 1 kHz		120		dB
C_{in}	Input capacitance	Differential		6		pF
		Common-mode		4.5		
SHDN characteristics (TSV7723 only, SHDN active low)						
I_{CC}	Supply current per channel in shutdown mode V_{OUT} = V_{CC} / 2, R_L > 1 MΩ, S_{HDN} = V_{CC-}	T = 25°C		2.5	50	nA
		-40°C < T < 85°C			450	
		-40°C < T < 125°C			4	µA
t_{on}	Amplifier turn-on time (other channel already on)	V_{OUT} = V_{CC-} to V_{CC-} + 0.2 V		2		µs
t_{init}	Initialization time (both channels off)	V_{OUT} to 200 mV of final value		7		µs
V_{IH}	SHDN logic high		2			V
V_{IL}	SHDN logic low				0.8	
I_{IH}	SHDN current high	SHDN = V_{CC+}		TBD		pA
I_{IL}	SHDN current low	SHDN = V_{CC-}		TBD		
I_{Oleak}	Output leakage in shutdown mode, SHDN = V_{CC-}	T = 25°C		TBD		pA
		-40°C < T < 125°C		TBD		nA

1. *Slew rate value is calculated as the average between positive and negative slew rates.*

Table 4. Electrical characteristics at V_{CC+} = 3.3 V, with V_{CC-} = 0 V, V_{icm} = V_{CC} / 2, T = 25°C, and OUT pin connected to V_{CC} / 2 through R_L = 10 kΩ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC Performance						
V_{io}	Input offset voltage (V_{icm} = 0 V)	T = 25°C		±50	±200	µV
		-40°C < T < 125°C			±600	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (V_{icm} = 0 V)	-40°C < T < 125°C			±4	µV/°C
I_{ib}	Input bias current (V_{OUT} = V_{CC}/2)	T = 25°C		1.8		pA
		-40°C < T < 125°C		60		
I_{io}	Input offset current (V_{OUT} = V_{CC}/2)	T = 25°C		1		pA
		-40°C < T < 125°C		20		
CMR1	Common-mode rejection ratio 20.log($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 V to V_{CC-} 1.1 V, R_L > 1 MΩ	T = 25°C	75	96		dB
		-40°C < T < 125°C	71			
CMR2	Common-mode rejection ratio 20.log($\Delta V_{icm}/\Delta Vio$), V_{icm} = - 0.1 V to V_{CC-} 1.1 V, R_L > 1 MΩ	T = 25°C	73			dB
		-40°C < T < 125°C	57			
A_{VD}	Large signal voltage gain V_{OUT} = 0.3 V to (V_{CC-} 0.3 V)	T = 25°C	107	128		dB
		-40°C < T < 125°C	103			
V_{OH}	High level output voltage (V_{OH} = V_{CC} - V_{OUT})	T = 25°C			15	mV
		-40°C < T < 125°C			25	
V_{OL}	Low level output voltage	T = 25°C			15	
		-40°C < T < 125°C			25	
I_{OUT}	I_{sink} (V_{OUT} = V_{CC})	T = 25°C	50	70		mA
		-40°C < T < 125°C	45			
	I_{source} (V_{OUT} = 0 V)	T = 25°C	45	65		
		-40°C < T < 125°C	40			
I_{CC}	Supply current (per channel, V_{OUT} = V_{CC}/2, R_L > 1 MΩ)	T = 25°C		1.7	2.2	mA
		-40°C < T < 125°C			2.5	
AC Performance						
GBW	Gain bandwidth product	C_L = 47 pF	14	21		MHz
F_u	Unity gain frequency			18.5		
Φ_m	Phase margin			42		degrees
G_m	Gain margin			8		dB
SR	Slew rate (1)		7.7	11		V/µs
t_s	Settling time	To 0.1%, V_{in} = 1 V_{p-p}		210		ns
e_n	Equivalent input noise voltage	f = 1 kHz		13		nV/√Hz
		f = 10 kHz		7		
C_S	Channel separation (for TSV7722 and TSV7723)	f = 1 kHz		120		dB
SHDN characteristics (TSV7723 only, SHDN active low)						
I_{CC}	Supply current per channel in shutdown mode	T = 25°C		2.5	50	nA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	V_{OUT} = V_{CC} / 2, R_L > 1 MΩ, S_{HDN} = V_{CC-}	-40°C < T < 85°C			450	nA
		-40°C < T < 125°C			4	µA
t_{on}	Amplifier turn-on time (other channel already on)	V_{OUT} = V_{CC-} to V_{CC-} + 0.2 V		2		µs
t_{init}	Initialization time (both channels off)	V_{OUT} to 200 mV of final value		11		µs
V_{IH}	SHDN logic high		2			V
V_{IL}	SHDN logic low				0.8	
I_{IH}	SHDN current high	SHDN = V_{CC+}		TBD		pA
I_{IL}	SHDN current low	SHDN = V_{CC-}		TBD		
I_{Oleak}	Output leakage in shutdown mode, SHDN = V_{CC-}	T = 25°C		TBD		pA
		-40°C < T < 125°C		TBD		nA

1. *Slew rate value is calculated as the average between positive and negative slew rates.*

Table 5. Electrical characteristics at V_{CC+} = 1.8 V, with V_{CC-} = 0 V, V_{icm} = 0.7 V, T = 25°C, and OUT pin connected to V_{CC} / 2 through R_L = 10 kΩ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC Performance						
V_{io}	Input offset voltage (V_{icm} = 0 V)	T = 25°C		±50	±250	µV
		-40°C < T < 125°C			±650	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (V_{icm} = 0 V)	-40°C < T < 125°C			±4	µV/°C
I_{ib}	Input bias current (V_{OUT} = V_{CC}/2)	T = 25°C		1		pA
		-40°C < T < 125°C		40		
I_{io}	Input offset current (V_{OUT} = V_{CC}/2)	T = 25°C		1		pA
		-40°C < T < 125°C		15		
CMR1	Common-mode rejection ratio 20.log($\Delta V_{icm}/\Delta V_{io}$), V_{icm} = 0 V to V_{CC-} 1.1 V, R_L > 1 MΩ	T = 25°C	72	93		dB
		-40°C < T < 125°C	68			
CMR2	Common-mode rejection ratio 20.log($\Delta V_{icm}/\Delta$Vio), V_{icm} = - 0.1 V to V_{CC-} 1.1 V, R_L > 1 MΩ	T = 25°C	70			dB
		-40°C < T < 125°C	52			
A_{VD}	Large signal voltage gain V_{OUT} = 0.3 V to (V_{CC-} 0.3 V)	T = 25°C	101	122		dB
		-40°C < T < 125°C	97			
V_{OH}	High level output voltage (V_{OH} = V_{CC} - V_{OUT})	T = 25°C			15	mV
		-40°C < T < 125°C			25	
V_{OL}	Low level output voltage	T = 25°C			15	
		-40°C < T < 125°C			25	
I_{OUT}	I_{sink} (V_{OUT} = V_{CC})	T = 25°C	35	42		mA
		-40°C < T < 125°C	20			
	I_{source} (V_{OUT} = 0 V)	T = 25°C	20	32		
		-40°C < T < 125°C	10			
I_{CC}	Supply current (per channel, V_{OUT} = V_{CC} / 2, R_L > 1 MΩ)	T = 25°C		1.7	2.2	mA
		-40°C < T < 125°C			2.5	
AC Performance						
GBW	Gain bandwidth product	C_L = 47 pF	14	21		MHz
F_u	Unity gain frequency			18		
Φ_m	Phase margin			41		degrees
G_m	Gain margin			8		dB
SR	Slew rate (1)		7.6	11		V/µs
e_n	Equivalent input noise voltage	f = 1 kHz		13		nV/√Hz
		f = 10 kHz		7		
C_S	Channel separation (for TSV7722 and TSV7723)	f = 1 kHz		120		dB
SHDN characteristics (TSV7723 only, SHDN active low)						
I_{CC}	Supply current per channel in shutdown mode V_{OUT} = V_{CC} / 2, R_L > 1 MΩ,	T = 25°C		2.5	50	nA
		-40°C < T < 85°C			450	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	S_{HDN} = V_{CC-}	-40°C < T < 125°C			4	µA
t_{on}	Amplifier turn-on time (other channel already on)	V_{OUT} = V_{CC} - to V_{CC} - + 0.2 V		1.5		µs
t_{init}	Initialization time (both channels off)	V_{OUT} to 200 mV of final value		38		µs
V_{IH}	SHDN logic high		1.2			V
V_{IL}	SHDN logic low				0.6	
I_{IH}	SHDN current high	SHDN = V_{CC+}		TBD		pA
I_{IL}	SHDN current low	SHDN = V_{CC-}		TBD		
I_{Oleak}	Output leakage in shutdown mode, SHDN = V_{CC-}	T = 25°C		TBD		pA
		-40°C < T < 125°C		TBD		nA

1. *Slew rate value is calculated as the average between positive and negative slew rates.*

4 Typical performance characteristics

R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 47 pF, unless otherwise specified.

Figure 4. Supply current vs. supply voltage

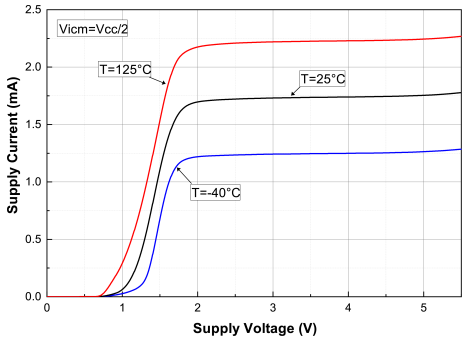


Figure 5. Input offset voltage distribution at V_{CC} = 5 V

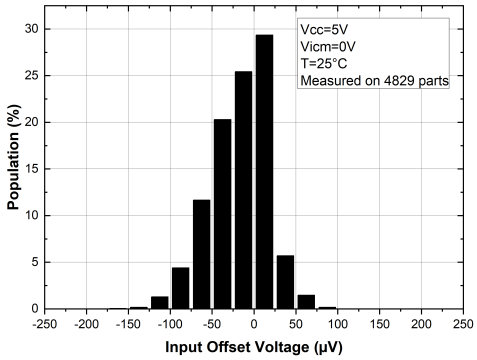


Figure 6. Input offset voltage distribution at V_{CC} = 1.8 V

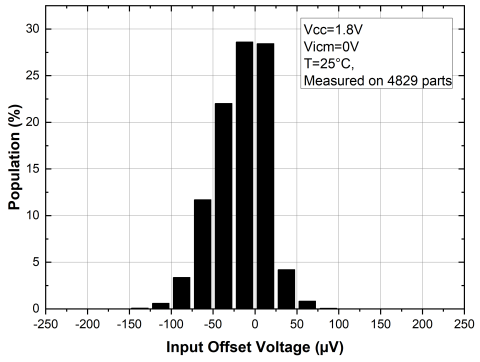


Figure 7. Input offset voltage vs. temperature at V_{CC} = 5 V

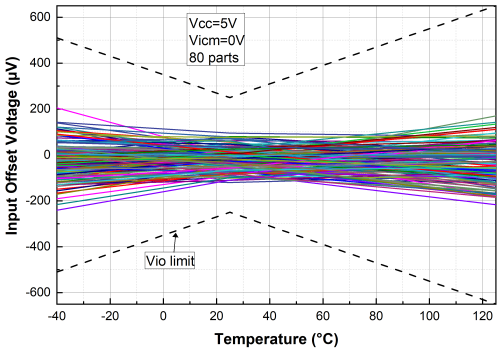


Figure 8. Input offset voltage vs. temperature at V_{CC} = 1.8 V

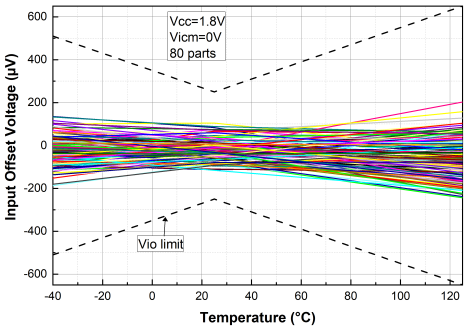


Figure 9. Input offset voltage thermal coefficient at V_{CC} = 5 V

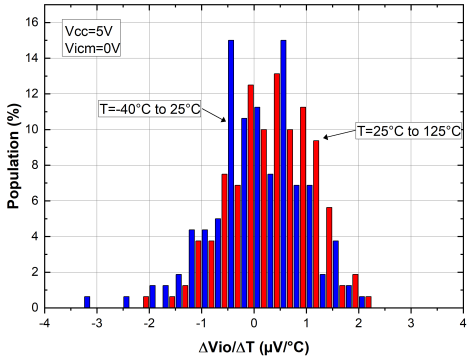


Figure 10. Input offset voltage thermal coefficient at V_{CC} = 1.8 V

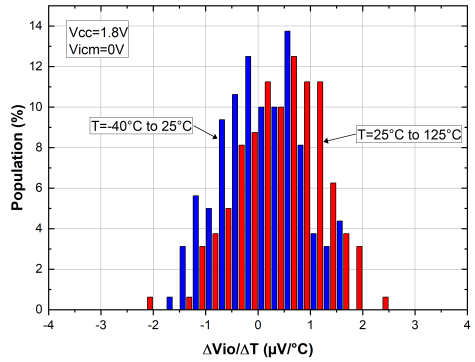


Figure 11. Input offset voltage vs. supply voltage

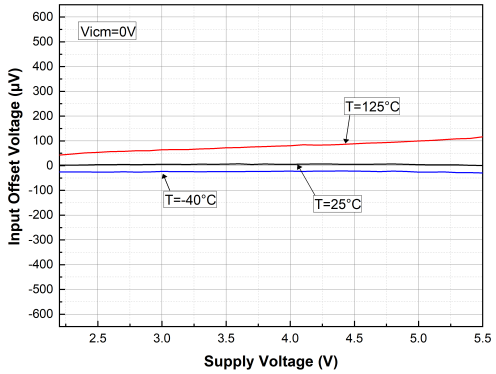


Figure 12. Input offset voltage vs. common-mode voltage at V_{CC} = 5 V

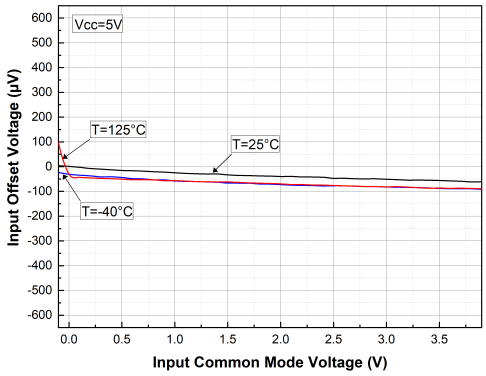


Figure 13. Input offset voltage vs. common-mode voltage at V_{CC} = 1.8 V

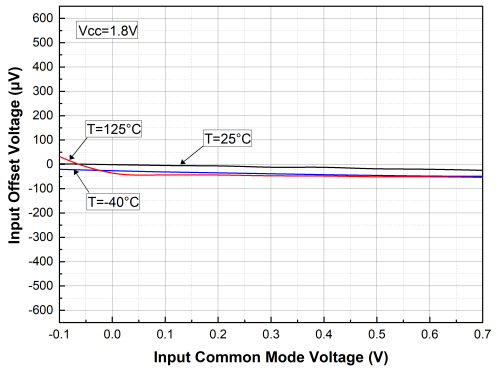


Figure 14. Input bias current vs. temperature at V_{ICM} = V_{CC} / 2

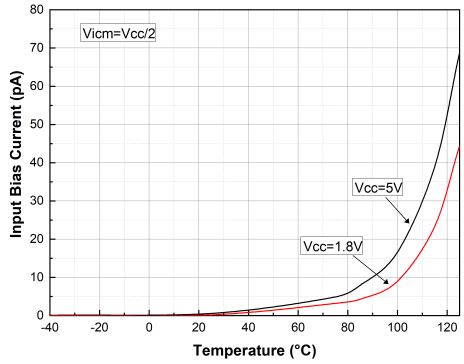


Figure 15. Input bias current vs. common-mode voltage at V_{CC} = 5 V

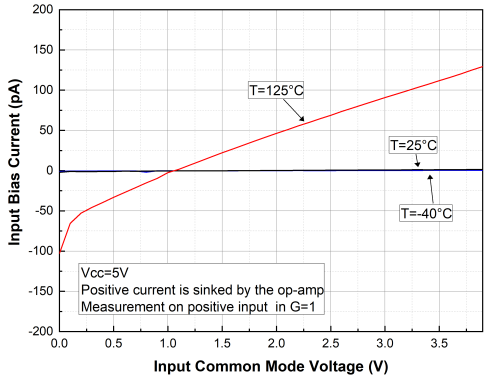


Figure 16. Output current vs. output voltage at V_{CC} = 5 V

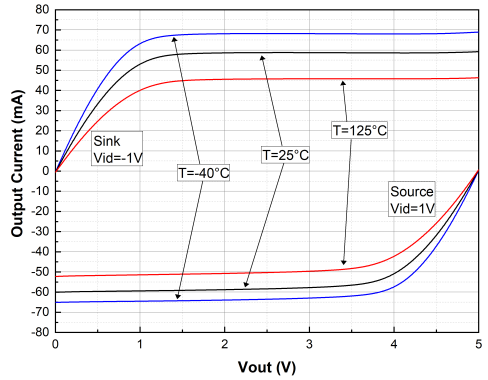


Figure 17. Output current versus output voltage at V_{CC} = 1.8 V

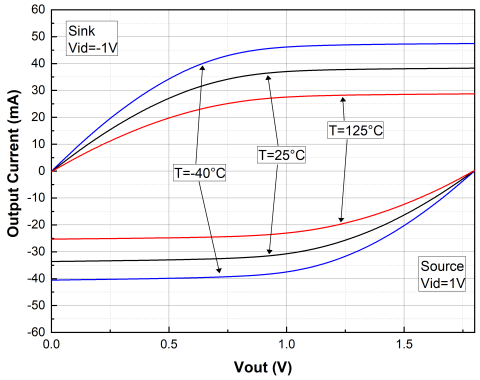


Figure 18. Output saturation voltage (V_{OL}) vs. supply voltage

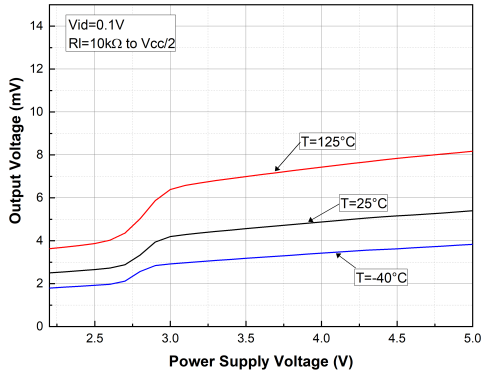


Figure 19. Output saturation voltage (V_{OH}) vs. supply voltage

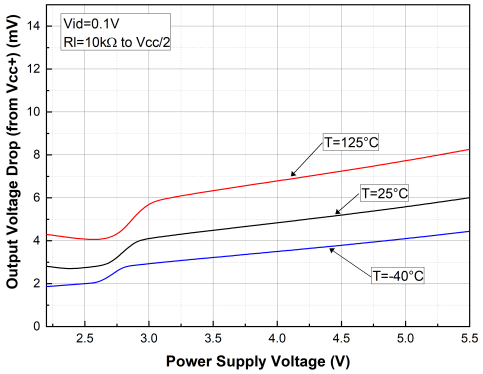


Figure 20. Positive slew rate at V_{CC} = 5 V

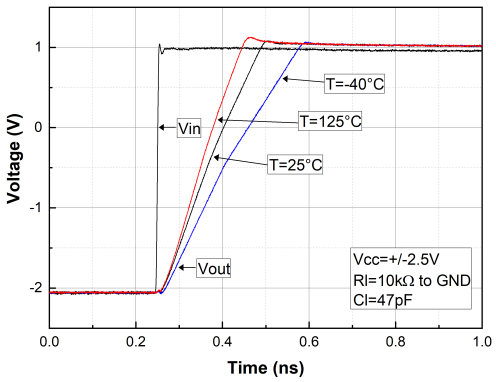


Figure 21. Negative slew rate at VCC = 5 V

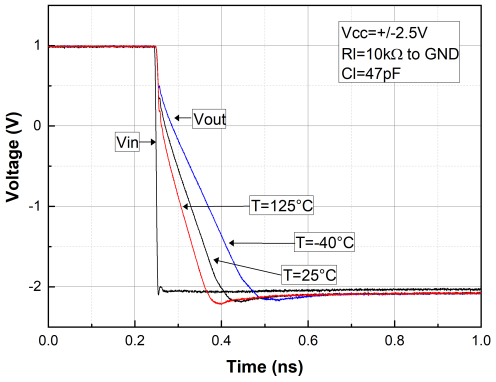


Figure 22. Slew rate vs. V_{CC}

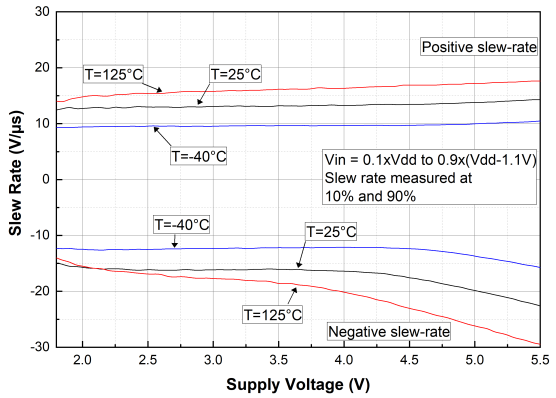


Figure 23. Open loop bode diagram at V_{CC} = 5 V

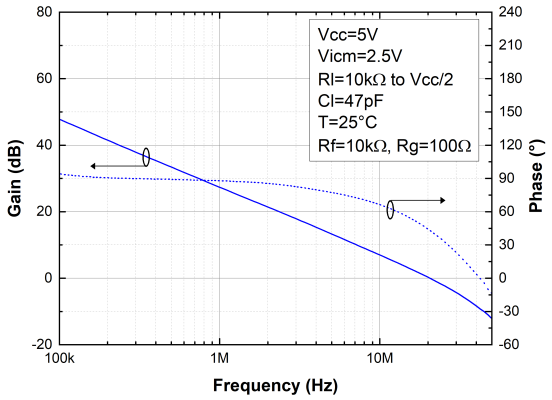


Figure 24. Open loop bode diagram at V_{CC} = 1.8 V

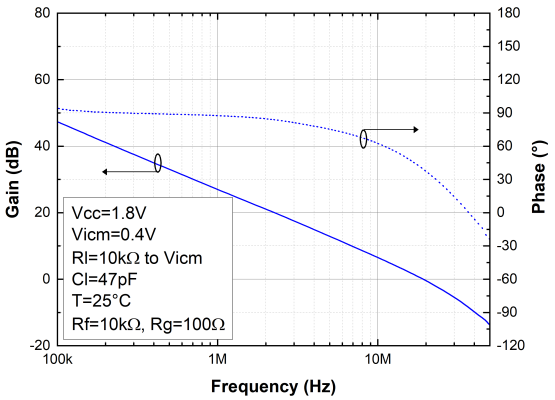


Figure 25. Closed loop bode diagram at V_{CC} = 5 V

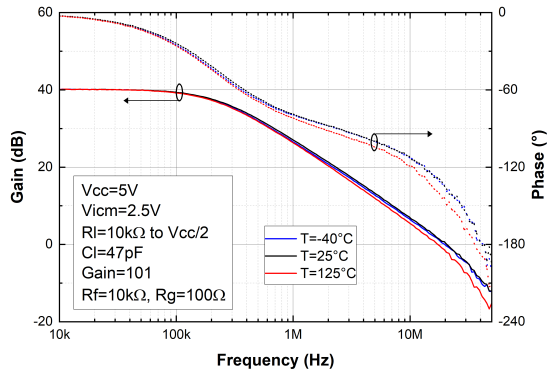


Figure 26. Closed loop bode diagram at V_{CC} = 1.8 V

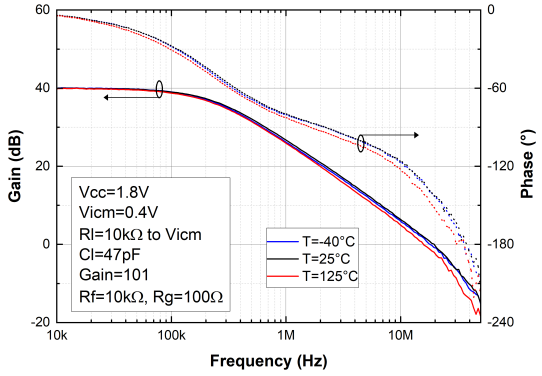


Figure 27. Phase margin vs. common-mode voltage and load current at V_{CC} = 5 V

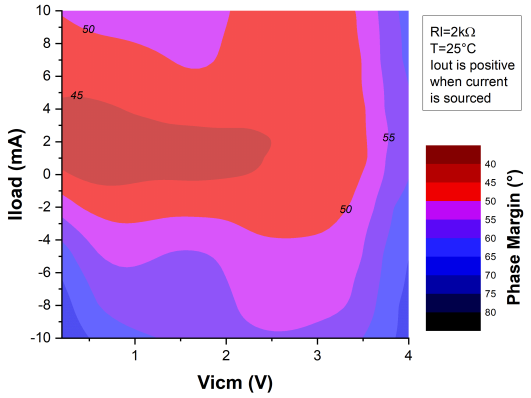


Figure 28. Phase margin vs. capacitive load

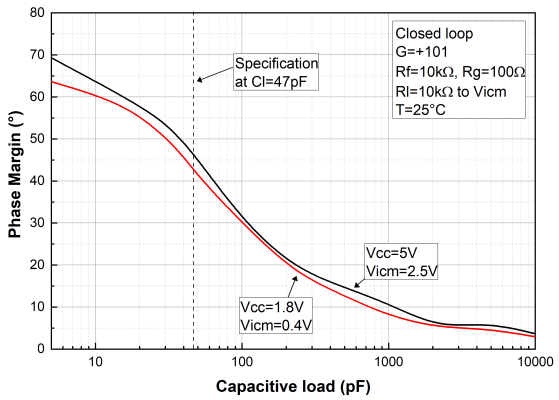


Figure 29. Small step response at V_{CC} = 5 V

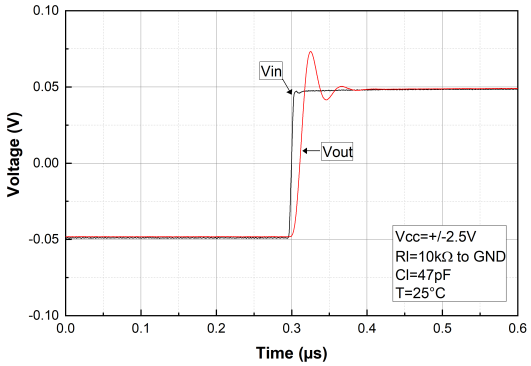


Figure 30. Small step response at V_{CC} = 1.8 V

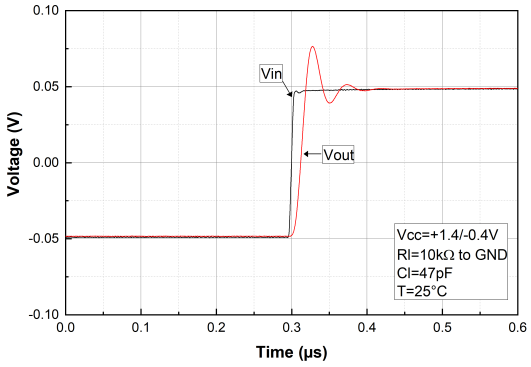


Figure 31. Desaturation from low rail at V_{CC} = 5 V

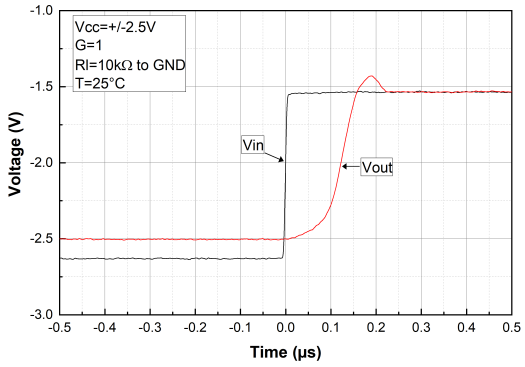


Figure 32. Desaturation from high rail at V_{CC} = 5 V

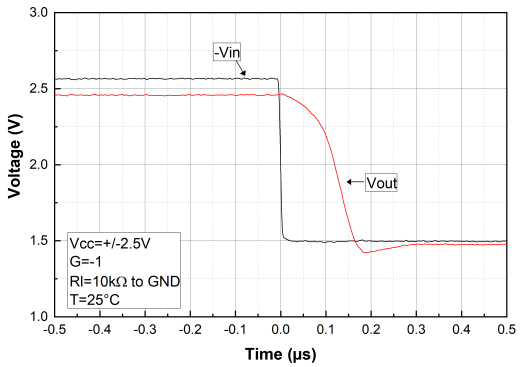


Figure 33. Settling time output high to low at V_{CC} = 5 V

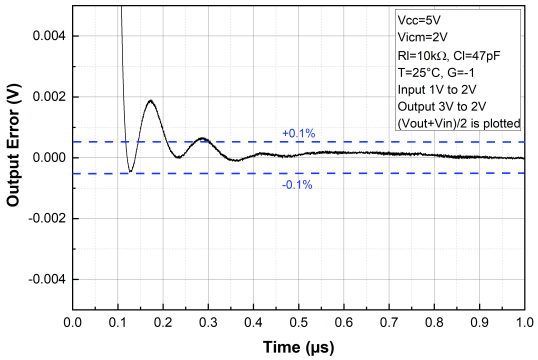


Figure 34. Settling time output low to high at V_{CC} = 5 V

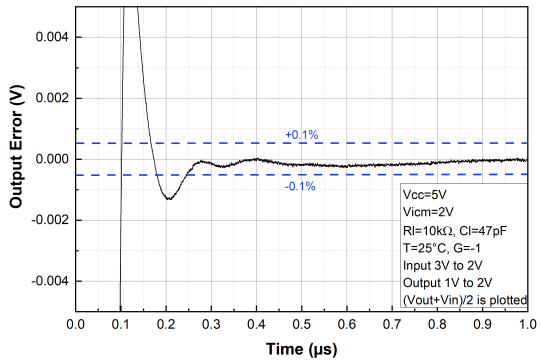


Figure 35. Small step overshoot vs. load capacitance

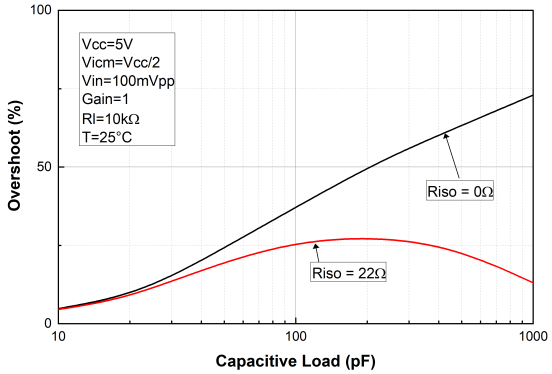


Figure 36. Linearity vs. load resistance at V_{CC} = 5 V

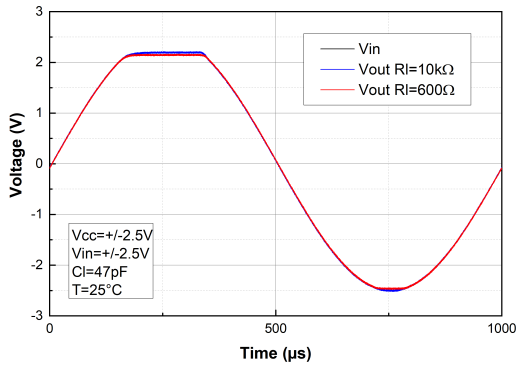


Figure 37. Noise vs. frequency

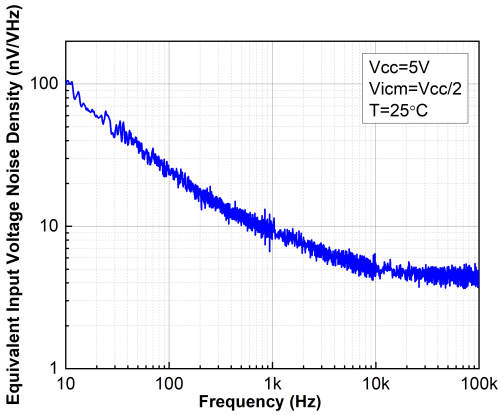


Figure 38. Noise versus time at V_{CC} = 5 V

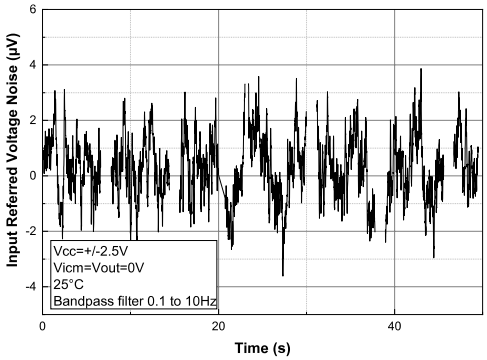


Figure 39. THD+N vs. frequency

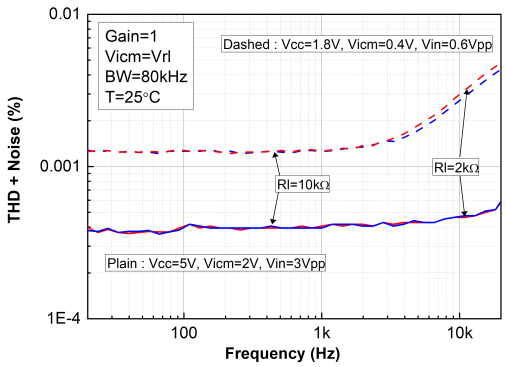


Figure 40. THD+N vs. output voltage

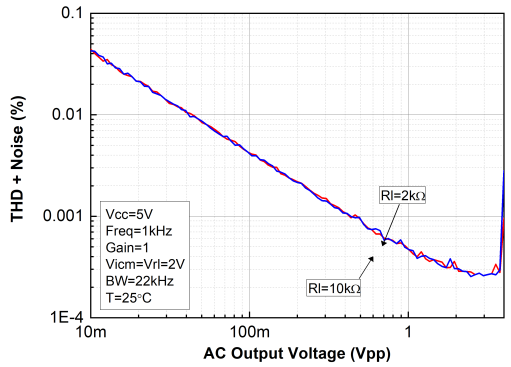


Figure 41. CMRR vs. frequency at V_{CC} = 5 V

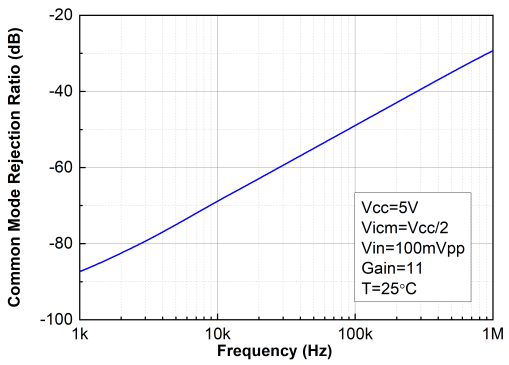
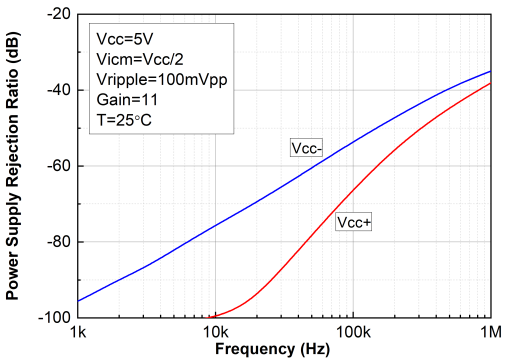


Figure 42. PSRR vs. frequency at V_{CC} = 5 V



5 Application information

5.1 Operating voltages

The TSV7722 device can operate from 1.8 to 5.5 V. The parameters are fully specified at 1.8 V, 3.3 V and 5 V power supplies. However, the parameters are very stable over the full V_{CC} range and several characterization curves show the TSV7722 device characteristics over the full operating range. Additionally, the main specifications are guaranteed in extended temperature range from - 40 to 125°C.

The TSV7722 device is low rail input, and rail-to-rail output. The common-mode operating range is from V_{cc-} - 0.1 V, to V_{cc+} - 1.1 V. The op amp V_{io} is trimmed at V_{cc} = 3.3 V, V_{icm} = 0 V, and thus the DC precision is optimized for operation with V_{icm} close to Vcc-.

5.2 Input offset voltage drift over the temperature

The maximum input voltage drift variation overtemperature is defined as the offset variation related to the offset value measured at 25°C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25°C can be compensated during production at application level. The maximum input voltage drift overtemperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift overtemperature is computed using the following equation:

$$\frac{\Delta V_{io}}{\Delta T} = max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right| \quad (1)$$

Where T = - 40°C and 125°C.

The TSV7721, TSV7722, TSV7723 datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.3 Unused channel

When one of the two channels of the TSV7722 is not used, it must be properly connected in order to avoid internal oscillations that can negatively impact the signal integrity on the other channel, as well as the current consumption. Two different configurations can be used:

Gain configuration: the channel can be set in gain, the input can be set to any voltage within the V_{icm} operating range.

Comparator configuration: the channel can be set to a comparator configuration (without negative feedback). In this case, positive and negative inputs can be set to any value provided these values are significantly different (100 mV or more, to avoid oscillation between positive and negative state).

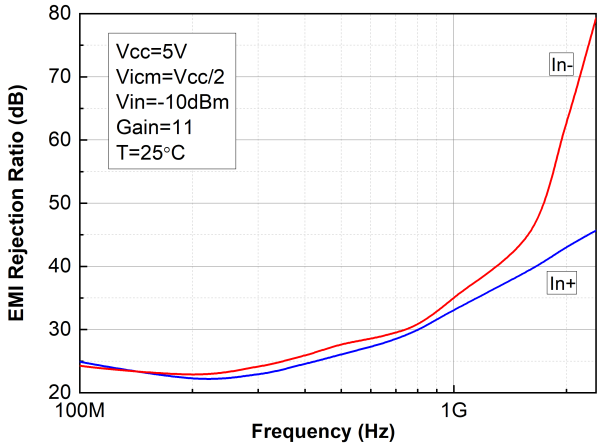
5.4 EMI rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. EMIRR is defined in equation 9:

$$EMIRR = 20 . log\left(\frac{V_{in\,pp}}{\Delta V_{io}}\right) \quad (2)$$

The TSV7722 has been specially designed to minimize susceptibility to EMIRR and shows a low sensitivity. As can be seen in the figure below, EMI rejection ratio has been measured on both inputs and output, from 400 MHz to 2.4 GHz.

Figure 43. **EMIRR on In+, In- and Out pins**



EMIRR performances might be improved by adding small capacitances (in the pF range) on the inputs, power supply and output pins.

These capacitances help to minimize the impedance of these nodes at high frequencies.

5.5 Maximum power dissipation

The usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the TSV7722 is 150°C. The junction temperature can be estimated as follows:

$$T_J = P_D \times \theta_{JA} + T_A \quad (3)$$

T_J is the die junction temperature

P_D is the power dissipated in the package

θ_{JA} is the junction to ambient thermal resistance of the package.

T_A is the ambient temperature.

The power dissipated in the package P_D is the sum of the quiescent power dissipated and the power dissipated by the output stage transistor. It is calculated as follows:

$P_D = (V_{CC} \times I_{CC}) + (V_{CC+} - V_{OUT}) \times ILoad$ when the op amp is sourcing the current.

$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} - V_{CC-}) \times ILoad$ when the op amp is sinking the current.

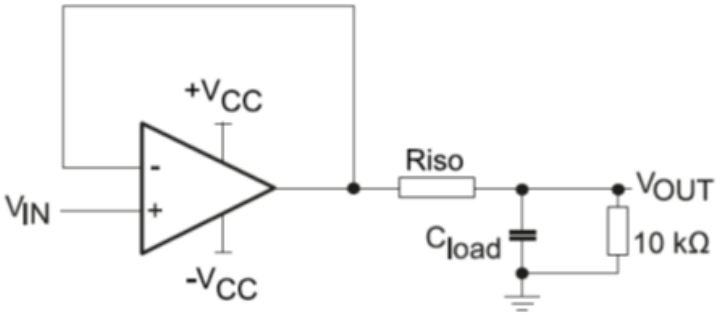
Do not exceed the 150°C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device.

5.6 Capacitive load and stability

Stability analysis must be performed for large capacitive loads over 47 pF; increasing the load capacitance to high values produces gain peaking in the frequency response, with overshoot and ringing in the step response.

Generally, unity gain configuration is the worst situation for stability and the ability to drive large capacitive loads. For additional capacitive load drive capability in unity-gain configuration, stability can be improved by inserting a small resistor R_{ISO} (10 Ω to 22 Ω) in series with the output (see Figure 35). This resistor significantly reduces ringing while maintaining DC performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L. R_{ISO} modifies the maximum capacitive load acceptable from a stability point of view, as described in the figure below:

Figure 44. **Test configuration for R_{ISO}**

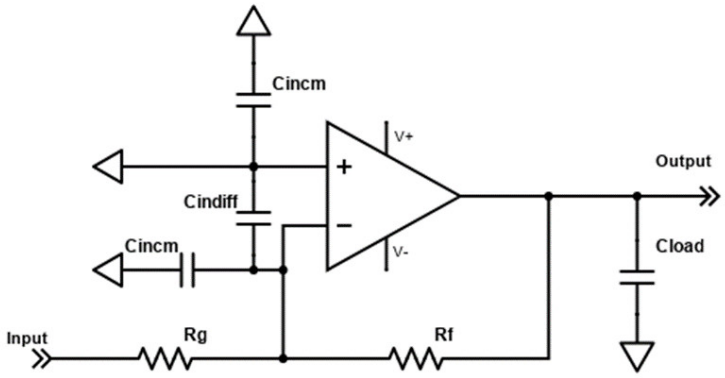


Please note that R_{ISO} = 22 Ω is sufficient to make the TSV7722 stable whatever the capacitive load.

5.7 Resistor values for high speed op amp design

Due to its high gain bandwidth product (GBP), this op amp is particularly sensitive to parasitic impedances. Board parasitics should be taken into account in any sensitive design. Indeed, excessive parasitic (both capacitive and inductive) in the op amp frequency range can alter performances and stability. These issues can often be mitigated by lowering the resistive impedances. More specifically, the RC network created by the schematic resistors (Rf and Rg) and the parasitic capacitances of both the op amp (as documented in Table 3 to Table 5 and illustrated in Figure 45) and the PCB can generate a pole below or in the same order of magnitude than the closed-loop bandwidth of the circuit. In this case, the feedback circuit is not able to fully play its role at high frequency, and the application can be unstable. This issue can happen when the schematic gain is low (typically < 5), or the device is used in follower mode with a resistor in the feedback. In these cases, it is advised to use a low value feedback resistor (Rf), typically 1 kΩ.

Figure 45. **Inverting amplifier configuration with parasitic input capacitances**

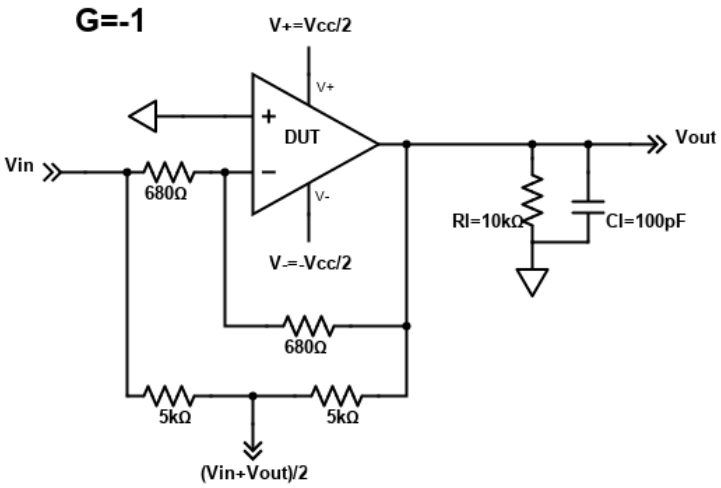


Also, some designs use an input resistor on the positive input, generally of the same value than the input resistance on the negative input. This resistor can be useful to balance the input currents on the positive and negative inputs, and reduce the impact of those input currents on precision. However, this is not useful on the TSV722 as the input currents are very low. Furthermore, this resistor can also interact with the input capacitances to generate a pole. The frequency of this pole should be kept higher than the closed-loop bandwidth frequency. The macromodel provided takes into account the circuit parasitic capacitors. Thus, a transient SPICE simulation (100 mV step) is an easy way to evaluate the stability of the application. However, this cannot replace a hardware evaluation of the application circuit.

5.8 Settling time

Settling time in an application can be defined as the amount of time between the input changes, and the output reaching its final value. It is usually defined with a given tolerance, so the output stability is reached when the output stays within the given range around the final value. In Figures 33 and 34, the settling time is measured in an inverting configuration, using the so-called “false summing node” circuit.

Figure 46. Settling time measurement configuration



This circuit is used with a step input voltage from a positive or negative value, to 0 V. The measurement point being (V_{in} + V_{out}) / 2, and V_{out} being in an ideal circuit equal to V_{in}; the measurement point gives half of the error on V_{out}, comparatively to V_{in}. This error is compared to the tolerance, 0.1% for this circuit, to deduce the settling time. This characteristic is particularly useful when driving an ADC. It is related to the slew rate, GBP and stability of the circuit. It also varies with the circuit gain, the circuit load, and the input voltage step value. However, computing the value of the settling time in a given configuration is not straightforward. The macromodel can give a good estimation, but prototyping can be needed for fine circuit optimization.

5.9 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimizing parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.10 Decoupling capacitor

In order to ensure op amp full functionality, it is mandatory to place a decoupling capacitor of at least 22 nF as close as possible to the op amp supply pins. A good decoupling helps to reduce electromagnetic interference impact.

5.11 Macro model

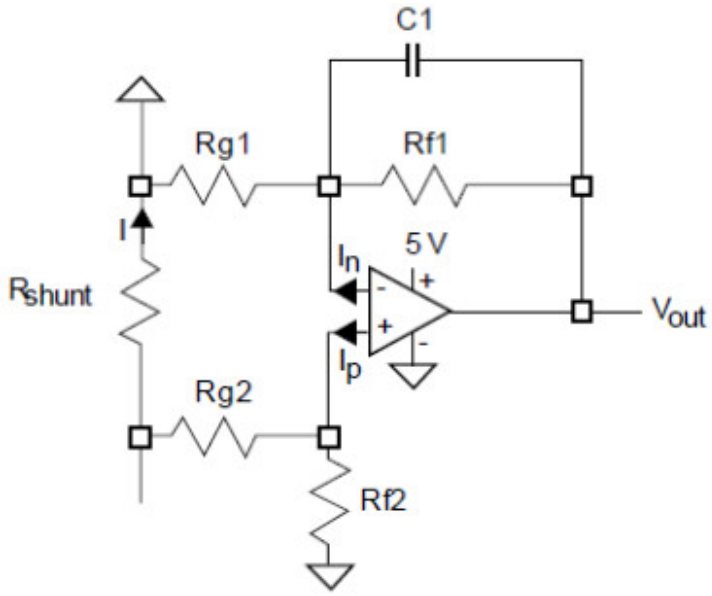
Accurate macro models of the TSV7722 device are available on the STMicroelectronics’ website at: www.st.com. These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSV7722 operational amplifier. They emulate the nominal performance of a typical device at 25°C within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, but they do not replace on-board measurements.

6 Typical applications

6.1 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSV772x (see Figure 48).

Figure 47. Low-side current sensing schematic



V_{out} can be expressed as follows:

$$V_{Out} = R_{shunt} \cdot I \left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right) \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) + I_p \cdot \frac{R_{g2} \cdot R_{f2}}{R_{g2} + R_{f2}} \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n \cdot R_{f1} - V_{io} \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) \quad (4)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, this equation can be simplified as follows:

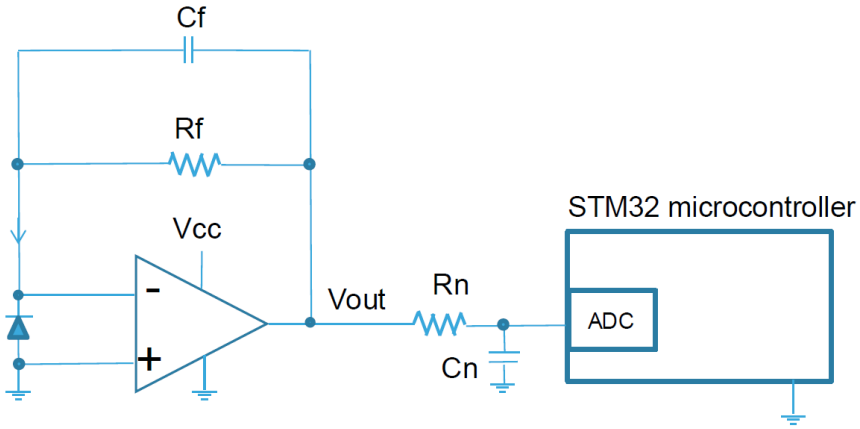
$$V_{Out} = R_{shunt} \cdot I \cdot \frac{R_f}{R_g} - V_{io} \cdot \left(1 + \frac{R_f}{R_g}\right) + R_f \cdot I_{io} \quad (5)$$

The main advantage of using the TSV7722 for a low-side current sensing relies on its low V_{io}, compared to general purpose operational amplifiers. For the same current and targeted accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost. Particular attention must be paid to the matching and precision of R_{g1}, R_{g2}, R_{f1}, and R_{f2}, to maximize the accuracy of the measurement. Furthermore, on the TSV772, the V_{io} is trimmed, and thus reaches his minimum value, at V_{icm} = 0 V. This allows optimized precision for low-side current sensing application without precision degradation due to the CMRR.

6.2 Photodiode transimpedance amplification

The TSV7722, with high bandwidth and slew rate, is well suited for photodiode signal conditioning in a transimpedance amplifier circuit. This application is useful in high performance UV sensors, smoke detectors or particle sensors.

Figure 48. Photodiode transimpedance amplifier circuit



The transimpedance amplifier circuit converts the small photodiode output current in the nA range, into a voltage signal readable by an ADC following Equation 12:

$$V_{Out} = R_f \cdot I_{photodiode} \quad (6)$$

The feedback resistance is usually in the MΩ range, in order to get a large enough voltage output range. However, together with the diode parasitic capacitance, the op amp input capacitances and the PCB stray capacitance, this feedback network creates a pole that makes the circuit oscillate. Using a small (few pF) capacitor in parallel with the feedback resistor is mandatory to stabilize the circuit. The value of this capacitor can be tuned to optimize the application settling time with a SPICE simulation using the op amp macromodel, or by prototyping.

For more details on tuning this circuit, please read the application note AN4451.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SOT23-5 package information

Figure 49. **SOT23-5 package outline**

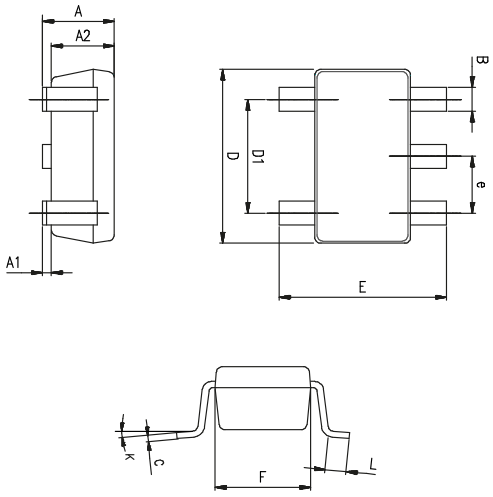


Table 6. **SOT23-5 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.020
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0°		10°	0°		10°

7.2 DFN8 2x2 package information

Figure 50. **DFN8 2x2 package outline**

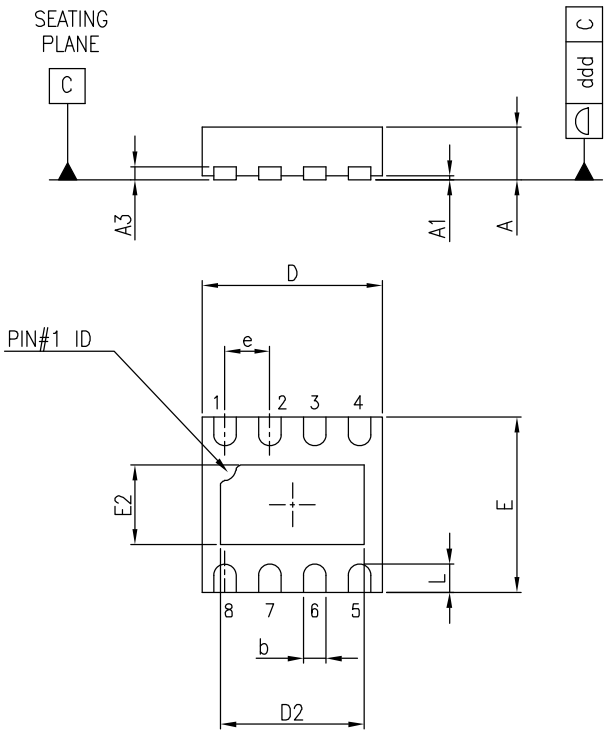
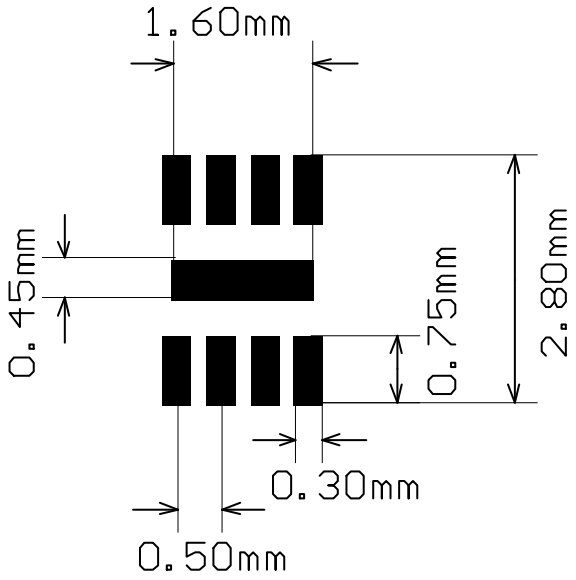


Table 7. **DFN8 2x2 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L	0.225	0.325	0.425	0.009	0.013	0.017
ddd			0.08			0.003

Figure 51. **DFN8 2x2 recommended footprint**



Note: The exposed pad of the DFN8 2x2 can be connected to VCC- or left floating.

7.3 MiniSO8 package information

Figure 52. **MiniSO8 package outline**

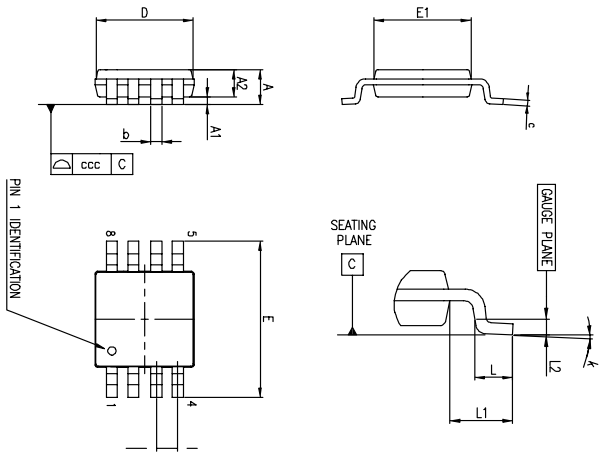


Table 8. **MiniSO8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

7.4 SO-8 package information

Figure 53. **SO-8 package outline**

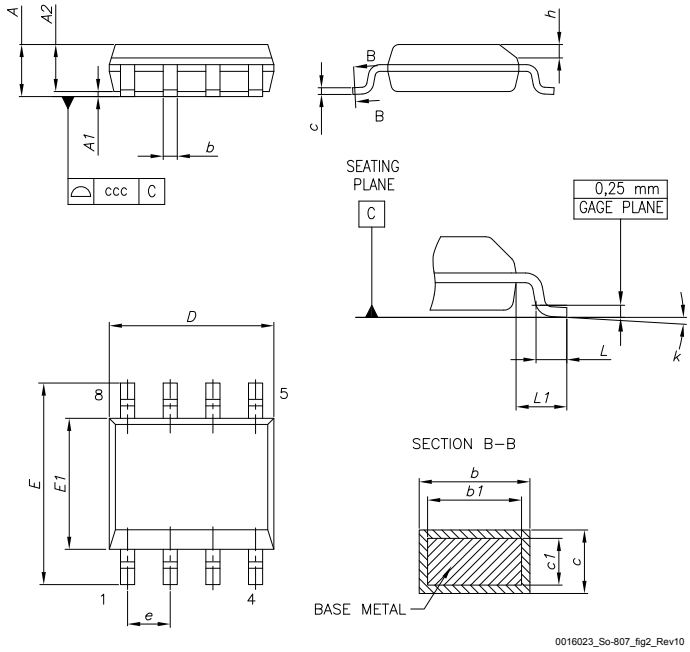


Table 9. **SO-8 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

7.5 MiniSO10 package information

Figure 54. **MiniSO10 package outline**

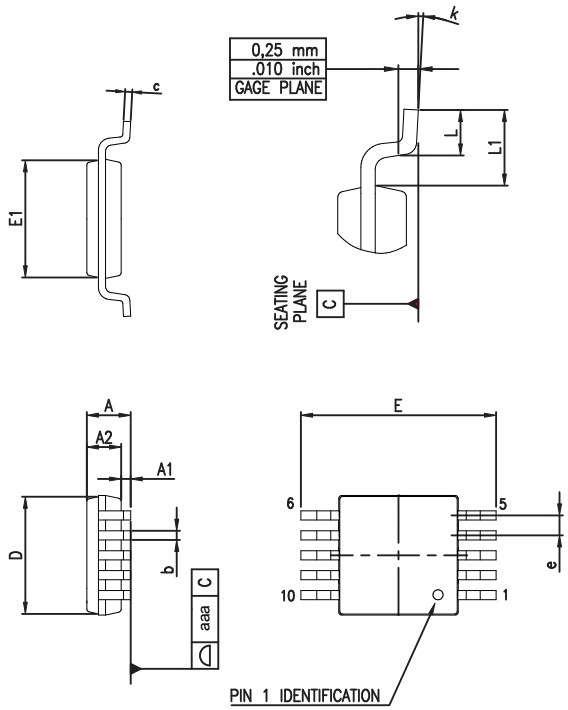


Table 10. **MiniSO10 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.10			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.034	0.037
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.15	0.23	0.30	0.006	0.009	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.50			0.020	
L	0.40	0.55	0.70	0.016	0.022	0.028
L1		0.95			0.037	
k	0 °	3 °	6 °	0 °	3 °	6 °
aaa			0.10			0.004

8 Ordering information

Table 11. Order code

Order code	Temperature range	Package	Channel	Automotive	Marking
TSV7721ILT	-40 to +125°C	SOT23-5	1		K2A
TSV7721IYLT	-40 to +125°C Automotive grade	SOT23-5	1	•	K217
TSV7722IQ2T	-40 to +125°C	DFN8 2x2	2		K2A
TSV7722IST		MiniSO8	2		K2A
TSV7722IDT		SO8	2		TSV7722I
TSV7723IST		MiniSO10	2		K2A
TSV7722IYST	-40 to +125°C Automotive grade	MiniSO8	2	•	K217
TSV7722IYDT		SO8	2	•	TSV7722Y

1. *Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are ongoing.*

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
20-Jan-2021	1	Initial release.

Contents