



**MICROCHIP**

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**PIC18F46J11 Family  
Data Sheet**

28/44-Pin, Low-Power,  
High-Performance Microcontrollers  
with nanoWatt XLP Technology

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**QUALITY MANAGEMENT SYSTEM  
CERTIFIED BY DNV  
== ISO/TS 16949:2002 ==**



# PIC18F46J11 FAMILY

## 28/44-Pin, Low-Power, High-Performance Microcontrollers

### Power Management Features with nanoWatt XLP for Extreme Low Power:

- Deep Sleep mode: CPU off, Peripherals off, Currents Down to 13 nA and 850 nA with RTCC
  - Able to wake-up on external triggers, programmable WDT or RTCC alarm
  - Ultra Low-Power Wake-up (ULPWU)
- Sleep mode: CPU off, Peripherals off, SRAM on, Fast Wake-up, Currents Down to 105 nA Typical
- Idle: CPU off, Peripherals on, Currents Down to 2.3  $\mu$ A Typical
- Run: CPU on, Peripherals on, Currents Down to 6.2  $\mu$ A Typical
- Timer1 Oscillator/w RTCC: 1  $\mu$ A, 32 kHz Typical
- Watchdog Timer: 813 nA, 2V Typical

### Special Microcontroller Features:

- 5.5V Tolerant Inputs (digital only pins)
- Low-Power, High-Speed CMOS Flash Technology
- C Compiler Optimized Architecture for Re-Entrant Code
- Priority Levels for Interrupts
- Self-Programmable under Software Control
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Operating Voltage Range of 2.0V to 3.6V
- On-Chip 2.5V Regulator
- Flash Program Memory of 10,000 Erase/Write Cycles Minimum and 20-Year Data Retention

### Peripheral Highlights:

- Peripheral Pin Select:
  - Allows independent I/O mapping of many peripherals
  - Continuous hardware integrity checking and safety interlocks prevent unintentional configuration changes
- Hardware Real-Time Clock and Calendar (RTCC):
  - Provides clock, calendar and alarm functions
- High-Current Sink/Source 25 mA/25 mA (PORTB and PORTC)

### Peripheral Highlights (Continued):

- Four Programmable External Interrupts
- Four Input Change Interrupts
- Two Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
  - Pulse steering control
- Two Master Synchronous Serial Port (MSSP) modules featuring:
  - 3-wire SPI (all 4 modes)
  - 1024-byte SPI Direct Memory Access (DMA) channel
  - I<sup>2</sup>C™ Master and Slave modes
- 8-Bit Parallel Master Port/Enhanced Parallel Slave Port
- Two-Rail – Rail Analog Comparators with Input Multiplexing
- 10-Bit, up to 13-Channel Analog-to-Digital (A/D) Converter module:
  - Auto-acquisition capability
  - Conversion available during Sleep
  - Self-Calibration
- High/Low-Voltage Detect module
- Charge Time Measurement Unit (CTMU):
  - Supports capacitive touch sensing for touch screens and capacitive switches
  - Provides a Precise Resolution Time Measurement for Both Flow Measurement and Simple Temperature Sensing
- Two Enhanced USART modules:
  - Supports RS-485, RS-232 and LIN/J2602
  - Auto-wake-up on Start bit
- Auto-Baud Detect

### Flexible Oscillator Structure:

- 1% Accurate High-Precision Internal Oscillator
- Two External Clock modes, up to 48 MHz (12 MIPS)
- Low-Power 31 kHz Internal RC Oscillator
- Tunable Internal Oscillator (31 kHz to 8 MHz,  $\pm 0.15\%$  Typical,  $\pm 1\%$  Max).
- 4x PLL Option
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops
- Two-Speed Oscillator Start-up
- Programmable Reference Clock Output Generator

# PIC18F46J11 FAMILY

PIC18F/LF <sup>(1)</sup> Device	Pins	Program Memory (bytes)	SRAM (bytes)	Remappable Pins	Timers 8/16-Bit	ECCP/(PWM)	EUSART	MSSP		10-Bit A/D (ch)	Comparators	Deep Sleep	PMP/PSP	CTMU	RTCC	
								SPI w/DMA	I <sup>2</sup> C™							
PIC18F24J11	28	16K	3776	19	2/3	2	2	2	Y	Y	10	2	Y	N	Y	Y
PIC18F25J11	28	32K	3776	19	2/3	2	2	2	Y	Y	10	2	Y	N	Y	Y
PIC18F26J11	28	64K	3776	19	2/3	2	2	2	Y	Y	10	2	Y	N	Y	Y
PIC18F44J11	44	16K	3776	25	2/3	2	2	2	Y	Y	13	2	Y	Y	Y	Y
PIC18F45J11	44	32K	3776	25	2/3	2	2	2	Y	Y	13	2	Y	Y	Y	Y
PIC18F46J11	44	64K	3776	25	2/3	2	2	2	Y	Y	13	2	Y	Y	Y	Y
PIC18LF24J11	28	16K	3776	19	2/3	2	2	2	Y	Y	10	2	N	N	Y	Y
PIC18LF25J11	28	32K	3776	19	2/3	2	2	2	Y	Y	10	2	N	N	Y	Y
PIC18LF26J11	28	64K	3776	19	2/3	2	2	2	Y	Y	10	2	N	N	Y	Y
PIC18LF44J11	44	16K	3776	25	2/3	2	2	2	Y	Y	13	2	N	Y	Y	Y
PIC18LF45J11	44	32K	3776	25	2/3	2	2	2	Y	Y	13	2	N	Y	Y	Y
PIC18LF46J11	44	64K	3776	25	2/3	2	2	2	Y	Y	13	2	N	Y	Y	Y

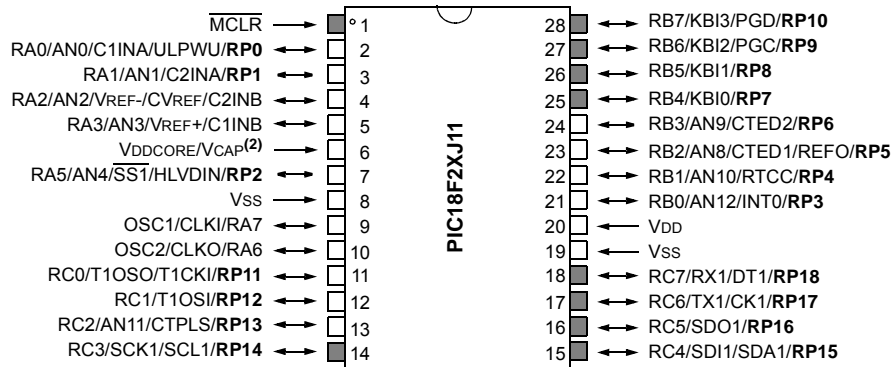
**Note 1:** See [Section 1.3 “Details on Individual Family Devices”](#), [Section 4.6 “Deep Sleep Mode”](#) and [Section 26.3 “On-Chip Voltage Regulator”](#) for details describing the functional differences between PIC18F and PIC18LF variants in this device family.

# PIC18F46J11 FAMILY

## Pin Diagrams

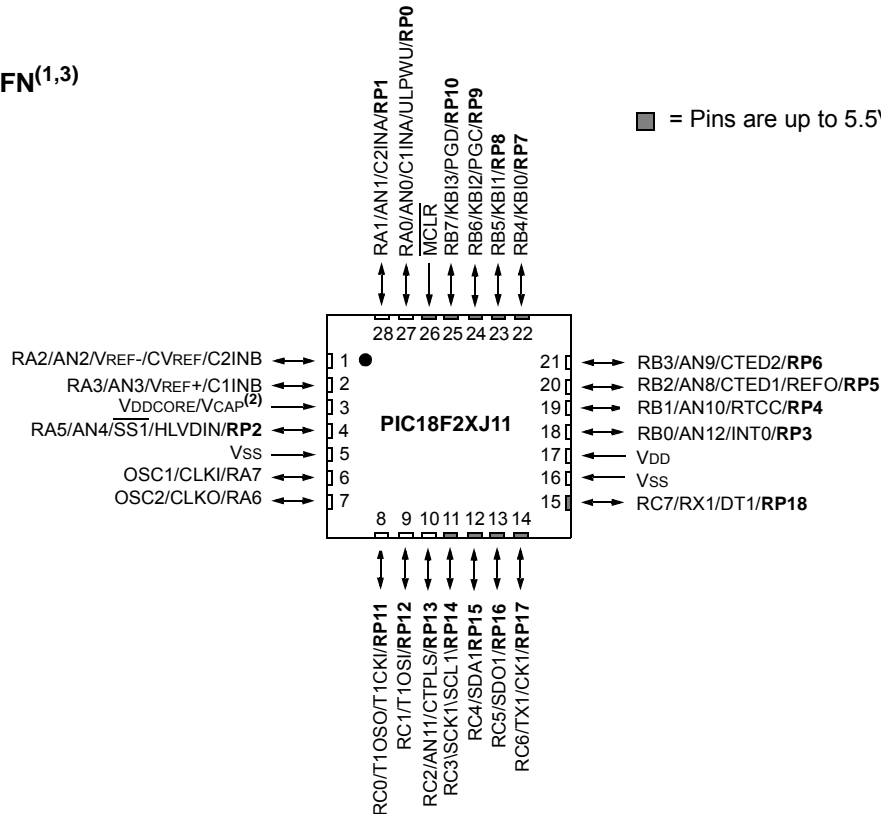
### 28-Pin SPDIP/SOIC/SSOP<sup>(1)</sup>

■ = Pins are up to 5.5V tolerant



### 28-Pin QFN<sup>(1,3)</sup>

■ = Pins are up to 5.5V tolerant



**Legend:** RPn represents remappable pins.

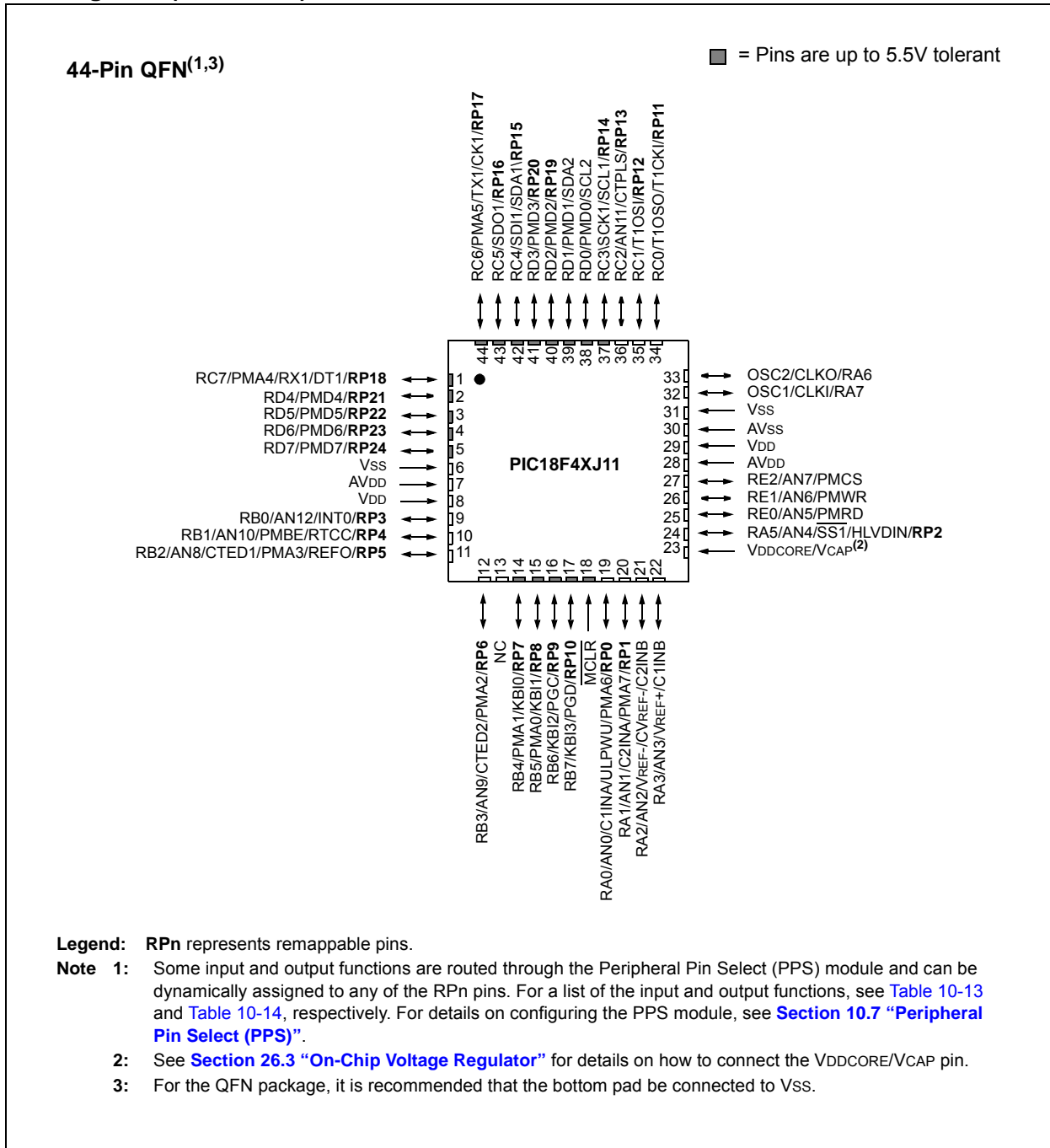
**Note 1:** Some input and output functions are routed through the Peripheral Pin Select (PPS) module and can be dynamically assigned to any of the RPn pins. For a list of the input and output functions, see [Table 10-13](#) and [Table 10-14](#), respectively. For details on configuring the PPS module, see [Section 10.7 "Peripheral Pin Select \(PPS\)"](#).

**2:** See [Section 26.3 "On-Chip Voltage Regulator"](#) for details on how to connect the VDDCORE/VCAP pin.

**3:** For the QFN package, it is recommended that the bottom pad be connected to Vss.

# PIC18F46J11 FAMILY

## Pin Diagrams (Continued)



# PIC18F46J11 FAMILY

## Pin Diagrams (Continued)

