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Evaluating the LTC6226 and the LTC6228 Low Distortion, Rail-to-Rail Output Op Amps with Shutdown

FEATURES

Enables efficient prototyping
User defined circuit configuration
Edge mounted SMA connector provisions
Simplified connection to test equipment and other circuits
RoHS compliant

EVALUATION KIT CONTENTS

EVAL-LTC6226S8 or EVAL-LTC6228IS8

EQUIPMENT NEEDED

Dual output dc power supply
Signal generator
3 banana plug to grabber cables
2 SMA to BNC male cables

EVALUATION BOARD PHOTOGRAPHS

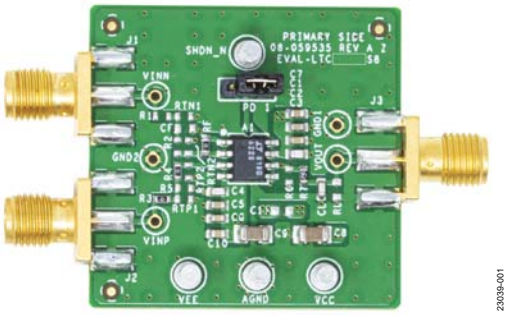

Figure 1. EVAL-LTC6226S8/EVAL-LTC6228IS8, Primary Side

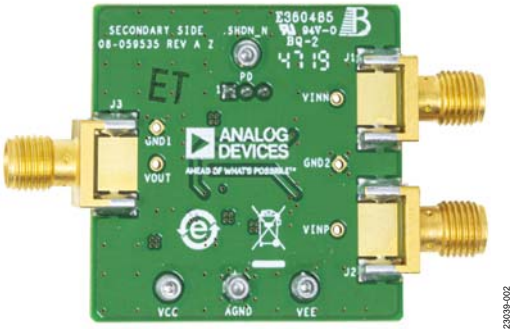

Figure 2. EVAL-LTC6226S8/EVAL-LTC6228IS8, Secondary Side

GENERAL DESCRIPTION

The EVAL-LTC6226S8/EVAL-LTC6228IS8 allow the evaluation of the LTC6226 and the LTC6228, 8-lead, single channel, small outline integrated circuit (SOIC_N), 150 mil op amps. The EVAL-LTC6226S8 and EVAL-LTC6228IS8 are prepopulated boards on a buffer configuration with a post low-pass filter. This configuration allows the LTC6226 and the LTC6228 to be used as a high speed analog-to-digital converter (ADC) drivers. The EVAL-LTC6226S8/EVAL-LTC6228IS8 support other typical configurations of an op amp and have provisions for typical applications of the LTC6226 and the LTC6228, which include an active filter. The SHDN_N pin can be shunt to the VCC pin or the VEE pin, or to an external voltage drive.

The 4-layer EVAL-LTC6226S8/EVAL-LTC6228IS8 accept edge mounted, Subminiature Version A (SMA) connectors on both inputs and outputs to provide an efficient connection to the test equipment and other circuitry. In addition, the EVAL-LTC6226S8/EVAL-LTC6228IS8 have sufficient test points for signal pins and groundings.

Optimized power and ground planes ensure low noise and high speed operation. Component placement and power supply bypassing are optimized for maximum circuit flexibility and performance. The EVAL-LTC6226S8/EVAL-LTC6228IS8 accept C0402 or C0603 surface-mount technology (SMT) components and C1206 bypass capacitors for C8 and C9.

All components are placed on the primary side of the EVAL-LTC6226S8/EVAL-LTC6228IS8, and no components are placed on the secondary side. The EVAL-LTC6226S8 and EVAL-LTC6228IS8 evaluation boards are identical except for the on-board devices.

For full details on the LTC6226 and the LTC6228, see the LTC6226 and the LTC6228 data sheets, which must be consulted in conjunction with this user guide when using the EVAL-LTC6226S8/EVAL-LTC6228IS8.

TABLE OF CONTENTS

REVISION HISTORY

4/2020—Rev. 0 to Rev. A

Added EVAL-LTC6226S8 ..... Universal
Added LTC6226 ..... Universal
Changes to Figure 1 and General Description Section 1
Changes to Using the Evaluation Board for Testing Section 3
Changes to Table 1 7

12/2019—Revision 0: Initial Version

EVALUATION BOARD QUICK START PROCEDURES

The following sections outline the basic prepopulated configuration of the EVAL-LTC6226S8/EVAL-LTC6228IS8 required to test the basic functionality of the LTC6226 or the LTC6228.

POWER SUPPLY CONSIDERATION

Use the turret pins (VCC, VEE, and GND) to power up the EVAL-LTC6226S8/EVAL-LTC6228IS8. Use the correct polarity and voltage level to avoid reverse polarity and overvoltage, which can permanently damage the EVAL-LTC6226S8/EVAL-LTC6228IS8 (see the Using the Evaluation Board for Testing section for more information).

INITIAL BOARD CONFIGURATION

To test the basic functionality of the EVAL-LTC6226S8/ EVAL-LTC6228IS8 and the LTC6226 or the LTC6228, take the following steps:

1. Ensure that all equipment is powered down, including the power supply and the signal generator.
2. Use a banana plug to grabber cable to connect the positive supply, ground, and negative supply to the VCC, GND, and VEE turret pins, respectively.
3. Use an SMA to bayonet Neill-Concelman (BNC) connector to connect the on-board SMA connector test point, VINP, on the J2 connector to a signal generator channel.
4. Use an SMA to BNC connector to connect the on-board SMA connector test point, VOUT, on the J3 connector to an oscilloscope channel.

USING THE EVALUATION BOARD FOR TESTING

When the procedure in the Initial Board Configuration section is complete, implement the following settings and verify the expected output:

1. Set the power supply to +5 V for the positive supply and −5 V for the negative supply.
2. Set the output waveform for both the signal generator channels to a sine wave with a frequency of 1 kHz and a peak-to-peak voltage of 2 V.
3. Set the output load of the signal generator to a high-Z load.
4. Set the oscilloscope termination to 1 MΩ and observe the oscilloscope frequency and the peak-to-peak voltage.
5. When all equipment is set up, turn on the power supply and check the voltage and current consumption of the EVAL-LTC6226IS8/EVAL-LTC6228IS8. The expected current consumption is approximately 6 mA for the LTC6226 and 18 mA for the LTC6228, and the current drawn from the supply must not exceed 10 mA and 25 mA, respectively.
6. Turn on the signal generator when the power supply turns on.
7. Observe the output at the oscilloscope. The output of VOUT is a sine wave with a frequency of 1 kHz and a peak-to-peak voltage of approximately 2 V.

EVALUATION BOARD HARDWARE

POWER SUPPLY BYPASSING

External bypass capacitors, such as C8 and C9, are provided for low level frequency bypassing at the amplifier power pins. Additional capacitors (C1 to C7 and C10) are provided for additional higher level frequency bypassing (see Figure 3).

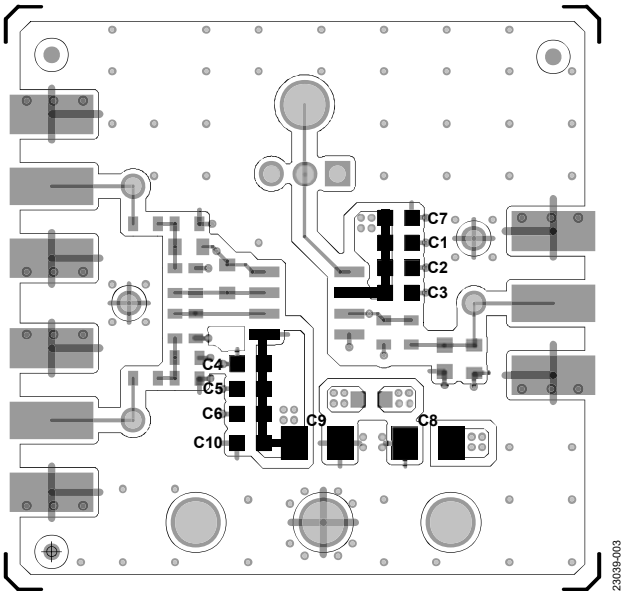

Figure 3. Bypass Capacitor Locations

EVALUATION BOARD STACK UP

The 4-layer board design of the EVAL-LTC6226S8/EVAL-LTC6228IS8 (see Figure 4) provides optimized high speed and low noise performance. The upper ground layer is spaced to provide 50 Ω controlled impedance with the top signal layer to optimize high frequency performance.

The VCC/VEE power plane layer is in between the two ground layers to provide mechanical stability and distributed interplanar capacitance between the power plane layer and the ground layer.

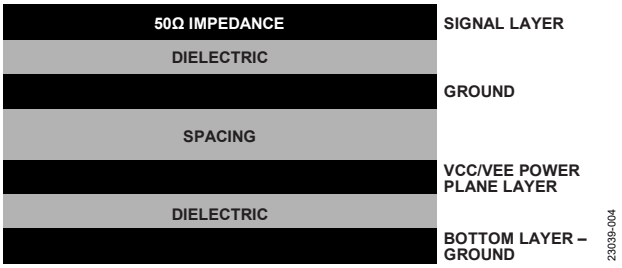

Figure 4. Stack Up

EVALUATION BOARD SCHEMATIC AND ARTWORK

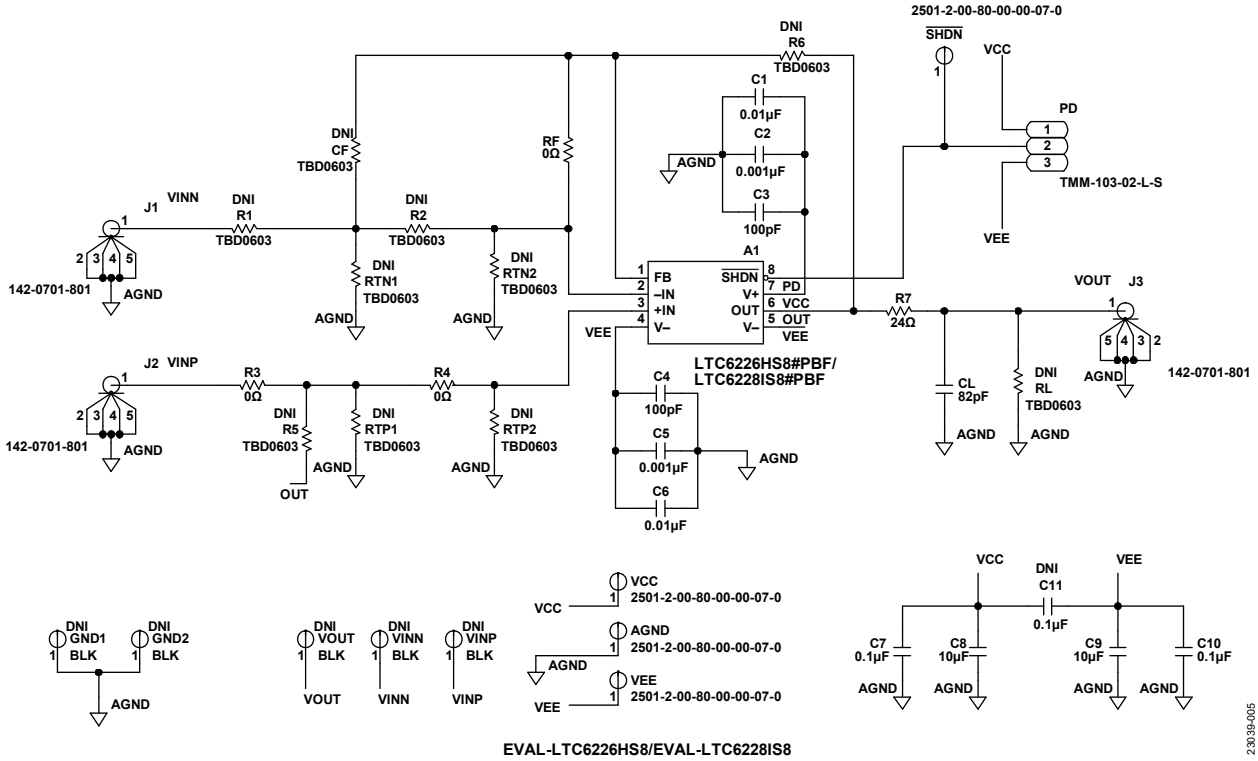

Figure 5. EVAL-LTC6226S8/EVAL-LTC6228IS8 Schematic

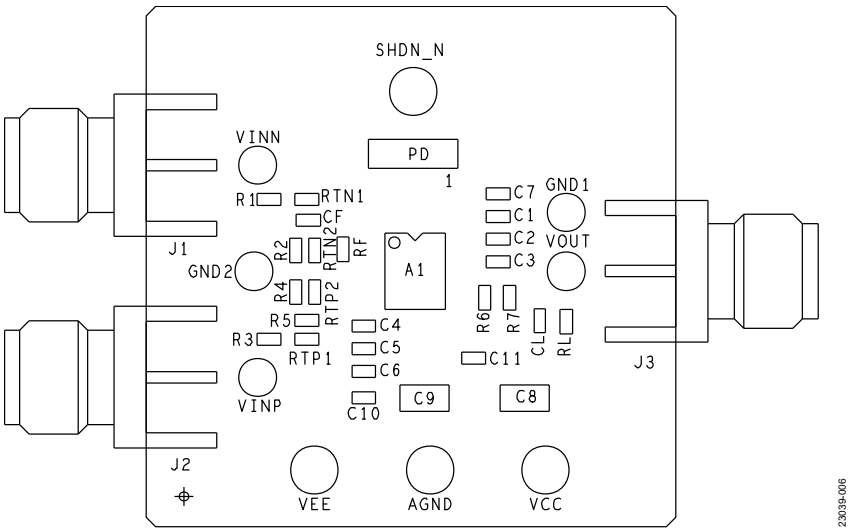

Figure 6. EVAL-LTC6226S8/EVAL-LTC6228IS8 Assembly Drawing, Primary Side

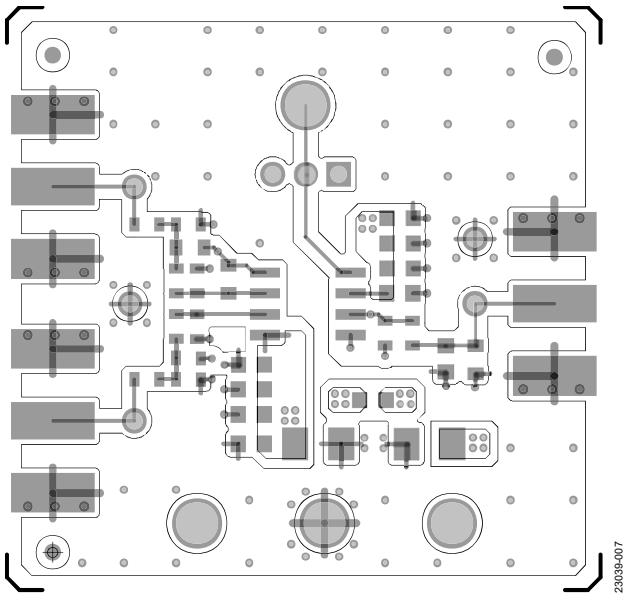

Figure 7. EVAL-LTC6226S8/EVAL-LTC6228IS8 Layout Pattern, Primary Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Qty	Reference Designator	Description	Part Number
1	A1	Rail-to-rail output op amp, LTC6226 or LTC6228	LTC6226S8#PBF or LTC6228IS8#PBF
4	AGND, SHDN_N, VCC, VEE	Terminal turrets	2501-2-00-80-00-00-07-0
10	CF, R1, R2, R5, R6, RL, RTN1, RTN2, RTP1, RTP2	Resistors, user defined, do not install (DNI), R0603/R0402	Not applicable
1	CL	Capacitor, 68 pF (LTC6226) or 82 pF (LTC6228), C0603	2238 867 15829
2	C1, C6	Capacitors, 0.01 µF, C0603	CC0603KRX7R9BB103
2	C2, C5	Capacitors, 0.001 µF, C0603	CC0603KRX7R9BB102
2	C3, C4	Capacitors, 100 pF, C0603	C0603C101K5RAC
2	C7, C10	Capacitors, 0.1 µF, C0603	06035C104KAT2A
2	C8, C9	Capacitors, 10 µF, C1206	GMK316AB7106KL-TR
1	C11	Capacitor, 0.1 µF, DNI, C0603	Not applicable
5	GND1, GND2, VINN, VINP, VOUT	Test points	5001
3	J1, J2, J3	SMA end launch connectors	142-0701-801
1	PD	Pin header	TMM-103-02-L-S
3	R3, R4, RF	Resistors, 0 Ω, R0603	MC0603WG00000T5E-TC
1	R7	Resistor, 33 Ω (LTC6226) or 24 Ω (LTC6228), R0603	MC 0.063W 0603 1% 24R.