

Notification# 20180531005 Datasheet for PCM1860- PCM1865 Information Only

Date: June 01, 2018 To: PREMIER FARNELL PCN

Dear Customer:

This is information-only announcement of a change to a product data sheet for a device that is currently offered by Texas Instruments. The details of this change are on the following pages.

The changes discussed within this notification are for your information only.

Any negotiated alternative change requirements will be provided via the customer's defined process. Customers with previously negotiated, special requirements will be handled separately. Any inquiries should be directed to your local Field Sales Representative.

For questions regarding this notice, contact your local Field Sales Representative or the PCN Manager (<u>PCN ww admin team@list.ti.com</u>).

Sincerely,

PCN Team SC Business Services

Information Only Attachments

Products Affected:

The devices listed on this page are a subset of the complete list of affected devices. According to our records, these are the devices that you have purchased within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

DEVICE	CUSTOMER PART NUMBER
PCM1862DBT	null
PCM1860DBT	null
PCM1861DBT	null
PCM1863DBT	null
PCM1864DBT	null
PCM1865DBT	null

Technical details of this Product Change follow on the next page(s).

PCN Number:	2018053	1005	PCN Date:	June	e 1, 201	8
Title: Datasheet for PCM1860- PCM1865						
Customer Contact:	PCN Manage	er		De	ept:	Quality Services
Change Type:						
Assembly Site		Desi	gn		Wafer	· Bump Site
Assembly Proces	s	🛛 🛛 Data	Sheet		Wafer	Bump Material
		Bump Process				
Mechanical Specification Test Site Wafer		· Fab Site				
Packing/Shipping	J/Labeling	Test	Process		Wafer	Fab Materials
					Wafer	Fab Process
		Notifi	cation Details			
Description of Char						
Texas Instruments In datasheet(s) is being						
further details.				-	-	
in Trans	Texas INSTRUMENTS Burr-Brown Audio PCM1860, PCM1861, PCM1862 PCM1863, PCM1864, PCM1865 Burr-Brown Audio SLAS831D - MARCH 2014-REVISED MARCH 2018					
			S	PC	:M1863, P	CM1864, PCM1865
INSTRUMENTS	(August 2014) to	Revision D	s	PC	:M1863, P	CM1864, PCM1865
INSTRUMENTS Burr-Brown Audio Changes from Revision C Added PCM1860, PCM ⁻	1862, and PCM18	64 and related	I content to this data sheet;	PC LAS831D these d	M1863, P	CM1864, PCM1865 4-REVISED MARCH 2018 Page e previously in
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•	Changed "latch enable" to "word clock" in LRCK pin description	11
•	Added operating ambient temperature and junction temperature to Absolute Maximum Ratings table	12
•	Changed ground voltage differences range from "AGND, DGND" to "AGND to DGND"	12
•	Changed storage temperature max value from 125°C to 150°C	12
•	Changed CDM value from ±1500 V to ±750 V	12
•	Changed "Operating junction temperature range" to "Operating ambient temperature, T _A " in <i>Recommended Operating Conditions</i> table	12
•	Changed Thermal Characteristics table to Thermal Information table	12
•	Changed Electrical Characteristics: Primary PGA and ADC performance to include secondary ADC performance data, and deleted separate Electrical Characteristics: Secondary ADC Performance table	13
•	Added new table note to clarify test condition at 32-dB PGA gain	13
•	Added min value of 85 dB to input channel signal-to-noise ratio for 32 dB	13
•	Changed input channel signal-to-noise ratio for 32 dB typical value from 93 dB to 90 dB	13
•	Added min value of –76 dB to input channel THD+N, differential input for 32 dB	13
•	Deleted "per input pin" and "out of phase" from full-scale voltage input parameter in Electrical Characteristics	13
•	Changed <i>input channel signal-to-noise ratio</i> , single-ended input value for PCM1865 from 110 dB to 106 dB; differential conditions used previously	13
•	Changed "Energysense Detection Threshold" to "Default Energysense Signal Detection Threshold" in Electrical Characteristics, Secondary ADC Performance	13
•	Changed secondary ADC sampling rate from "same as audio sampling rate" to min of 8 kHz and max of 192 kHz	13
•	Changed <i>Electrical Characteristics, DC</i> conditions from master to slave mode; system clock from 256 × f _s to 512 x f _s	14
•	Changed POWER section of the Electrical Characteristics, DC; updated section structure for clarity	14
•	Deleted all rows with XTAL as condition; not required for normal operation	14
•	Deleted all rows with Powerdown; not a valid operating mode	14
•	Changed AVDD current typ value for 2-channel, 3.3-V, active mode from 16 mA to 18 mA	14
•	Changed Total power value for 2-channel, 3.3 V, sleep mode from 24 mW to 17.6 mW	14
•	Changed DVDD current for 2-channel, 3.3 V, standby mode from 353 µA to 0.015 mA	14
•	Changed <i>Total power</i> for 2-channel, 3.3 V, standby mode for software device from 0.59 mW to 0.64 mW	
•	DVDD current for 2-channel, 3.3 V and 1.8 V active mode typ value from 10 µA to 0.015 mA	14
•	Changed Total power for 2-channel, 3.3 V and 1.8 V active mode from 68 mW to 69.2 mW	. 14
•	Changed Total power for 4-channel, 3.3 V, active mode from 145 mW to 135.3 mW	14
•	Changed Total power for 4-channel, 3.3 V and 1.8 V, active mode from 128 mW to 117.3 mW	15
•	Deleted redundant text "Valid with recommended values on analog rails (AVDD, VREF, and so on)" from PSRR	. 15
•	Changed "HPF frequency response" to "HPF -3-dB cutoff frequency" in Electrical Characteristics: Digital Filter	
•	Added maximum BCK frequency rows to Timing Requirements, External Clock table	16
•	Changed all FFT plot X axes from log scale to linear scale	21
•	Added Figure 7	21
•	Changed Figure 9	21
•	Deleted previous Figure 11 and Figure 12	21
•	Added Figure 11	21
•	Added Figure 13	22
•	Added Figure 15	22
•	Changed Overview section for clarity	25
•	Deleted Terminology section; moved content to Overview section	25
•	Added Feature Description section, and moved existing content here	28
•	Changed text in Analog Front End section for clarity	28

•	Changed <i>Mic Bias</i> section; internal resistor is a terminating resistor	. 29
•	Deleted Figure 21 and Figure 22 from <i>Mic Bias</i> section	. 29
•	Added note stating that clocks are required to be running in order to change PGA in the <i>Programmable Gain</i> Amplifier section	31
•	Added text to clarify digital PGA update use in <i>Programmable Gain Amplifier</i> section	
•	Changed note to clarify that the full scale moves to 4.2 V _{RMS} when in differential mode at the end of the <i>Programmable Gain Amplifier</i> section	. 31
•	Added new paragraph to end of Stereo PCM Sources section	. 33
•	Changed Figure 33; clock tree updated and corrected	. 36
•	Added new paragraph to target ADC, DSP1 and DSP2 clock rates in Device Clock Distribution and Generation section	36
•	Changed Clock Configuration and Selection section; relevant to hardware-controlled devices only	. 37
•	Added new paragraph regarding register MST_SCK_SRC to Clock Sources for Software-Controlled Devices section	. 37
•	Added note ("In Master Mode on") to Clock Sources for Software-Controlled Devices section	. 38
•	Changed Table 7; updated descriptions for clarity	. 38
•	Changed "CLK_DIV_MST_SCK" to "CLK_DIV_SCK_BCK" and "CLK_DIV_MST_BCK" to "CLK_DIV_BCK_LRCK" in Table 7	38
•	Changed Figure 34; clock tree updated and corrected	. 38
•	Added "Target Clock Rates for ADC, DSP#1 and DSP#2" section	. 39
•	Changed Table 9; corrected PLL values by increasing P and R by 1, and corrected DSP1 clock divider values	. 40
•	Changed Table 10; corrected PLL values by increasing P and R by 1, and corrected DSP1 clock divider values	. 41
•	Changed Table 12; corrected PLL values by increasing P and R by 1, and corrected typo in DSP2 column title	. 43
•	Changed Table 13; corrected PLL values by increasing P and R by 1, and corrected typo in DSP2 column title	. 44
•	Added text "The clock tree must also be set" to Software-Controlled Devices ADC Non-Audio MCK PLL Mode section	45
•	Changed PLL condition for D = 0000 to show 1 MHz ≤ (PLLCKIN / P) ≤ 20 MHz and 1 ≤ J ≤ 63	. 45
•	Changed PLL condition for D ≠ 0000 to show 6.667 MHz ≤ (PLLCLKIN / P) ≤ 20 MHz and 4 ≤ J ≤ 11	. 45
•	Changed register numbers in Software-Controlled Devices Manual PLL Calculation section to align with the register numbers in Table 14	46
•	Changed Clock Halt and Error section; clock error moved to Clocks section, and interrupt capability deleted	. 46
•	Added Changing Clock Sources and Sample Rates section	. 47
•	Changed Secondary ADC: Energysense and Analog Control section; energysense signal detection not available in active mode	. 48
•	Changed text from "control signals up to 1.65 V" to "control signals up to 4.3 V" in the Secondary ADC Analog Input Range section	. 49
•	Changed section title from "Secondary ADC DC Level Change Detection" to "Secondary ADC <i>Controlsense</i> DC Level Change Detection"	. 49
•	Added text to the Secondary ADC Controlsense DC Level Change Detection section; controlsense is available in both active and sleep modes	. 49
•	Added details to the Secondary ADC Controlsense DC Level Change Detection section regarding how to read simple 8-bit values from the secondary ADC	. 49
•	Added new second paragraph to <i>Energysense</i> section	
•	Changed paragraph after Figure 38 in <i>Energysense Signal Loss Flag</i> section for clarity	
•	Changed <i>Digital Decimation Filters</i> section; clarified two different HPFs in the device	
•	Changed text to clarify digital PGA update use in <i>Digital PGA</i> section	
•	Changed Interrupt Controller section; deleted clock error as an interrupt source	
•	Changed text after Figure 44 in Interrupt Controller section; clarified INT pins all have same logic signal	
•	Added short description in the DIN Toggle Detection section	
•	Added Clearing Interrupts section	

•	Changed Digital Audio Output 2 Configuration see	ction; DOUT2 not available in TDM mo	de, only for 4-ch devices	. 58	
•	Added Time Division Multiplex (TDM Support) section				
•	Changed location of timing diagrams to Specifications section, and deleted Interface Timing section			. 59	
•	Changed text in <i>Bypassing the Internal LDO to Reduce Power Consumption</i> section to clarify TDM mode with 1.8-V IOVDD operation			. 61	
•	Added text "The I ² C control port" to the <i>I²C Interface</i> section			. 64	
•	Changed pin numbers in Table 22 from "15, 16, 14" to "23, 24, 25"			. 64	
•	Added Real World Software Configuration using EnergySense and Controlsense section			. 65	
•	Added more detail to <i>Programming DSP Coefficie</i> location			. 68	
•	Added Dual PCM186x TDM Functionality section			. 73	
•	Added new paragraph to end of Analog Front-End	d Circuit For Single-Ended, Line-In Ap	plications section	. 74	
•	Changed 1.8-V Support section; clarified that both				
•	Added Brownout Conditions section				
•	Added test condition to step 3 in Power Up Seque	ence section; (PLL requires < 250 μs)		. 80	
•	Changed Layout section for clarity				
•	Deleted old Figure 67, PCM1865 EVM Signal Par	-	-		
•	Added Figure 75				
•	Changed "0xFF" to "0xFE" in last sentence of Reg				
•	Changed values for register 3, bits 6-0; changed t				
•	Changed bits 4 and 3 from 1 and 0 to RSV, respe				
•	Changed register 44 (0x2C) from reserved ("RSV				
•	Changed registers 52 and 53 to registers 51 and 52, respectively				
•	Changed TX_WLEN bit option 00 description from "Reserved" to "32-bit" in Page 0, register 11			. 95	
•	 Changed GPIO0_FUNC for 001 from "SPI MISO (Out:Default)" to "Digital MIC Input 0 (In)" and for 010 from "RESERVED" to "SPI MISO (Out)" in register 16				
•	Changed "DPGA" to "APGA" in description column for bits 3, 2, 1, and 0 in register 25 10				
•	Changed DIV_NUM default value in page 0, register 33 from "000 0001" to "000 0000" 10				
•	Changed names and descriptions of master mode clock dividers in registers 37, 38, and 39 for clarity 108				
•	Changed "Divider" to "Multiplier" in R[3:0] descript	ion for register 42		110	
•	Changed values for R[3:0] from 1, 1/2, 1/3, 1/4, ar	-			
•	Changed "Divider" to "Multiplier" in J[5:0] descripti	-	-		
•	Changed "Divider" to "Multiplier" in D_LSB[7:0] de	escription for register 44		111	
•	Changed "Divider" to "Multiplier" in D_MSB[5:0] de	escription for register 45		111	
•	Changed register 52 to register 51			114	
•	Changed register 53 to register 52			115	
•	Changed bit 3 from CLKERR to RSV in register 96			123	
•	Deleted bit 3 from CLKERR to RSV in register 97.			124	
•	• Changed default values in page 1: register 1 for bits 4, 2, 1, and 0 from "1" to "0", and updated descriptions for clarity. 129			129	
	e datasheet number will be changing		~ ~		
De	evice Family	Change From:	Change To:		
L	CM1860- PCM1865	SLVS893C	SLVS893D		
The	ese changes may be reviewed at the	datasheet links provided.			
	p://www.ti.com/product/PCM1860				
	ason for Change:	-			
То	accurately reflect device characterist	ics.			
An	ticipated impact on Fit, Form, Fu	nction, Quality or Reliabi	lity (positive / nega	tive):	
	anticipated impact. This is a specific the actual device.	ation change announcemen	t only. There are no ch	anges	
Changes to product identification resulting from this PCN:					
Nor					
Pro	oduct Affected:				

Γ	PCM1860DBT	PCM1860DBTR	PCM1861DBT	PCM1861DBTR
	PCM1862DBT	PCM1862DBTR	PCM1863DBT	PCM1863DBTR
	PCM1864DBT	PCM1864DBTR	PCM1865DBT	PCM1865DBTR

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
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Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com