PIC18(L)F2X/4X/6XK40

Large Memory, Highly Integrated 8-Bit General Purpose Flash Microcontrollers Product Brief

Description:

PIC18(L)F2X/4X/6XK40 microcontrollers combine large Flash/EE/RAM memory, rich peripheral integration, XLP and 5V support to suit a variety of general purpose applications. These 28-pin, 40-pin and 64-pin devices deliver Core Independent Peripherals such as CWG, WWDT, CRC/Memory Scan, Hardware CVD, Zero-Cross Detect, SMT and Peripheral Pin Select, providing for increased design flexibility and lower system cost.

Core Features:

- C Compiler Optimized RISC Architecture
- Only 83 Instructions
- Operating Speed:
  - 0-64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Interrupt Capability
- 31-Level Deep Hardware Stack
- Up to Five 8-bit Timers/Counters
- Up to Four 16-bit Timers/Counters
- Low Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Extended Watchdog Timer (WDT) with Dedicated On-Chip Oscillator for Reliable Operation
- Programmable Code Protection
- Window Watchdog Timer (WWDT):
  - Timer monitoring of overflow and underflow events
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software

Memory:

- Up to 128 Kbytes Flash Program Memory
- Up to 4096 bytes Data SRAM Memory
- Up to 1024 bytes Data EEPROM

Operating Characteristics:

- Operating Voltage Ranges:
  - 1.8V to 3.6V (PIC18LF2X/4XK40)
  - 2.3V to 5.5V (PIC18F2X/4XK40)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Operating Modes:

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is slower)
- Idle: CPU Halted while Peripherals Operate
- Sleep: Lowest Power Consumption

eXtreme Low-Power (XLP) Features:

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

Digital Peripherals:

- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Up to Five Capture/Compare/PWM (CCP) modules
- PWM: Two 10-Bit Pulse-Width Modulators
- Serial Communications:
  - Up to five Enhanced USART (EUSART)
  - Up to two SPI, I^2C, RS-232, RS-485, LIN compatible
  - Auto-Baud Detect, Auto-wake-up on start
- Up to 53 I/O Pins and One Input-Only Pin:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for fail-safe operation (e.g., Class B)
  - Calculate CRC over any portion of Flash or EEPROM
  - High-speed or background operation
- Hardware Limit Timer (HLT):
  - Hardware monitoring and Fault detection
- Constant Current I/Os

© 2013-2016 Microchip Technology Inc.

- Signal Measurement Timer (SMT):
  - 24-bit signal measurement timer and 24-bit timer/counter
- Hardware Capacitive Voltage Divider (CVD):
  - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
  - Adjustable sample and hold capacitor array
  - Two guard ring output drives
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

Analog Peripherals:

- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 47 external channels
  - Conversion available during Sleep
  - Temperature indicator
- Zero-Cross Detect (ZCD):
  - Detect when AC signal on pin crosses ground
- 5-Bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Programmable 5-bit voltage (% of V_{DD})
  - Internal connections to comparators, Fixed Voltage Reference and ADC
- Up to Three Comparators (CMP):
  - Four external inputs
  - External output via PPS
- Fixed Voltage Reference (FVR) module:
  - 1.024V, 2.048V and 4.096V output levels

Clocking Structure:

- 16 MHz Internal Oscillator Block:
  - ±1% at calibration
  - Selectable frequency range from 1 MHz to 16 MHz
- 32 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Two Crystal/Resonator modes up to 64 MHz
  - External clock up to 64 MHz
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up

Programming/Debug Features:

- In-Circuit Debug Integrated On-Chip
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- x2/x4 PLL for up to 64 MHz from Internal or External Clock Sources

 © 2013-2016 Microchip Technology Inc.

TABLE 1: PIC18(L)F2X/4X/6XK40 FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (bytes)	Data SRAM (bytes)	Data EEPROM (bytes)	I/O Pins	8-bit/16-bit Timers	Comparators	10-bit ADC^2 (ch)	5-bit DAC	Zero-Cross Detect	CCP/10-bit PWM	CWG	HLT	Windowed Watchdog Timer	CRC with Memory Scan	EUSART	I^{2}C/SPI	PPS	Debug$^{(1)}$	SMT
PIC18(L)F24K40	(A)	16k	1024	256	24	4/3	2	24	1	1	2/2	1	3	Y	Y	1	1	Y	I	0
PIC18(L)F25K40	(A)	32k	2048	256	24	4/3	2	24	1	1	2/2	1	3	Y	Y	1	1	Y	I	0
PIC18(L)F26K40	(B)	64k	4096	1024	24	4/3	2	24	1	1	2/2	1	3	Y	Y	2	2	Y	I	0
PIC18(L)F27K40	(C)	128k	4096	1024	24	4/3	2	24	1	1	2/2	1	3	Y	Y	2	2	Y	I	0
PIC18(L)F45K40	(B)	32k	2048	256	35	4/3	2	35	1	1	2/2	1	3	Y	Y	2	2	Y	I	0
PIC18(L)F46K40	(B)	64k	4096	1024	35	4/3	2	35	1	1	2/2	1	3	Y	Y	2	2	Y	I	0
PIC18(L)F47K40	(C)	128k	4096	1024	35	4/3	2	35	1	1	2/2	1	3	Y	Y	2	2	Y	I	0
PIC18(L)F65K40	(D)	32k	2048	1024	53	5/4	3	47	1	1	5/2	1	4	Y	Y	5	2	Y	I	2
PIC18(L)F66K40	(D)	64k	4096	1024	53	5/4	3	47	1	1	5/2	1	4	Y	Y	5	2	Y	I	2
PIC18(L)F67K40	(E)	128k	4096	1024	53	5/4	3	47	1	1	5/2	1	4	Y	Y	5	2	Y	I	2

Note 1: Debugging Methods: (I) – Integrated on Chip; (H) – via ICD Header; E – using Emulation Product.

Data Sheet Index:

- **A.** Future Release PIC18(L)F24K40/25K40 Data Sheet, 28-Pin, 8-bit Flash Microcontrollers
- **B.** Future Release PIC18(L)F26K40/45K40/46K40 Data Sheet, 28/40-Pin, 8-bit Flash Microcontrollers
- **C.** Future Release PIC18(L)F27K40/47K40 Data Sheet, 28/40-Pin, 8-bit Flash Microcontrollers
- **D.** Future Release PIC18(L)F65K40/66K40 Data Sheet, 64-Pin, 8-bit Flash Microcontrollers
- **E.** Future Release PIC18(L)F67K40 Data Sheet, 64-Pin, 8-bit Flash Microcontrollers

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

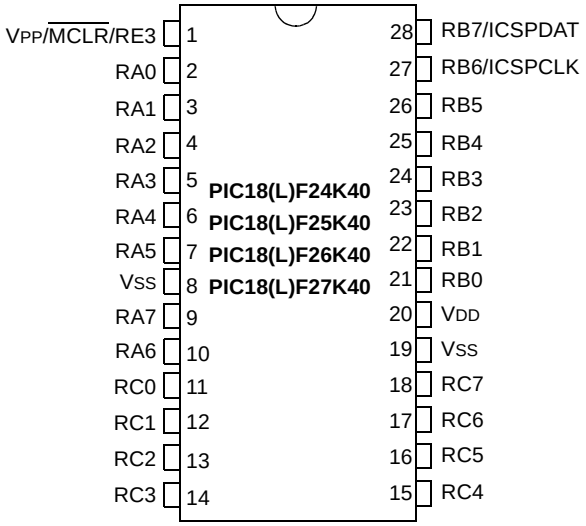
TABLE 2: PACKAGES

Packages	SPDIP (SP)	SOIC (SO)	SSOP (SS)	QFN (ML) (6x6x0.9)	UQFN (MV) (4x4x0.5)	TQFP (PT)	PDIP (P)	UQFN (MV) (5x5x0.5)	QFN (ML) (8x8)	QFN (MR) (9x9)
PIC18(L)F24K40	X	X	X	X	X					
PIC18(L)F25K40	X	X	X	X	X					
PIC18(L)F26K40	X	X	X	X	X					
PIC18(L)F27K40	X	X	X	X						
PIC18(L)F45K40						X	X	X	X	
PIC18(L)F46K40						X	X	X	X	
PIC18(L)F47K40						X	X	X	X	
PIC18(L)F65K40						X				X
PIC18(L)F66K40						X				X
PIC18(L)F67K40						X				X

Note: Pin details are subject to change.

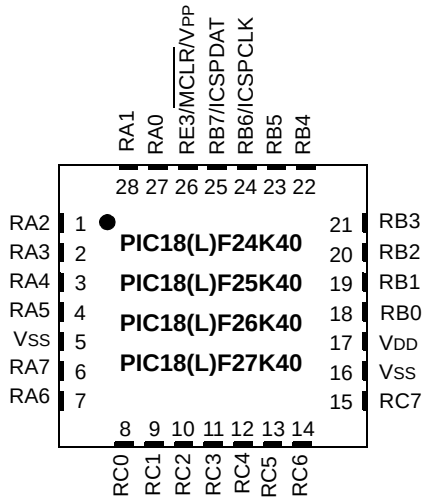
PIN DIAGRAMS

FIGURE 1: 28-PIN PDIP, SOIC, SSOP PIN DIAGRAM FOR PIC18(L)F24K40, PIC18(L)F25K40, PIC18(L)F26K40, PIC18(L)F27K40



Note: See Table 3 for location of all peripheral functions.

FIGURE 2: 28-PIN UQFN (4x4x0.5 mm), QFN (6x6x0.9 mm) PIN DIAGRAM FOR PIC18(L)F24K40, PIC18(L)F25K40, PIC18(L)F26K40, PIC18(L)F27K40

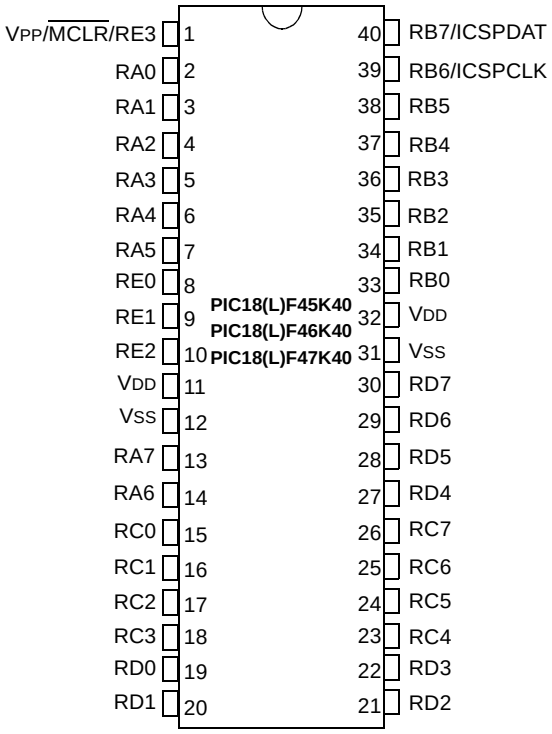


Note 1: See Table 3 for location of all peripheral functions.

2: It is recommended that the exposed bottom pad be connected to VSS.

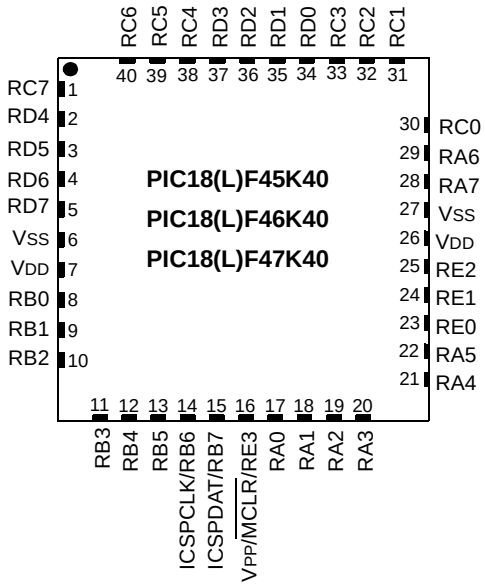
© 2013-2016 Microchip Technology Inc.

FIGURE 3: 40-PIN PDIP PIN DIAGRAM FOR PIC18(L)F45K40, PIC18(L)F46K40, PIC18(L)F47K40



Note: See Table 4 for location of all peripheral functions.

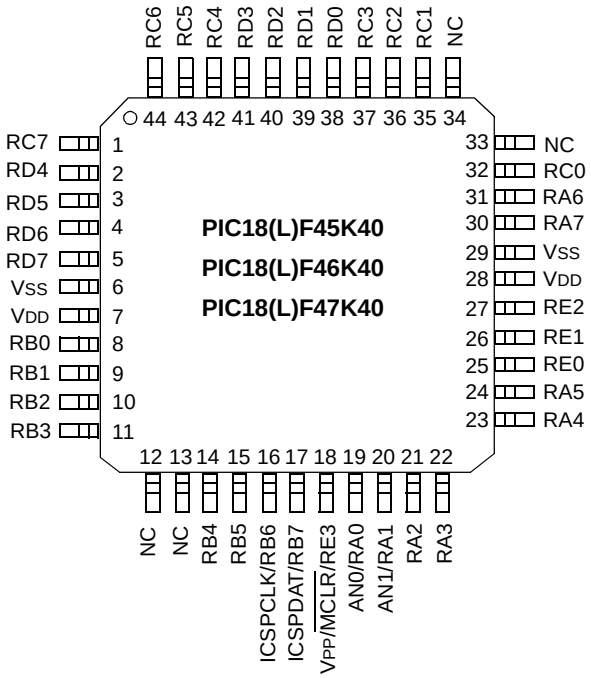
FIGURE 4: 40-PIN UQFN (5x5x0.5 mm) PIN DIAGRAM FOR PIC18(L)F45K40, PIC18(L)F46K40, PIC18(L)F47K40



Note 1: See Table 4 for location of all peripheral functions.

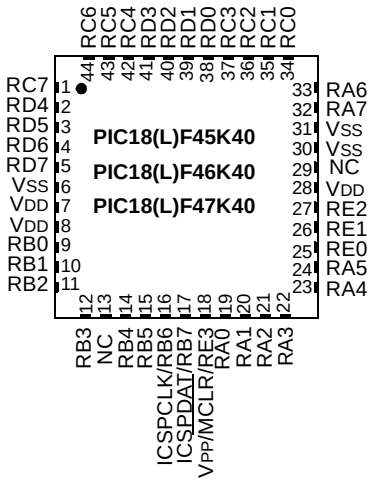
2: It is recommended that the exposed bottom pad be connected to VSS.

FIGURE 5: 44-PIN TQFP PIN DIAGRAM FOR PIC18(L)F45K40, PIC18(L)F46K40, PIC18(L)F47K40



Note: See Table 4 for location of all peripheral functions.

FIGURE 6: 44-PIN QFN (8x8x0.9 mm) PIN DIAGRAM FOR PIC18(L)F45K40, PIC18(L)F46K40, PIC18(L)F47K40

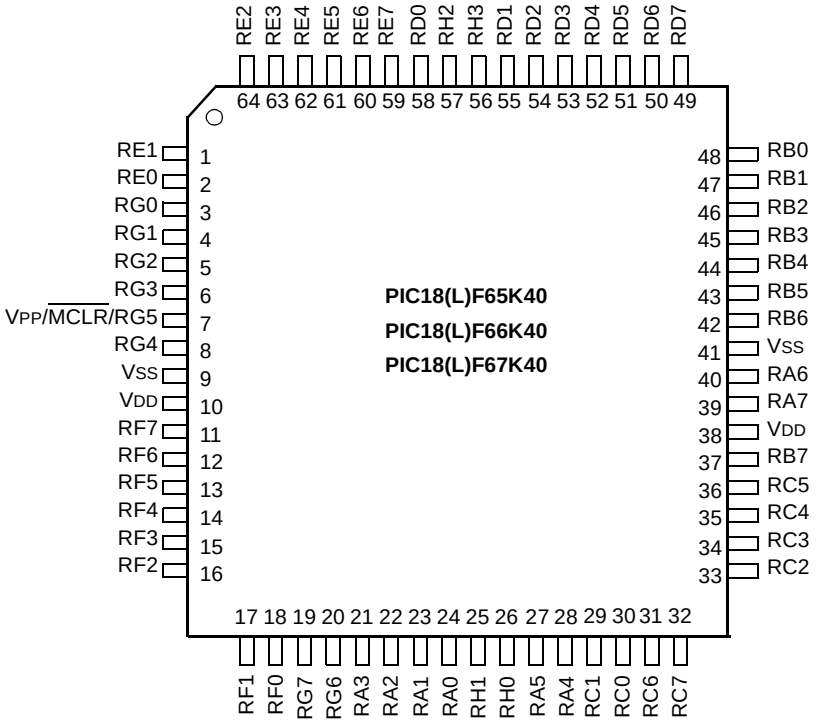


Note 1: See Table 4 for location of all peripheral functions.

2: It is recommended that the exposed bottom pad be connected to VSS.

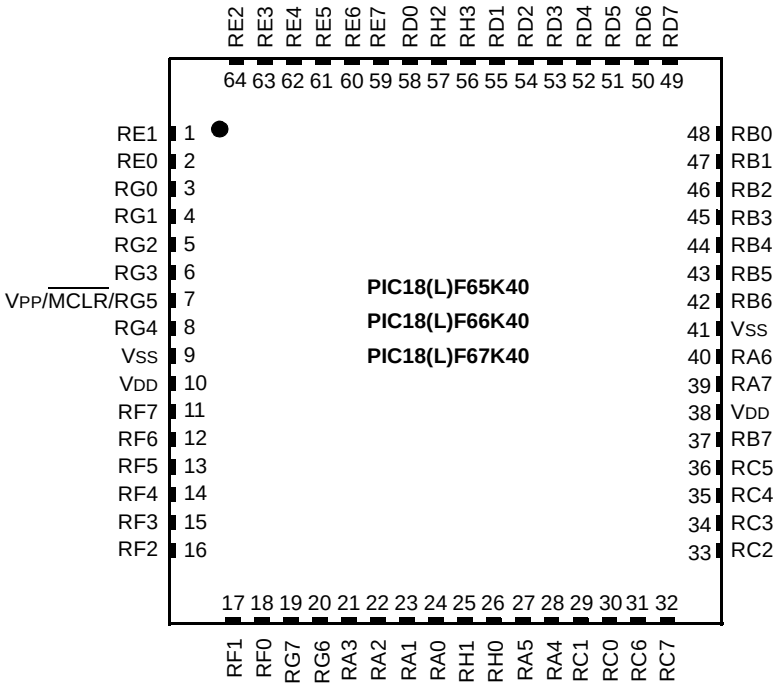
 © 2013-2016 Microchip Technology Inc.

FIGURE 7: 64-PIN TQFP PIN DIAGRAM FOR PIC18(L)F65K40, PIC18(L)F66K40, PIC18(L)F67K40



Note 1: See Table 5 for list of pin peripheral function.

FIGURE 8: 64-PIN QFN (9x9 mm) PIN DIAGRAM FOR PIC18(L)F65K40, PIC18(L)F66K40, PIC18(L)F67K40



Note 1: See Table 5 for list of pin peripheral function.

PIN ALLOCATION TABLES

TABLE 3: 28-PIN ALLOCATION TABLE (PIC18(L)F2XK40)

I/O(2)	28-Pin PDIP, SOIC, SSOP	28-Pin (U)QFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	LVD	Pull-up	Basic
RA0	2	27	AN0	—	C1IN0- C2IN0-	—	—	—	—	IOCA0	—	—	—	—	Y	—
RA1	3	28	AN1	—	C1IN1- C2IN1-	—	—	—	—	IOCA1	—	—	—	—	Y	—
RA2	4	1	AN2	DAC1OUT1 VREF- (DAC5) VREF- (ADC)	C1IN0+ C2IN0+	—	—	—	—	IOCA2	—	—	—	—	Y	—
RA3	5	2	ANA3	VREF+ (DAC5) VREF+ (ADC)	C1IN1+	—	—	—	—	IOCA3	—	MDCIN1(1)	—	—	Y	—
RA4	6	3	—	—	—	T0CKI(1)	—	—	—	IOCA4	—	MDCIN2(1)	—	—	Y	—
RA5	7	4	AN4	—	—	—	—	—	—	IOCA5	—	MDMIN(1)	SSP1SS(1)	LVDIN	Y	—
RA6	10	7	—	—	—	—	—	—	—	IOCA6	—	—	—	—	Y	CLKOUT OSC2
RA7	9	6	—	—	—	—	—	—	—	IOCA7	—	—	—	—	Y	OSC1 ECIN
RB0	21	18	AN12	—	C2IN1+	—	—	CWG1(1)	ZCD	IOCB0 INT0(1)	—	—	—	—	Y	—
RB1	22	19	AN10	—	C1IN3- C2IN3-	—	—	—	—	IOCB1 INT1(1)	—	—	—	—	Y	—
RB2	23	20	AN8	—	—	—	—	—	—	IOCB2 INT2(1)	—	—	—	—	Y	—
RB3	24	21	AN9	—	C1IN2- C2IN2-	—	—	—	—	IOCB3	—	—	—	—	Y	—
RB4	25	22	AN11	—	—	T5G(1)	—	—	—	IOCB4	—	—	—	—	Y	—
RB5	26	23	AN13	—	—	T1G(1)	—	—	—	IOCB5	—	—	—	—	Y	—
RB6	27	24	—	—	—	—	—	—	—	IOCB6	—	—	—	—	Y	ICSPCLK
RB7	28	25	—	DAC1OUT2	—	T6AIN(1)	—	—	—	IOCB7	—	—	—	—	Y	ICSPDAT
RC0	11	8	—	—	—	T1CKI(1) T3CKI(1) T3G(1)	—	—	—	IOCC0	—	—	—	—	Y	SOSCO

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Advance Information
© 2013-2016 Microchip Technology Inc.

TABLE 3: 28-PIN ALLOCATION TABLE (PIC18(L)F2XK40) (CONTINUED)

I/O(2)	28-Pin PDIP, SOIC, SSOP	28-Pin (U)QFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	LVD	Pull-up	Basic
RC1	12	9	—	—	—	—	CCP2(1)	—	—	IOCC1	—	—	—	—	Y	SOSCIN SOSCI
RC2	13	10	AN14	—	—	T5CKI(1)	CCP1(1)	—	—	IOCC2	—	—	—	—	Y	—
RC3	14	11	AN15	—	—	T2AIN(1)	—	—	—	IOCC3	—	—	SSP1CLK(1,3)	—	Y	—
RC4	15	12	AN16	—	—	—	—	—	—	IOCC4	—	—	SSP1DAT(1,3)	—	Y	—
RC5	16	13	AN17	—	—	T4AIN(1)	—	—	—	IOCC5	—	—	—	—	Y	—
RC6	17	14	AN18	—	—	—	—	—	—	IOCC6	TX/CK(1)	—	—	—	Y	—
RC7	18	15	AN19	—	—	—	—	—	—	IOCC7	RX/DT(1)	—	—	—	Y	—
RE3	1	26	—	—	—	—	—	—	—	IOCE3	—	—	—	—	Y	$\overline{\text{MCLR}}$
VSS	19	16	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
AVDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	AVDD
AVSS	8	5	—	—	—	—	—	—	—	—	—	—	—	—	—	AVSS

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

© 2013-2016 Microchip Technology Inc.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC18(L)F4XK40)

I/O(2)	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	LVD	Pull-up	Basic
RA0	2	17	19	19	AN0	—	—	—	—	—	—	IOCA0	—	—	—	—	Y	—
RA1	3	18	20	20	AN1	—	C1IN1- C2IN1-	—	—	—	—	IOCA1	—	—	—	—	Y	—
RA2	4	19	21	21	AN2	DAC1OUT1 VREF- (DAC5) VREF- (ADC)	C1IN0+ C2IN0+	—	—	—	—	IOCA2	—	—	—	—	Y	—
RA3	5	20	22	22	ANA3	VREF+ (DAC5) VREF+ (ADC)	C1IN1+	—	—	—	—	IOCA3	—	MDCIN1(1)	—	—	Y	—
RA4	6	21	23	23		—	—	T0CKI(1)	—	—	—	IOCA4	—	MDCIN2(1)	—	—	Y	—
RA5	7	22	24	24	AN4	—	—	—	—	—	—	IOCA5	—	MDMIN(1)	SSP1SS(1)	LVDIN	Y	—
RA6	14	29	33	31	—	—	—	—	—	—	—	IOCA6	—	—	—	—	Y	CLKOUT OSC2
RA7	13	28	32	30	—	—	—	—	—	—	—	IOCA7	—	—	—	—	Y	OSC1 ECIN
RB0	33	8	9	8	AN12	—	C2IN1+	—	—	CWG1(1)	ZCD	IOCB0 INT0(1)	—	—	—	—	Y	—
RB1	34	9	10	9	AN10	—	C1IN3- C2IN3-	—	—	—	—	IOCB1 INT1(1)	—	—	—	—	Y	—
RB2	35	10	11	10	AN8	—	—	—	—	—	—	IOCB2 INT2(1)	—	—	—	—	Y	—
RB3	36	11	12	11	AN9	—	C1IN2- C2IN2-	—	—	—	—	IOCB3	—	—	—	—	Y	—
RB4	37	12	14	14	AN11	—	—	T5G(1)	—	—	—	IOCB4	—	—	—	—	Y	—
RB5	38	13	15	15	AN13	—	—	T1G(1)	—	—	—	IOCB5	—	—	—	—	Y	—
RB6	39	14	16	16	—	—	—	—	—	—	—	IOCB6	—	—	—	—	Y	ICSPCLK
RB7	40	15	17	17	—	DAC1OUT2	—	T6AIN(1)	—	—	—	IOCB7	—	—	—	—	Y	ICSPDAT
RC0	15	30	34	32	—	—	—	T1CKI(1) T3CKI(1) T3G(1)	—	—	—	IOCC0	—	—	—	—	Y	SOSCO
RC1	16	31	35	35	—	—	—	—	CCP2(1)	—	—	IOCC1	—	—	—	—	Y	SOSCIN SOSCI
RC2	17	32	36	36	AN14	—	—	T5CKI(1)	CCP1(1)	—	—	IOCC2	—	—	—	—	Y	—
RC3	18	33	37	37	AN15	—	—	T2AIN(1)	—	—	—	IOCC3	—	—	SSP1CLK(1,3)	—	Y	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

© 2013-2016 Microchip Technology Inc.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC18(L)F4XK40) (CONTINUED)

I/O[2]	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	LVD	Pull-up	Basic
RC4	23	38	42	42	AN16	—	—	—	—	—	—	IOCC4	—	—	SSP1DAT[1,3]	—	—	—
RC5	24	39	43	43	AN17	—	—	T4AIN[1]	—	—	—	IOCC5	—	—	—	—	Y	—
RC6	25	40	44	44	AN18	—	—	—	—	—	—	IOCC6	—	—	—	—	Y	—
RC7	26	1	1	1	AN19	—	—	—	—	—	—	IOCC7	TX/CK[1]	—	—	—	Y	—
RD0	19	34	38	38	AN20	—	—	—	—	—	—	IOCD0	RX/DT[1]	—	—	—	Y	—
RD1	20	35	39	39	AN21	—	—	—	—	—	—	IOCD1	—	—	—	—	Y	—
RD2	21	36	40	40	AN22	—	—	—	—	—	—	IOCD2	—	—	—	—	Y	—
RD3	22	37	41	41	AN23	—	—	—	—	—	—	IOCD3	—	—	—	—	Y	—
RD4	27	2	2	2	AN24	—	—	—	—	—	—	IOCD4	—	—	—	—	Y	—
RD5	28	3	3	3	AN25	—	—	—	—	—	—	IOCD5	—	—	—	—	Y	—
RD6	29	4	4	4	AN26	—	—	—	—	—	—	IOCD6	—	—	—	—	Y	—
RD7	30	5	5	5	AN27	—	—	—	—	—	—	IOCD7	—	—	—	—	Y	—
RE0	8	23	25	25	AN5	—	—	—	—	—	—	IOCE0	—	—	—	—	Y	—
RE1	9	24	26	26	AN6	—	—	—	—	—	—	IOCE1	—	—	—	—	Y	—
RE2	10	25	27	27	AN7	—	—	—	—	—	—	IOCE2	—	—	—	—	Y	—
RE3	1	16	18	18	—	—	—	—	—	—	—	IOCE3	—	—	—	—	Y	$\overline{MCLR}$
VSS	12	6	6	6	—	—	—	—	—	—	—	—	—	—	—	—	—	AVSS
VDD	11	7	7	7	—	—	—	—	—	—	—	—	—	—	—	—	—	AVDD
VDD	32	26	28	28	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	31	27	30	29	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
VDD	—	—	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
VDD	—	—	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

© 2013-2016 Microchip Technology Inc.

TABLE 5: 64-PIN ALLOCATION TABLE PIC18(L)F6XK40

I/O	64-pin TQFP/QFN	ADC	DAC	Comparators	Zero Cross Detect	MSSP (SPI/I²C)	EUSART	DSM	Timers	SMT	CCP and PWM	CWG	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RA0	24	ANA0	—	C1IN4- C2IN4- C3IN4-	—	—	—	—	T8IN(1)	—	—	—	—	—	—
RA1	23	ANA1	—	—	—	—	—	—	T2IN(1)	—	—	—	—	—	—
RA2	22	VREF- ANA2	VREF-	C1IN1+ C2IN1+ C3IN1+	—	—	—	—	—	—	—	—	—	—	—
RA3	21	VREF+ ANA3	VREF+	—	—	—	—	—	—	—	—	—	—	—	—
RA4	28	ANA4	—	—	—	—	—	—	T0CKI(1)	—	—	—	—	—	—
RA5	27	ANA5	—	—	—	—	—	—	T3G(1)	—	—	—	—	—	—
RA6	40	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	OSC2 CLKOUT
RA7	39	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	OSC1 CLKIN
RB0	48	ANB0	—	—	ZCD	—	—	—	—	—	—	—r	—	INT0(1) IOCB0	—
RB1	47	ANB1	—	—	—	—	—	—	—	—	—	—	—	INT1(1) IOCB1	—
RB2	46	ANB2	—	—	—	—	—	—	—	—	—	—	—	INT2(1) IOCB2	—
RB3	45	ANB3	—	—	—	—	—	—	—	—	—	—	—	INT3(1) IOCB3	—
RB4	44	ANB4	—	—	—	—	—	—	—	—	—	—	—	IOCB4	—
RB5	43	ANB5	—	—	—	—	—	—	T1G(1) T3CKI(1)	—	—	—	—	IOCB5	—
RB6	42	ANB6	—	—	—	—	—	—	—	—	—	—	—	IOCB6	ICSPCLK
RB7	37	ANB7	DAC1OUT2	—	—	—	—	—	—	—	—	—	—	IOCB7	ICSPDAT
RC0	30	—	—	—	—	—	CK4(3)	—	T1CKI(1)	—	—	—	—	IOCC0	SOSCO

Note 1: This is a PPS remappable signal. The input function may be removed from the default location shown to one of several other PORTx pins. Details about this can be found in the data sheet.
2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several POTRTx pin options. Details about this can be found in the data sheet.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I²C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected b the INLVL register, instead of the I²C specific input buffer thresholds.

© 2013-2016 Microchip Technology Inc.

TABLE 5: 64-PIN ALLOCATION TABLE PIC18(L)F6XK40 (CONTINUED)

I/O	64-pin TQFP/QFN	ADC	DAC	Comparators	Zero Cross Detect	MSSP (SPI/I2C)	EUSART	DSM	Timers	SMT	CCP and PWM	CWG	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RC1	29	—	—	—	—	—	RX4(1) DT4(3)	—	T6IN(1)	—	—	—	—	IOCC1	SOSCI
RC2	33	—	—	—	—	—	—	—	—	—	—	CWG1IN(1)	—	IOCC2	—
RC3	34	—	—	—	—	SCL1(3,4) SCK1(1)	—	—	—	—	—	—	—	IOCC3	—
RC4	35	—	—	—	—	SDA1(3,4) SDI1(1)	—	—	—	—	—	—	—	IOCC4	—
RC5	36	—	—	—	—	—	—	—	—	—	—	—	—	IOCC5	—
RC6	31	—	—	—	—	—	CK1(3)	—	—	—	—	—	—	IOCC6	—
RC7	32	—	—	—	—	—	RX1(1) DT1(3)	—	—	—	—	—	—	IOCC7	—
RD0	58	AND0	—	—	—	—	—	—	—	—	—	—	—	—	—
RD1	55	AND1	—	—	—	—	—	—	T5CKI(1) T7G(1)	—	—	—	—	—	—
RD2	54	AND2	—	—	—	—	—	—	—	—	—	—	—	—	—
RD3	53	AND3	—	—	—	—	—	MDCARL(1)	—	—	—	—	—	—	—
RD4	52	AND4	—	—	—	—	—	MDCARH(1)	—	—	—	—	—	—	—
RD5	51	AND5	—	—	—	SDA2(3,4) SDI2(1)	—	MDSRC(1)	—	—	—	—	—	—	—
RD6	50	AND6	—	—	—	SCL2(3,4) SCK2(1)	—	—	—	—	—	—	—	—	—
RD7	49	AND7	—	—	—	$\overline{SS2}$(1)	—	—	—	—	—	—	—	—	—
RE0	2	ANE0	—	—	—	—	CK3(3)	—	—	—	—	—	—	IOCE0	—
RE1	1	ANE1	—	—	—	—	RX3(1) DT3(3)	—	—	—	—	—	—	IOCE1	—
RE2	64	ANE2	—	—	—	—	CK5(3)	—	—	—	—	—	—	IOCE2	—
RE3	63	ANE3	—	—	—	—	RX5(1) DT5(3)	—	—	—	—	—	—	IOCE3	—
RE4	62	ANE4	—	—	—	—	—	—	T4IN(1)	—	CCP5(1)	—	—	IOCE4	—
RE5	61	ANE5	—	—	—	—	—	—	—	—	CCP4(1)	—	—	IOCE5	—

Note 1: This is a PPS remappable signal. The input function may be removed from the default location shown to one of several other PORTx pins. Details about this can be found in the data sheet.
2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several POTRTx pin options. Details about this can be found in the data sheet.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I^2C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected b the INLVL register, instead of the I^2C specific input buffer thresholds.

© 2013-2016 Microchip Technology Inc.

TABLE 5: 64-PIN ALLOCATION TABLE PIC18(L)F6XK40 (CONTINUED)

I/O	64-pin TQFP/QFN	ADC	DAC	Comparators	Zero Cross Detect	MSSP (SPI/I²C)	EUSART	DSM	Timers	SMT	CCP and PWM	CWG	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RE6	60	ANE6	—	—	—	—	—	—	—	SMT1WIN1(1)	CCP3(1)	—	—	IOCE6	—
RE7	59	ANE7	—	—	—	—	—	—	—	SMT1SIG1(1)	—	—	—	IOCE7	—
RF0	18	ANF0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	—
RF1	17	ANF1	—	—	—	—	—	—	—	—	—	—	—	—	—
RF2	16	ANF2	—	—	—	—	—	—	—	—	—	—	—	—	—
RF3	15	ANF3	—	C1IN2- C2IN2- C3IN2-	—	—	—	—	—	—	—	—	—	—	—
RF4	14	ANF4	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—
RF5	13	ANF5	DAC1OUT1	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—
RF6	12	ANF6	—	C1IN0+	—	—	—	—	—	—	—	—	—	—	—
RF7	11	ANF7	—	C1IN3- C2IN3- C3IN3-	—	$\overline{SS1}$(1)	—	—	—	—	—	—	—	—	—
RG0	3	ANG0	—	—	—	—	—	—	—	—	—	—	—	—	—
RG1	4	ANG1	—	—	—	—	CK2(3)	—	—	—	—	—	—	—	—
RG2	5	ANG2	—	C3IN0+	—	—	RX2(1) DT2(3)	—	—	—	—	—	—	—	—
RG3	6	ANG3	—	C3IN0-	—	—	—	—	—	—	CCP1(1)	—	—	—	—
RG4	8	ANG4	—	C3IN1-	—	—	—	—	T5G(1) T7CKI(1)	—	CCP2(1)	—	—	—	—
RG5	7	—	—	—	—	—	—	—	—	—	—	—	—	—	$\overline{MCLR}$ VPP
RG6	20	ANG6	—	—	—	—	—	—	—	SMT2WIN1(1)	—	—	—	—	—
RG7	19	ANG7	—	—	—	—	—	—	—	SMT2SIG1(1)	—	—	—	—	—
RH0	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RH1	25	ADCACT(1)	—	—	—	—	—	—	—	—	—	—	—	—	—
RH2	57	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Note 1: This is a PPS remappable signal. The input function may be removed from the default location shown to one of several other PORTx pins. Details about this can be found in the data sheet.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several POTRTx pin options. Details about this can be found in the data sheet.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I²C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected b the INLVL register, instead of the I²C specific input buffer thresholds.

© 2013-2016 Microchip Technology Inc.

TABLE 5: 64-PIN ALLOCATION TABLE PIC18(L)F6XK40 (CONTINUED)

I/O	64-pin TQFP/QFN	ADC	DAC	Comparators	Zero Cross Detect	MSSP (SPI/I²C)	EUSART	DSM	Timers	SMT	CCP and PWM	CWG	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RH3	56	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VDD	10, 38	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	9, 41	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT(2)	—	ADGRDA ADGRDB	—	C1OUT C2OUT C3OUT	—	SDO1 SCK1 SDO2 SCK2	TX1/CK1(3) DT1(3) TX2/CK2(3) DT2(3) TX3/CK3(3) DT3(3) TX4/CK4(3) DT4(3) TX5/CK5(3) DT5(3)	DSM	TMR0	—	CCP1 CCP2 CCP3 CCP4 CCP5 PWM6OUT PWM7OUT	CWG1A CWG1B CWG1C CWG1D	CLKR	—	—

Note 1: This is a PPS remappable signal. The input function may be removed from the default location shown to one of several other PORTx pins. Details about this can be found in the data sheet.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several POTRTx pin options. Details about this can be found in the data sheet.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I²C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected b the INLVL register, instead of the I²C specific input buffer thresholds.

© 2013-2016 Microchip Technology Inc.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE**.** Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, KeeLoq logo, Kleer, LANCheck, LINK MD, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, ETHERSYNCH, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and QUIET-WIRE are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, RightTouch logo, REAL ICE, Ripple Blocker, Serial Quad I/O, SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2013-2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-0349-4

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

07/14/15