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FDMS86500L

N-Channel PowerTrench® MOSFET

60 V, 158 A, 2.5 mΩ

Features

- Max $r_{DS(on)}$ = 2.5 mΩ at $V_{GS} = 10$ V, $I_D = 25$ A
- Max $r_{DS(on)}$ = 3.7 mΩ at $V_{GS} = 4.5$ V, $I_D = 20$ A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

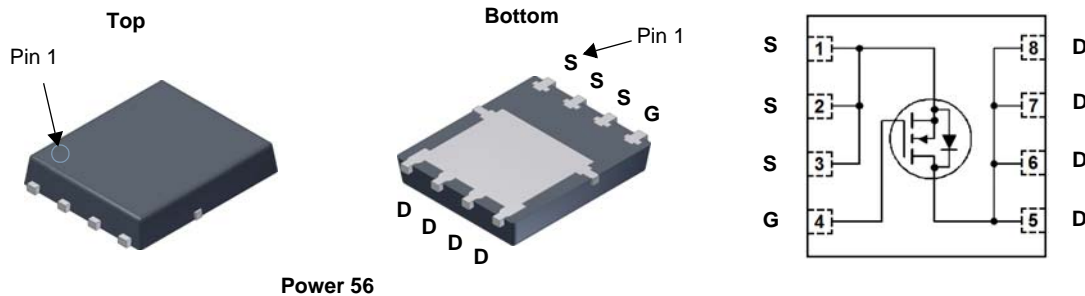


General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or asynchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- Primary Switch in Isolated DC-DC
- Synchronous Rectifier
- Load Switch



Power 56

MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous	$T_C = 25^\circ\text{C}$ (Note 5)	158
	-Continuous	$T_C = 100^\circ\text{C}$ (Note 5)	100
	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	25
	-Pulsed	(Note 4)	799
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	240
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	104
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	2.5
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86500L	FDMS86500L	Power 56	13"	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		30		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 25\text{ A}$		2.1	2.5	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 20\text{ A}$		2.9	3.7	
		$V_{GS} = 10\text{ V}$, $I_D = 25\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		3.1	3.7	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 20\text{ A}$		95		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		9420	12530	pF
C_{oss}	Output Capacitance			1470	1955	pF
C_{rss}	Reverse Transfer Capacitance			50	80	pF
R_g	Gate Resistance		0.1	1.1	3.0	Ω

Switching Characteristics

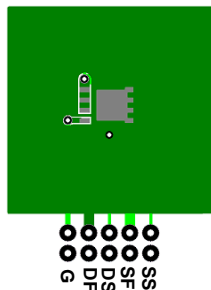
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}$, $I_D = 25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		27	43	ns
t_r	Rise Time			16	28	ns
$t_{d(off)}$	Turn-Off Delay Time			63	100	ns
t_f	Fall Time			7.8	16	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 30\text{ V}$, $I_D = 25\text{ A}$	117	165	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$		54	108	nC
Q_{gs}	Gate to Source Charge			26.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			11.5		nC

Drain-Source Diode Characteristics

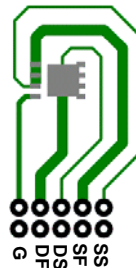
I_s	Continuous Drain to Source Diode Forward Current	$T_C = 25\text{ }^\circ\text{C}$			80	A
$I_{s, pluse}$	Pluse Drain to Source Diode Forward Current	$T_C = 25\text{ }^\circ\text{C}$			799	A
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.1\text{ A}$ (Note 2)		0.68	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 25\text{ A}$ (Note 2)		0.79	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 25\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		54	87	ns
Q_{rr}	Reverse Recovery Charge			42	67	nC
t_{rr}	Reverse Recovery Time	$I_F = 25\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$		46	73	ns
Q_{rr}	Reverse Recovery Charge			84	134	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) $50\text{ }^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b) $125\text{ }^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. E_{AS} of 240 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 40\text{ A}$, $V_{DD} = 54\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 66\text{ A}$.

4. Pulsed I_d please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

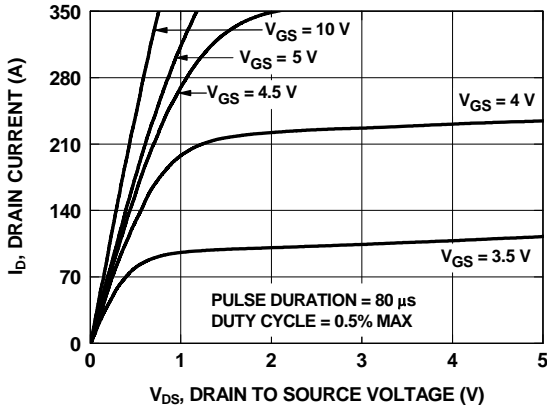


Figure 1. On-Region Characteristics

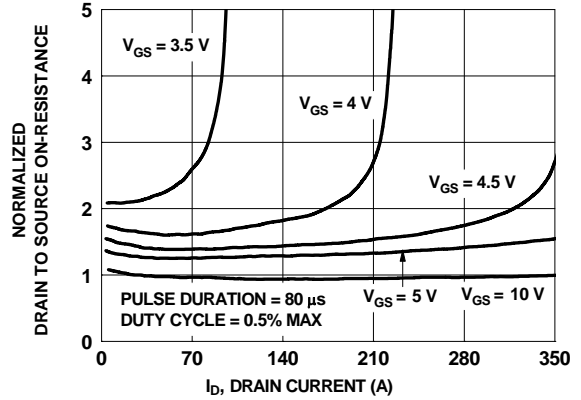


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

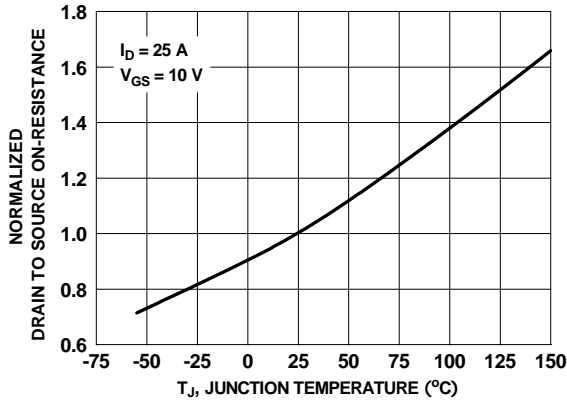


Figure 3. Normalized On-Resistance vs. Junction Temperature

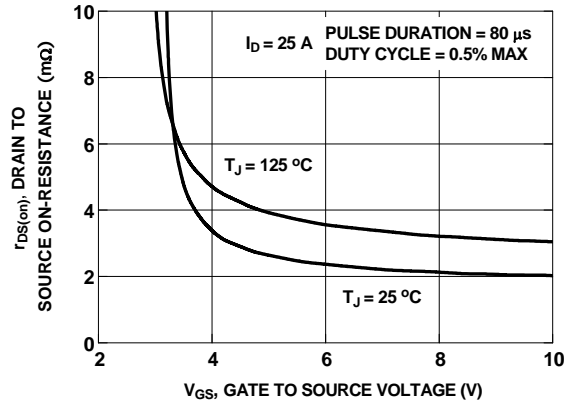


Figure 4. On-Resistance vs. Gate to Source Voltage

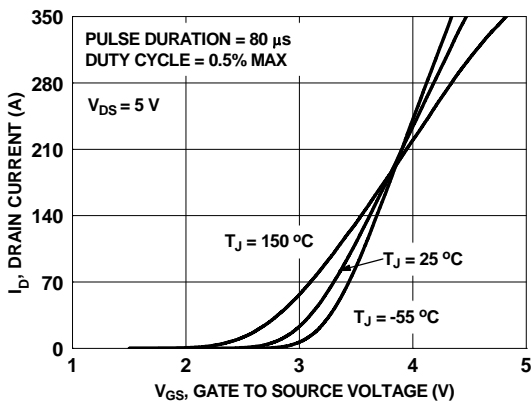


Figure 5. Transfer Characteristics

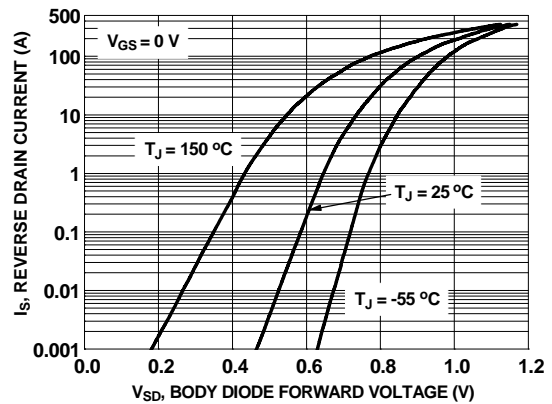


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

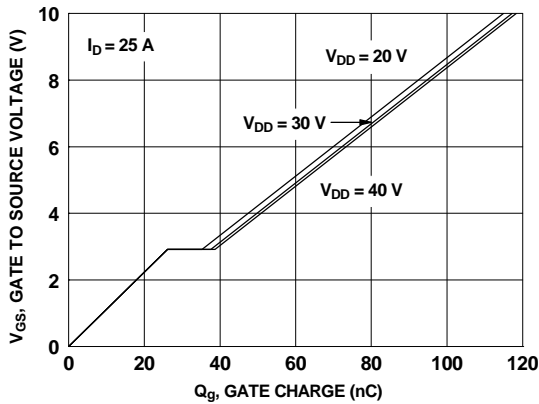


Figure 7. Gate Charge Characteristics

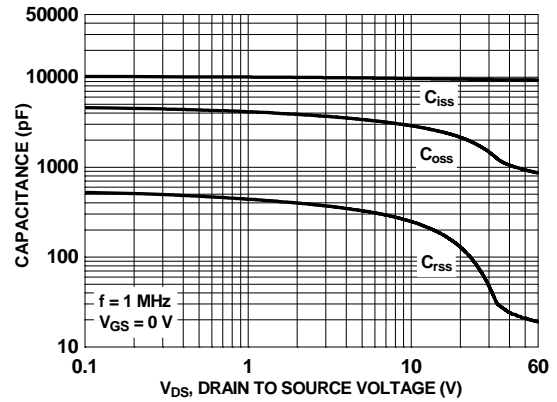


Figure 8. Capacitance vs. Drain to Source Voltage

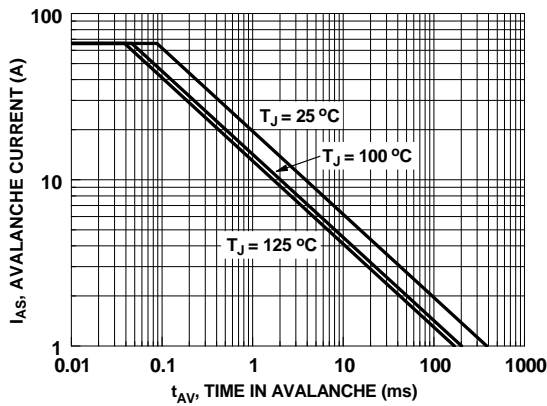


Figure 9. Unclamped Inductive Switching Capability

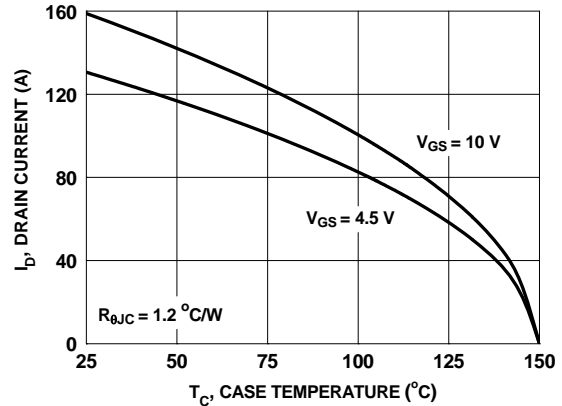


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

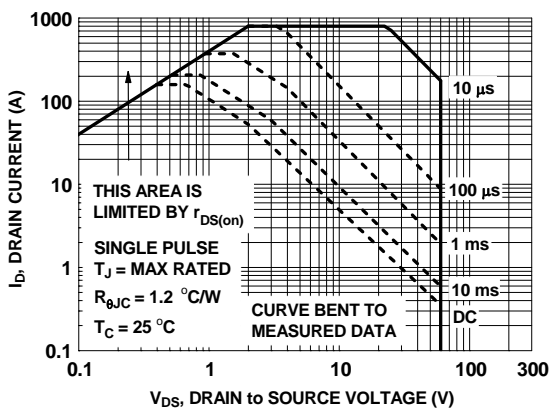


Figure 11. Forward Bias Safe Operating Area

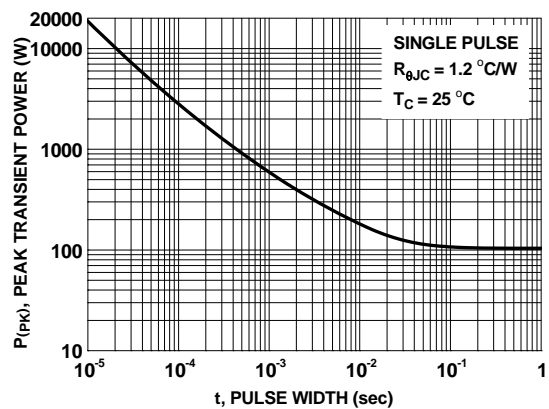


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

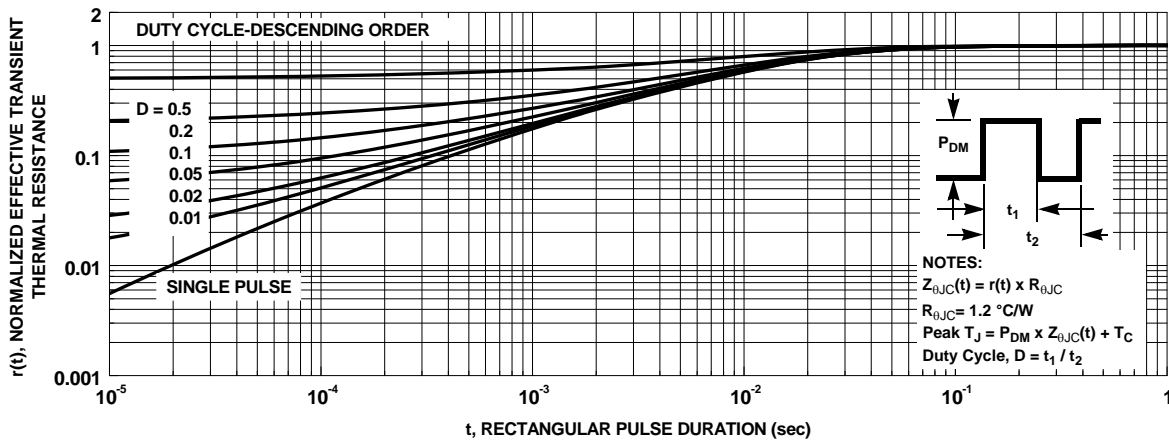
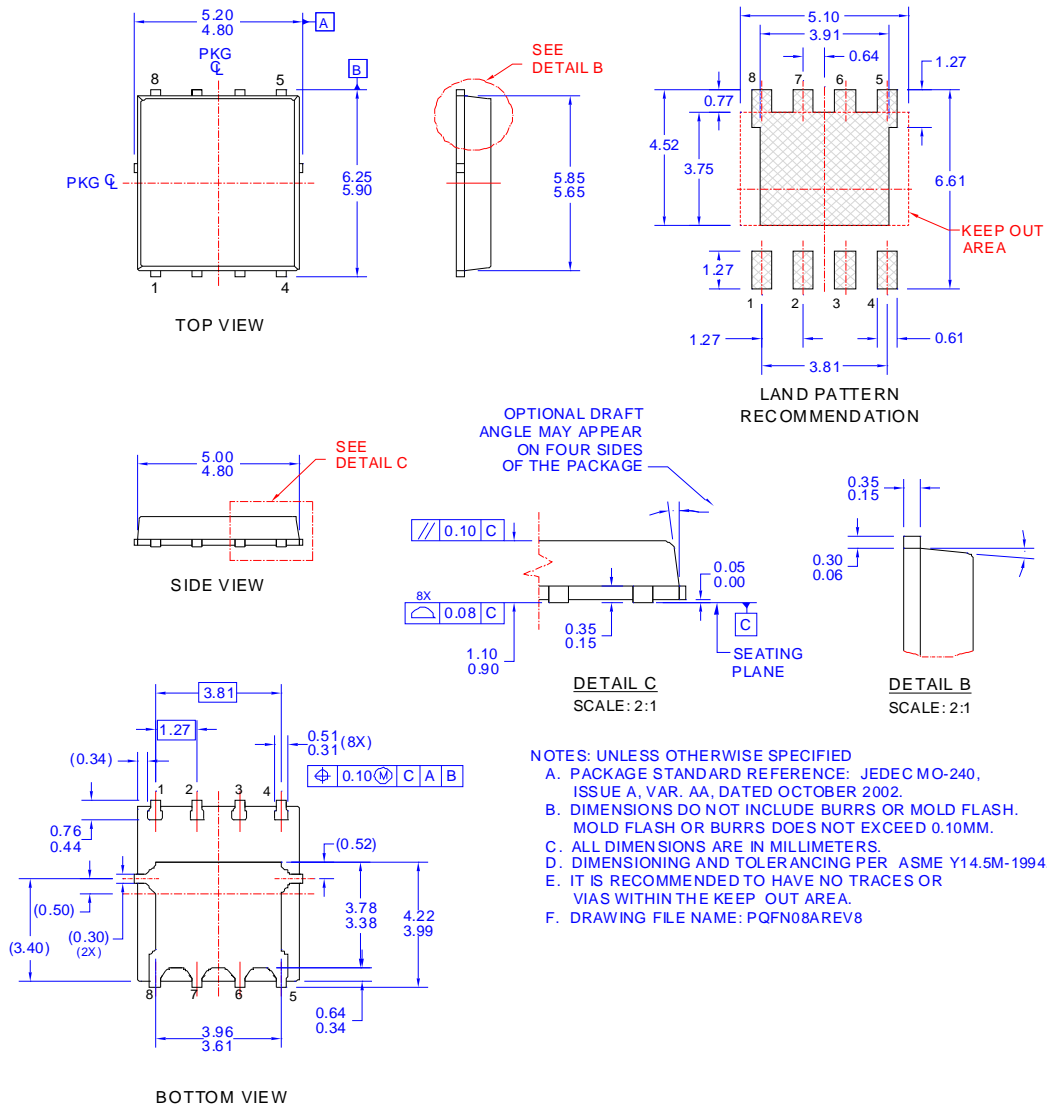
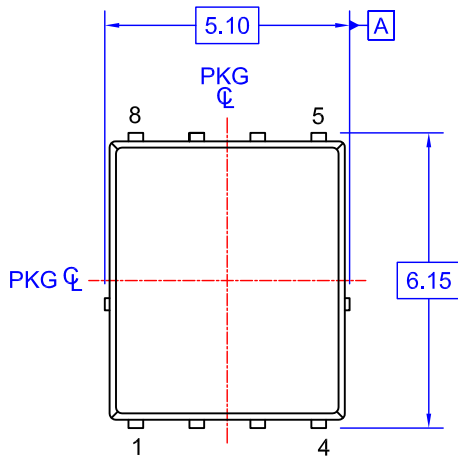


Figure 13. Junction-to-Case Transient Thermal Response Curve

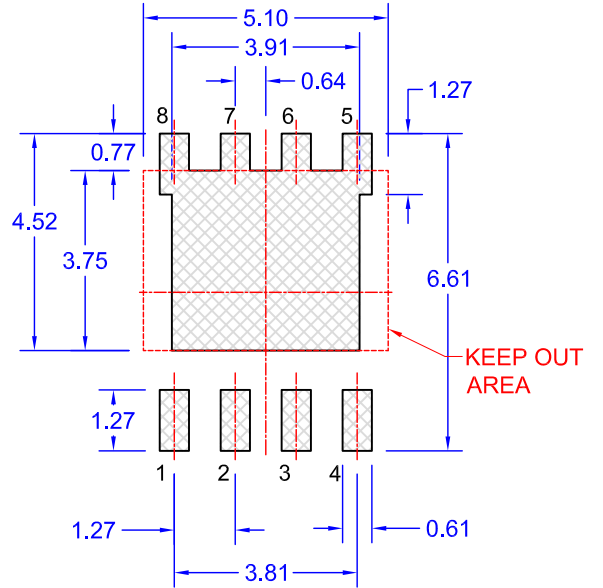
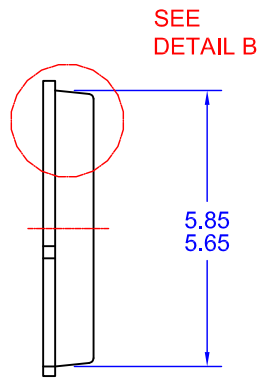
Dimensional Outline and Pad Layout



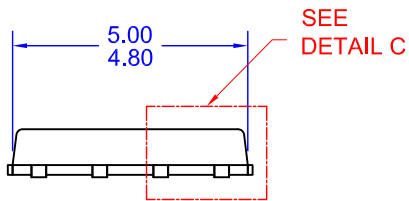
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TOP VIEW

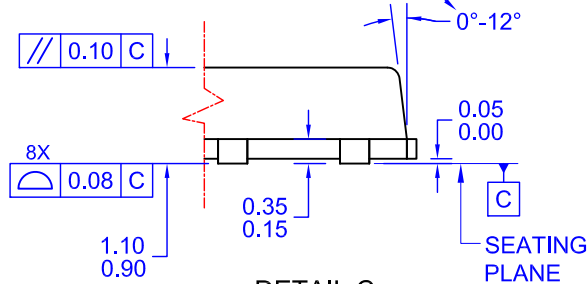


LAND PATTERN RECOMMENDATION

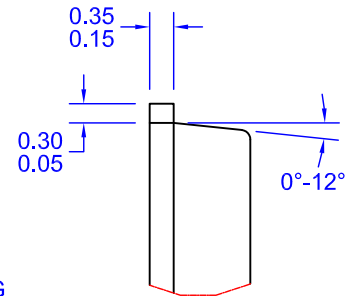


SIDE VIEW

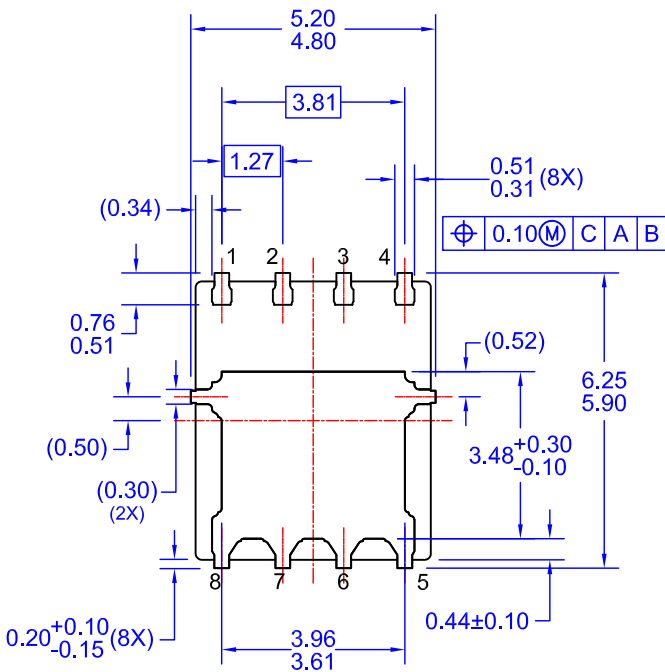
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F. DRAWING FILE NAME: PQFN08AREV10



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