MOSFET - Power, N-Channel, SUPERFET® III, FAST

650 V, 95 mΩ, 30 A

NTHL095N65S3H

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET FAST series helps minimize various power systems and improve system efficiency.

Features

- 700 V @ $T_J = 150$ °C
- Typ. $R_{DS(on)} = 77 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. Q_g = 58 nC)
- Low Effective Output Capacitance (Typ. Coss(eff.) = 522 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

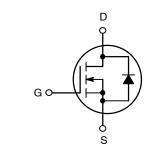
- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar

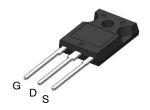


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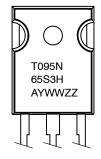
V _{DSS}	R _{DS(ON)} MAX	I _D MAX
650 V	95 mΩ @ 10 V	30 A





TO-247 Long Leads CASE 340CX

MARKING DIAGRAM



T095N65S3H

= Specific Device Code

A YWW = Assembly Plant Code= Data Code (Year & Week)

ZZ

= Lot

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$, Unless otherwise noted)

Symbol	Parameter	Value	Unit	
V_{DSS}	Drain to Source Voltage	ce Voltage		V
V_{GSS}	Gate to Source Voltage	Source Voltage – DC		V
		- AC (f > 1 Hz)	±30	
I _D	Drain Current	- Continuous (T _C = 25°C)		Α
		- Continuous (T _C = 100°C)	18	
I _{DM}	Drain Current	Current – Pulsed (Note 1)		Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	284	mJ	
I _{AS}	Avalanche Current (Note 2)		5.5	А
E _{AR}	Repetitive Avalanche Energy (Note 1)		2.08	mJ
dv/dt	MOSFET dv/dt Peak Diode Recovery dv/dt (Note 3)		120	V/ns
			20	
P_{D}	Power Dissipation	(T _C = 25°C)	208	W
		- Derate Above 25°C	1.67	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
TL	Maximum Lead Temperature for Soldering, 1/8"	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse–width limited by maximum junction temperature.

2. $I_{AS} = 5.5 \text{ A}$, $R_{G} = 25 \Omega$, starting $T_{J} = 25^{\circ}\text{C}$.

3. $I_{SD} \le 15 \text{ A}$, $di/dt \le 200 \text{ A/µs}$, $V_{DD} \le 400 \text{ V}$, starting $T_{J} = 25^{\circ}\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{ heta JC}$	Thermal Resistance, Junction to Case, Max.	0.60	°C/W
$R_{ heta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

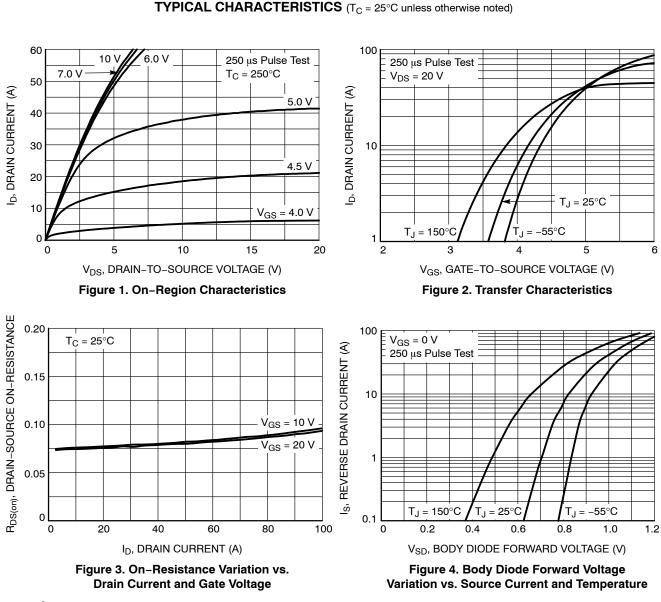
Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NTHL095N65S3H	T095N65S3H	TO-247 (Pb-Free / Halogen Free)	Tube	N/A	N/A	30 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARACT	ERISTICS					
BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V, } I_D = 1 \text{ mA, } T_J = 25^{\circ}\text{C}$		_	-	V
		$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}, T_J = 150^{\circ}\text{C}$	700	-	-	V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.63	_	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	-	-	1	μΑ
		V _{DS} = 520 V, T _C = 125°C	_	1.8	-	
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	_	-	±100	nA
N CHARACTE	RISTICS		-		•	•
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 2.8 \text{ mA}$	2.4	_	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 15 A	_	77	95	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 15 A	-	30	-	S
OYNAMIC CHA	RACTERISTICS		I			
C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 250 kHz	-	2833	_	pF
C _{oss}	Output Capacitance		_	43	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	_	522	-	pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	_	75	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 400 V, I _D = 15 A, V _{GS} = 10 V	-	58	-	nC
Q _{gs}	Gate to Source Gate Charge	(Note 4)	_	14	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		_	15	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	_	1.2	-	Ω
WITCHING CH	IARACTERISTICS		1	•	•	
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400 \text{ V}, I_D = 15 \text{ A},$	_	24	-	ns
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, R_g = 4.7 \Omega$ (Note 4)	_	7.4	-	ns
t _{d(off)}	Turn-Off Delay Time	,	_	69	-	ns
t _f	Turn-Off Fall Time		_	2.4	-	ns
OURCE-DRAII	N DIODE CHARACTERISTICS					
I _S	Maximum Continuous Source to Drain Diode Forward Current		-	_	30	Α
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current		_	-	84	Α
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 15 A	-	-	1.2	٧
t _{rr}	Reverse Recovery Time	V _{DD} = 400 V, I _{SD} = 15 A,	-	367	-	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/μs	_	6.3	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.



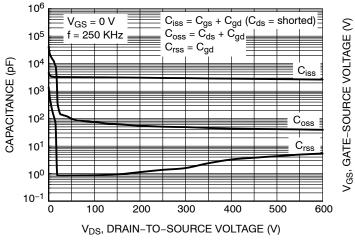


Figure 5. Capacitance Characteristics

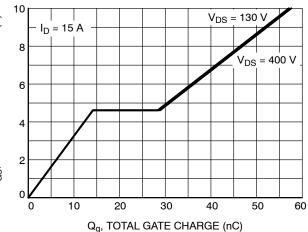


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

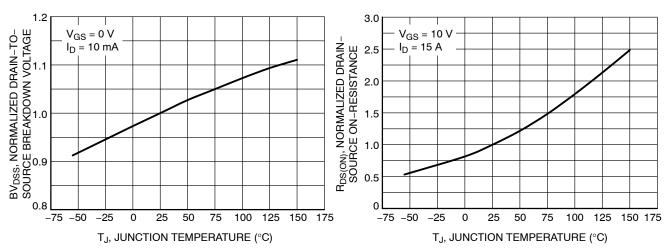


Figure 7. Breakdown Voltage Variation vs. Temperature

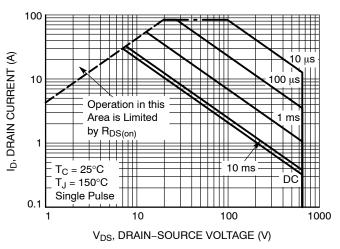


Figure 9. Maximum Safe Operating Area

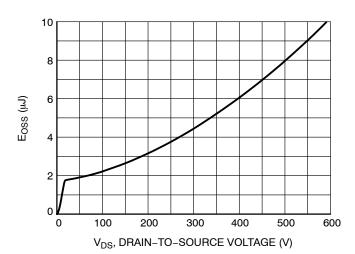


Figure 11. E_{OSS} vs. Drain to Source Voltage



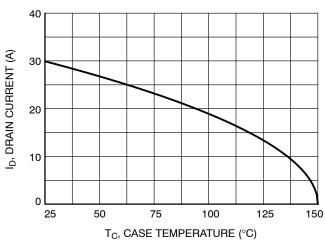


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

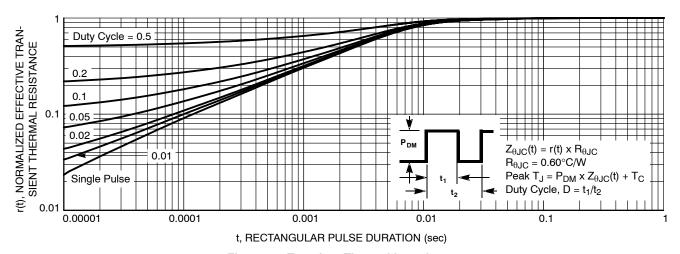


Figure 12. Transient Thermal Impedance

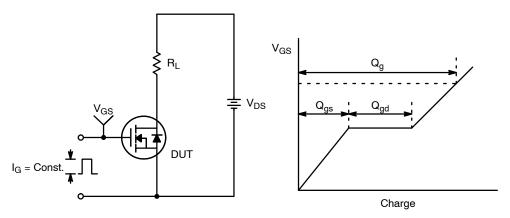


Figure 13. Gate Charge Test Circuit & Waveform

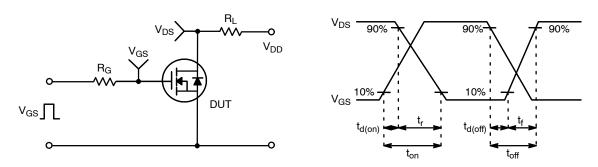


Figure 14. Resistive Switching Test Circuit & Waveforms

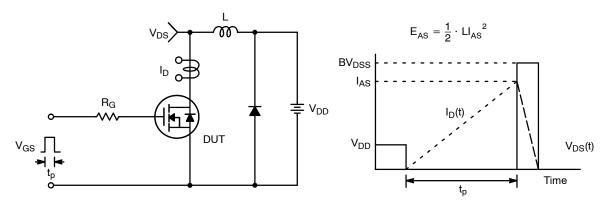


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

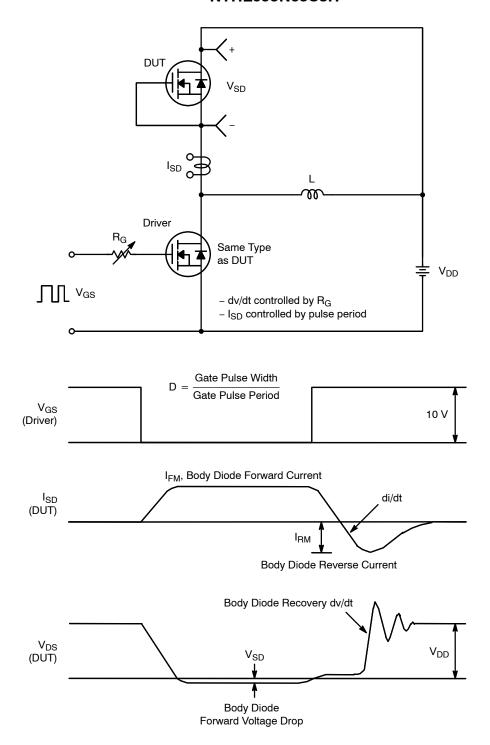
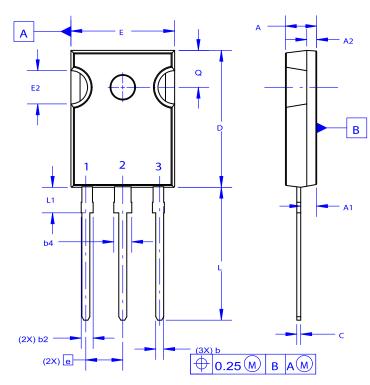


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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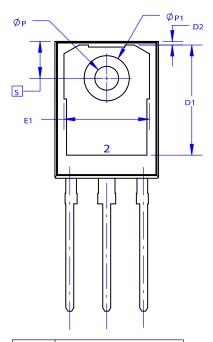
PACKAGE DIMENSIONS

TO-247-3LD CASE 340CX **ISSUE A**



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.



DIM	MILLIMETERS					
DIM	MIN	NOM	MAX			
Α	4.58	4.70	4.82			
A 1	2.20	2.40	2.60			
A2	1.40	1.50	1.60			
D	20.32	20.57	20.82			
Е	15.37	15.62	15.87			
E2	4.96	5.08	5.20			
е	~	5.56	~			
L	19.75	20.00	20.25			
L1	3.69	3.81	3.93			
ØΡ	3.51	3.58	3.65			
Q	5.34	5.46	5.58			
S	5.34	5.46	5.58			
b	1.17	1.26	1.35			
b2	1.53	1.65	1.77			
b4	2.42	2.54	2.66			
С	0.51	0.61	0.71			
D1	13.08	?	~			
D2	0.51	0.93	1.35			
E1	12.81	~	~			
ØP1	6.60	6.80	7.00			

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