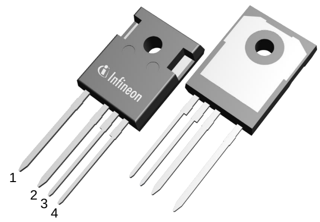
CoolSiC™ 1200 V SiC Trench MOSFET : Silicon Carbide MOSFET with .XT interconnection technology



Lead-Free
Green
Halogen-Free
RoHS

Features

- V_{DSS} = 1200 V at T_{vj} = 25°C
- I_{DCC} = 225 A at T_{vj} = 25°C
- $R_{DS(on)}$ = 7 mΩ at V_{GS} = 18 V, T_{vj} = 25°C
- Very low switching losses
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.2 V
- Robust against parasitic turn on, 0 V turn-off gate voltage can be applied
- Robust body diode for hard commutation
- .XT interconnection technology for best-in-class thermal performance

Potential applications

- General purpose drives (GPD)
- EV-Charging
- Online UPS/Industrial UP
- String inverters
- Solar power optimizer

Product validation

- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

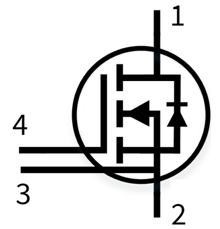
1 – drain

2 – source

3 – Kelvin sense contact

4 – gate

Note: the source and sense pins are not exchangeable, their exchange might lead to malfunction (only for 4pin, TO263-7L)



Type	Package	Marking
IMZA120R007M1H	PG-TO247-4-STD-T3.7	12M1H007

Table of contents

1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature		wave soldering 1.6 mm (0.063 in.) from case for 10 s			260	°C
Mounting torque	M	M3 screw Maximum of mounting process: 3			0.6	Nm
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 18$ V	$T_c = 25$ °C	225	A
			$T_c = 100$ °C	168	
Peak drain current, t_p limited by $T_{vj(max)}$	I_{DM}	$V_{GS} = 18$ V		504	A
Gate-source voltage, max. transient voltage[1)]	V_{GS}	$t_p \leq 0.5$ µs, D<0.01		-10/23	V
Gate-source voltage, max. static voltage	V_{GS}			-5/20	V
Avalanche energy, single pulse	E_{AS}	$I_D = 35$ A, $V_{DD} = 50$ V, $L = 1$ mH		638	mJ
Avalanche energy, repetitive	E_{AR}	$I_D = 35$ A, $V_{DD} = 50$ V, $L = 5.2$ µH		3.2	mJ
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25$ °C	750	W
			$T_c = 100$ °C	375	

1) Important note: The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note AN2018-09 must be considered to ensure sound operation of the device over the planned lifetime.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		15...18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-5...0	V

Table 4 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 108 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 18 V		7	9.9	mΩ
			T_{vj} = 100 °C, $V_{GS(on)}$ = 18 V		10		
			T_{vj} = 175 °C, $V_{GS(on)}$ = 18 V		14		
			T_{vj} = 25 °C, $V_{GS(on)}$ = 15 V		8.9	11.1	
Gate-emitter threshold voltage	$V_{GS(th)}$	I_D = 47 mA, $V_{DS} = V_{GS}$ (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.5	4.2	5.2	V
			T_{vj} = 175 °C		3.6		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	T_{vj} = 25 °C			860	µA
			T_{vj} = 175 °C		14.6		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = 23 V			300	nA
			V_{GS} = -10 V			-300	
Forward transconductance	g_{fs}	I_D = 108 A, V_{DS} = 20 V			72.6		S
Internal gate resistance	$R_{G,int}$	f = 1 MHz, V_{AC} = 25 mV			1.8		Ω
Input capacitance	C_{iss}	V_{DD} = 25 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			9170		nF
Output capacitance	C_{oss}	V_{DD} = 25 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			420		pF
Reverse transfer capacitance	C_{rss}	V_{DD} = 25 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			61		pF
C_{oss} stored energy	E_{oss}	V_{DD} = 25 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			172		µJ
Total gate charge	Q_G	V_{DD} = 800 V, I_D = 108 A, V_{GS} = -2/18 V, turn-on pulse			220		nC
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 800 V, I_D = 108 A, V_{GS} = -2/18 V, turn-on pulse			72		nC
Gate-to-drain charge	Q_{GD}	V_{DD} = 800 V, I_D = 108 A, V_{GS} = -2/18 V, turn-on pulse			64		nC
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 108 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, diode: body diode at V_{GS} = 0 V , $L_σ$ = 15 nH	T_{vj} = 25 °C		97		ns
			T_{vj} = 175 °C		92		

(table continues...)

Table 4 (continued) Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Rise time	t_r	V_{DD} = 800 V, I_D = 108 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, diode: body diode at V_{GS} = 0 V, L_σ = 15 nH	T_{vj} = 25 °C		36		ns
			T_{vj} = 175 °C		41		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 108 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, diode: body diode at V_{GS} = 0 V, L_σ = 15 nH	T_{vj} = 25 °C		116		ns
			T_{vj} = 175 °C		121		
Fall time	t_f	V_{DD} = 800 V, I_D = 108 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, diode: body diode at V_{GS} = 0 V, L_σ = 15 nH	T_{vj} = 25 °C		39		ns
			T_{vj} = 175 °C		39		
Turn-on energy	E_{on}	V_{DD} = 800 V, I_D = 108 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, diode: body diode at V_{GS} = 0 V, L_σ = 15 nH	T_{vj} = 25 °C		1360		µJ
			T_{vj} = 175 °C		2040		
Turn-off energy	E_{off}	V_{DD} = 800 V, I_D = 108 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, diode: body diode at V_{GS} = 0 V, L_σ = 15 nH	T_{vj} = 25 °C		410		µJ
			T_{vj} = 175 °C		440		
Total switching energy	E_{tot}	V_{DD} = 800 V, I_D = 108 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, diode: body diode at V_{GS} = 0 V, L_σ = 15 nH	T_{vj} = 25 °C		1926		µJ
			T_{vj} = 175 °C		3110		
MOSFET/body diode thermal resistance, junction to case	$R_{th(j-c)}$				0.15	0.20	K/W
Virtual junction temperature	T_{vj}			-55		175	°C

Note: The chip technology was characterized up to 200 kV/µs. The measured dV/dt was limited by measurement test setup and package.

Dynamic test circuit see Fig. F.

3 Body diode

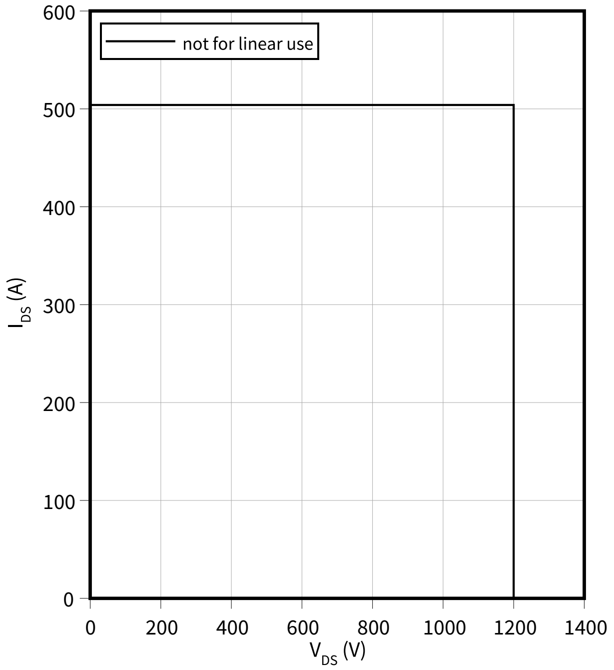
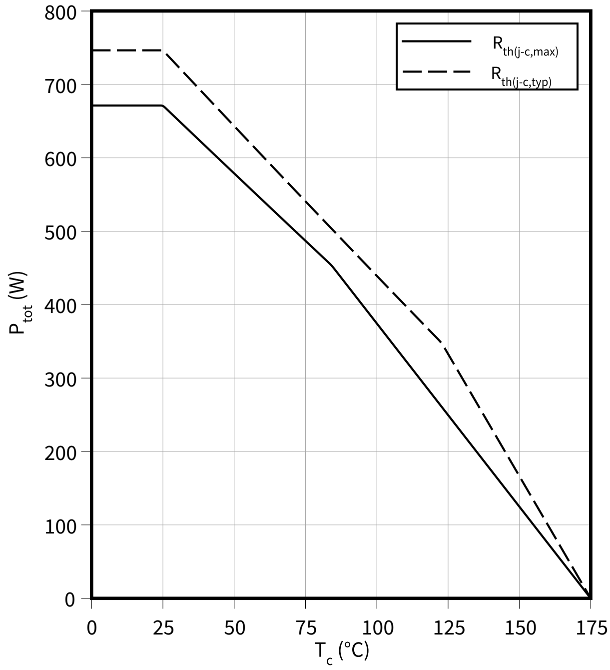
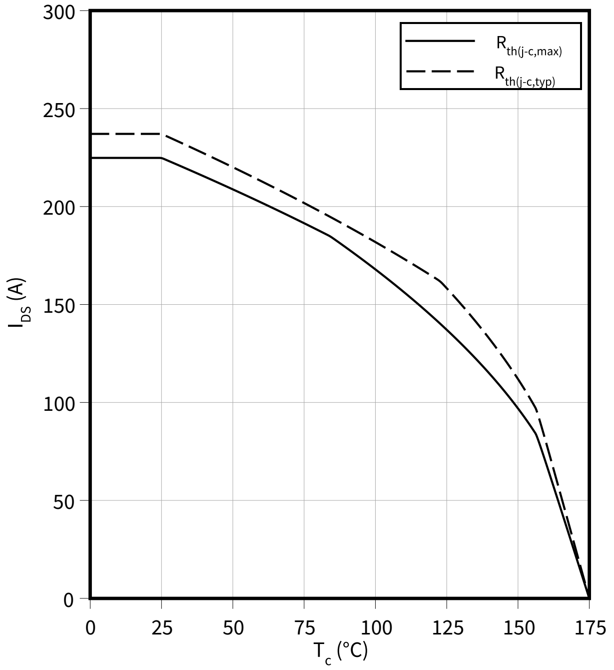
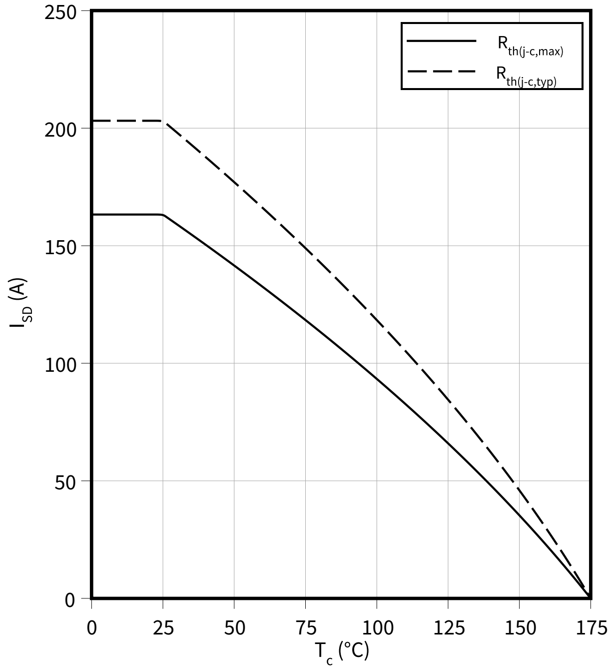
Table 5 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1200	V
Continuous reverse drain current for $R_{th(j\text{-}c,max)}$, limited by $T_{vj(max)}$	I_{SDC}	$V_{GS} = 0$ V	$T_c = 25$ °C	163	A
			$T_c = 100$ °C	93	
Peak reverse drain current, t_p limited by $T_{vj(max)}$	I_{SM}	$V_{GS} = 0$ V		504	A

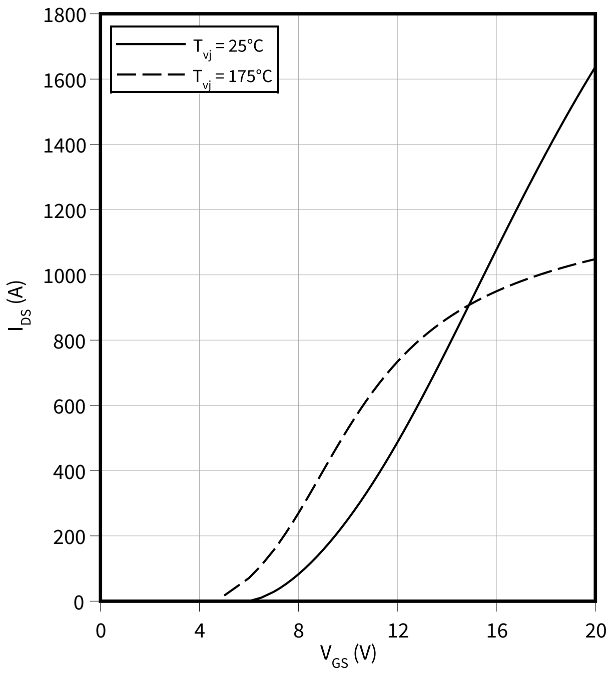
Table 6 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	$I_{SD} = 108$ A, $V_{GS} = 0$ V	$T_{vj} = 25$ °C		3.8	5	V
			$T_{vj} = 100$ °C		3.7		
			$T_{vj} = 175$ °C		3.6		
MOSFET forward recovery charge	Q_{fr}	$V_{DD} = 800$ V, $I_{SD} = 108$ A, $V_{GS} = 0$ V, $di_f/dt = 3000$ A/µs, Q_{fr} includes also Q_C	$T_{vj} = 25$ °C		900		nC
			$T_{vj} = 175$ °C		1651		
MOSFET peak forward recovery current	I_{frm}	$V_{DD} = 800$ V, $I_{SD} = 108$ A, $V_{GS} = 0$ V, $di_f/dt = 3000$ A/µs, Q_{fr} includes also Q_C	$T_{vj} = 25$ °C		5		A
			$T_{vj} = 175$ °C		9		
MOSFET forward recovery energy	E_{fr}	$V_{DD} = 800$ V, $I_{SD} = 108$ A, $V_{GS} = 0$ V, $di_f/dt = 3000$ A/µs, Q_{fr} includes also Q_C	$T_{vj} = 25$ °C		156		µJ
			$T_{vj} = 175$ °C		630		
MOSFET/body diode thermal resistance, junction to case	$R_{th(j\text{-}c)}$				0.15	0.20	K/W
Virtual junction temperature	T_{vj}			-55		175	°C

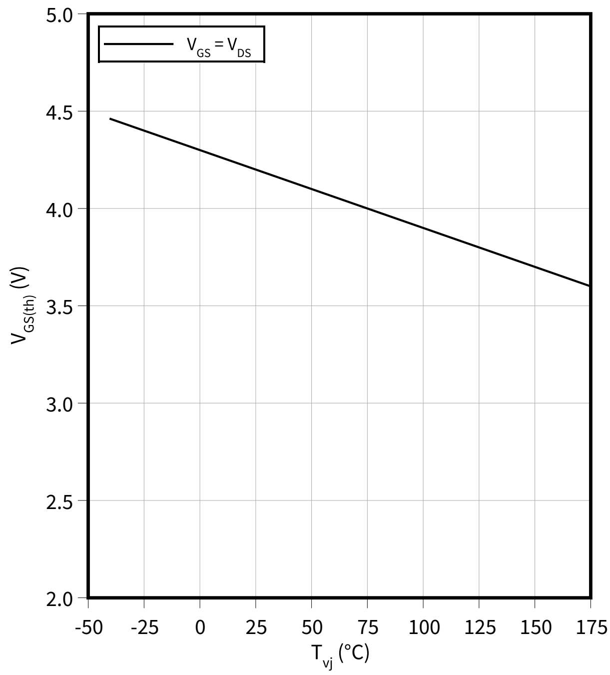
4 Characteristics diagrams

Reverse bias safe operating area (RBSOA), MOSFET $I_{DS} = f(V_{DS})$ $T_{vj} \leq 175$ °C, $V_{GS} = 0/18$ V, $T_c = 25$ °C	**Power dissipation as a function of case temperature limited by bond wire, MOSFET** $P_{tot} = f(T_c)$
	
Maximum DC drain to source current as a function of case temperature limited by bond wire, MOSFET $I_{DS} = f(T_c)$	**Maximum source to drain current as a function of case temperature limited by bond wire, Body diode, MOSFET** $I_{SD} = f(T_c)$ $V_{GS} = 0$ V
	

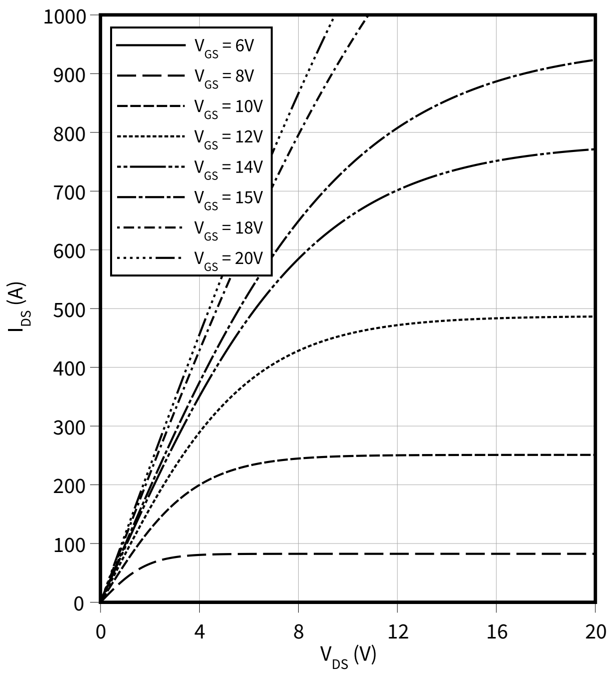
Typical transfer characteristic , MOSFET
$I_{DS} = f(V_{GS})$
$V_{DS} = 20$ V, $t_p = 20$ µs



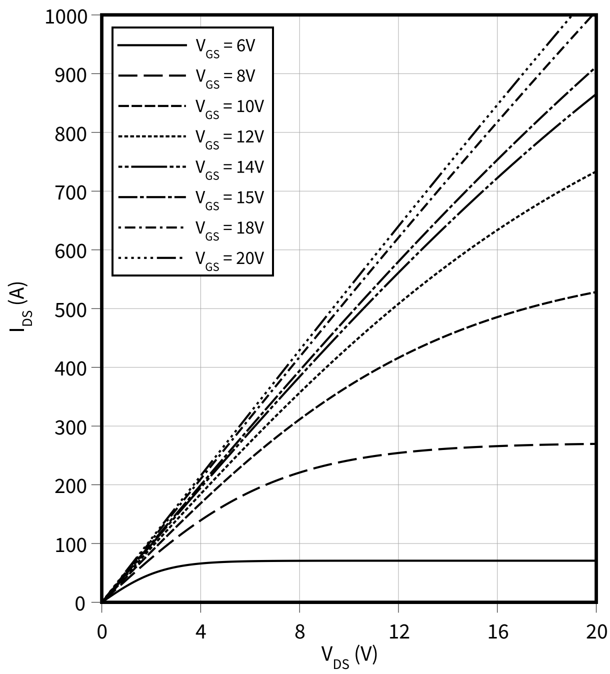
Typical gate-source threshold voltage as a function of junction temperature , MOSFET
$V_{GS(th)} = f(T_{vj})$
$I_D = 47$ mA

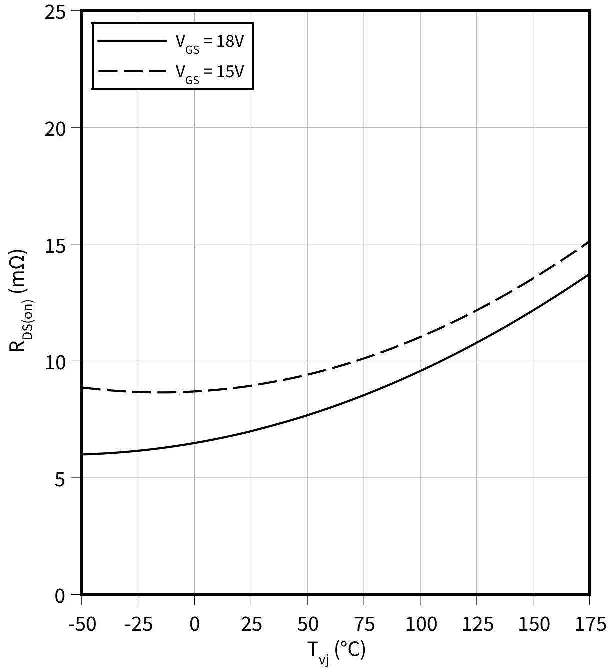
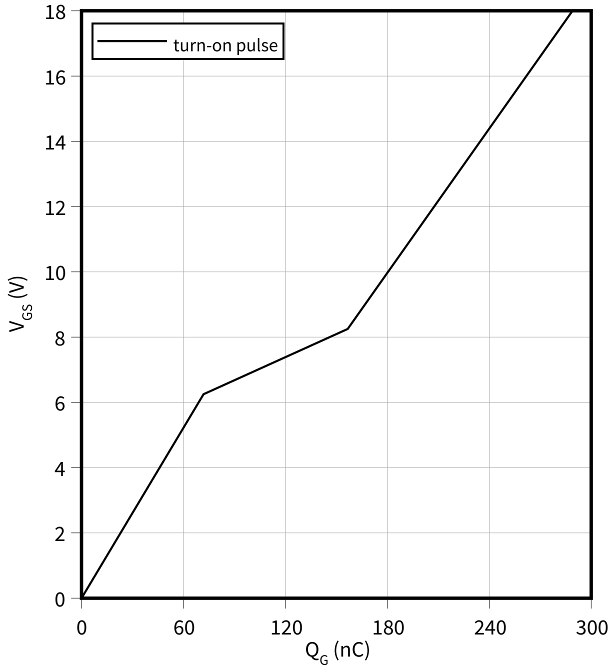
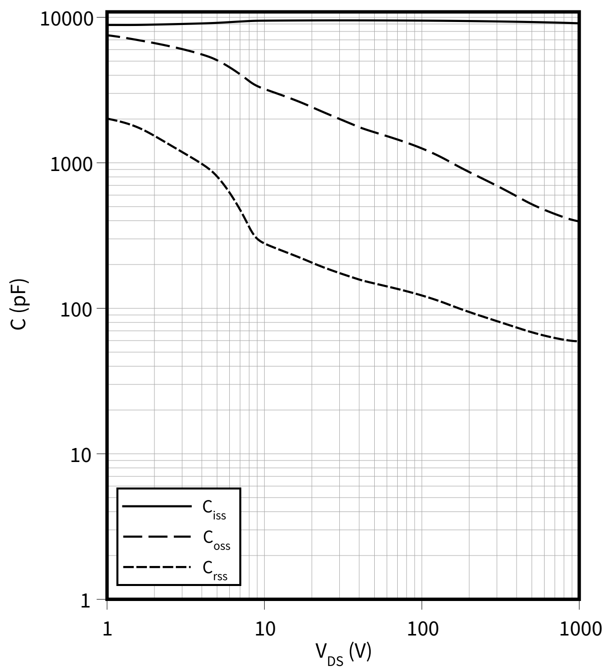
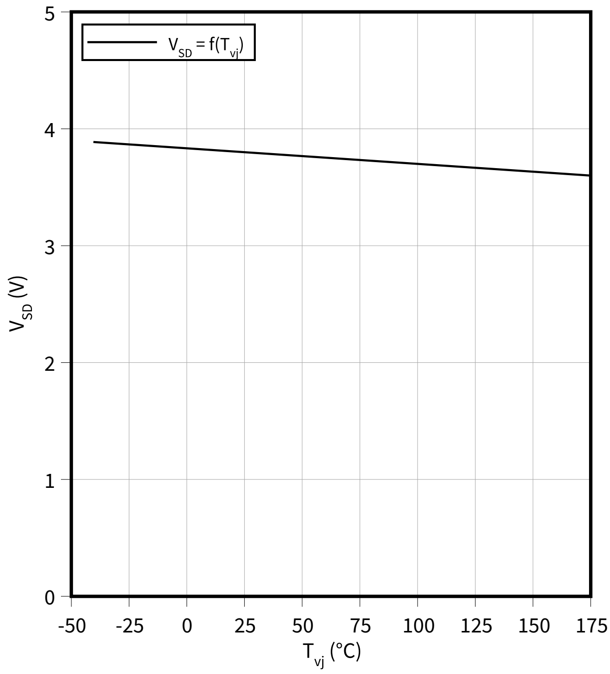


Typical output characteristic, V_{GS} as parameter , MOSFET
$I_{DS} = f(V_{DS})$
$T_{vj} = 25$ °C, $t_p = 20$ µs



Typical output characteristic, V_{GS} as parameter, MOSFET
$I_{DS} = f(V_{DS})$
$T_{vj} = 175$ °C, $t_p = 20$ µs

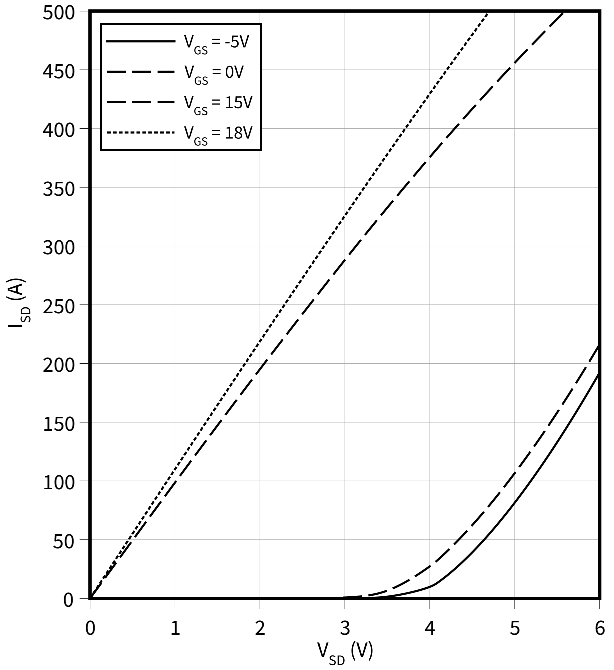


Typical on-state resistance as a function of junction temperature, MOSFET $R_{DS(on)} = f(T_{vj})$ $I_D = 108$ A	**Typical gate charge , MOSFET** $V_{GS} = f(Q_G)$ $I_D = 108$ A, $V_{DS} = 800$ V
	
Typical capacitance as a function of drain-source voltage , MOSFET $C = f(V_{DS})$ f = 100 kHz, $V_{GS} = 0$ V	**Typical reverse drain voltage as function of junction temperature , MOSFET** $V_{SD} = f(T_{vj})$ $I_{SD} = 108$ A, $V_{GS} = 0$ V
	

Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter, MOSFET

$I_{SD} = f(V_{SD})$

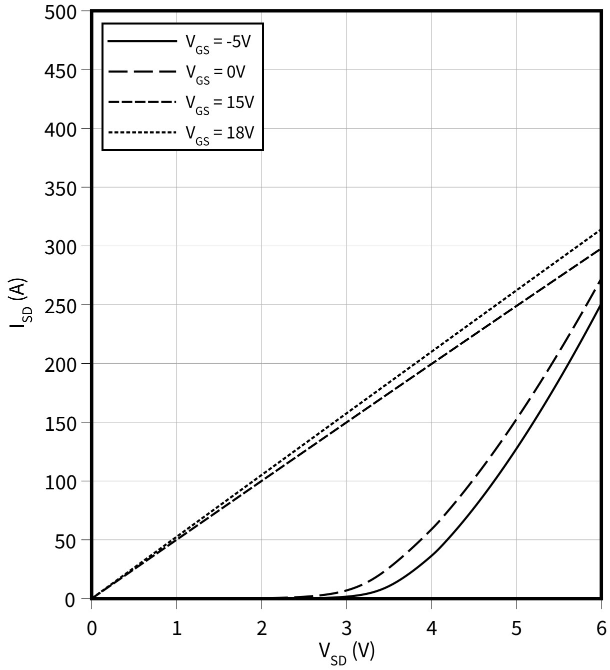
$T_{vj} = 25\ °C$, $t_p = 20\ µs$



Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter, MOSFET

$I_{SD} = f(V_{SD})$

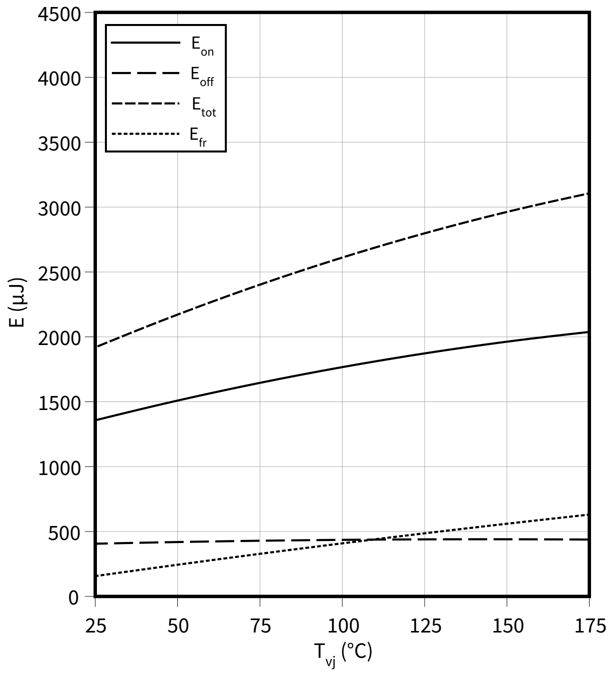
$T_{vj} = 175\ °C$, $t_p = 20\ µs$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V, MOSFET

$E = f(T_{vj})$

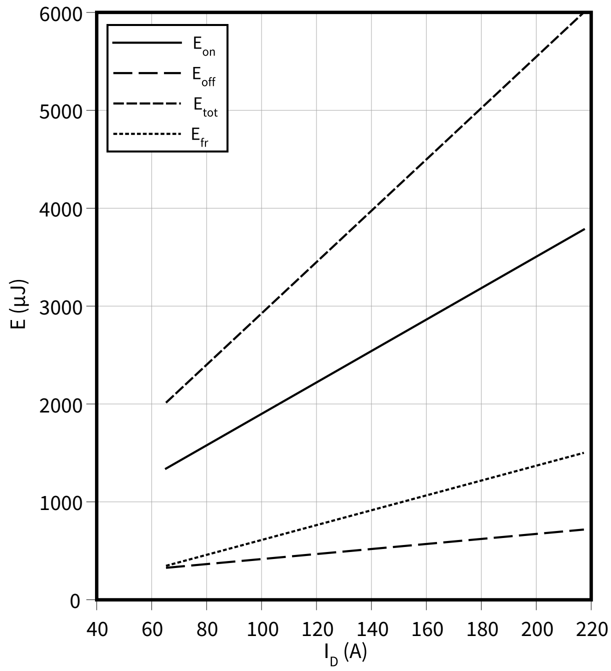
$V_{GS} = 0/18\ V$, $I_D = 108\ A$, $R_{G,ext} = 1\ Ω$, $V_{DD} = 800\ V$



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V, MOSFET

$E = f(I_D)$

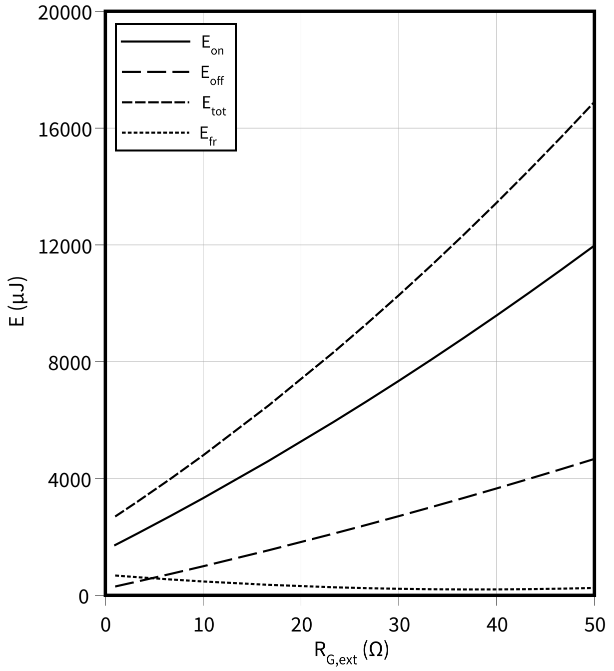
$V_{GS} = 0/18\ V$, $T_{vj} = 175\ °C$, $R_{G,ext} = 1\ Ω$, $V_{DD} = 800\ V$



Typical switching energy losses as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V, MOSFET

$E = f(R_{G,ext})$

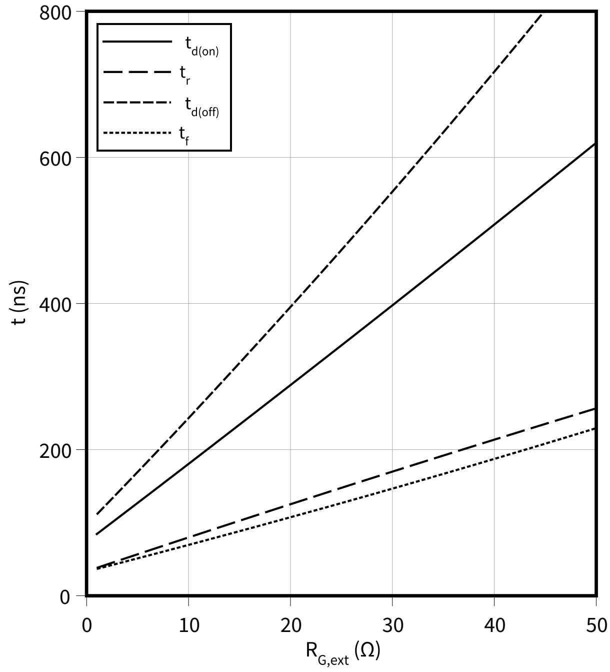
V_{GS} = 0/18 V, I_D = 108 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V, MOSFET

$t = f(R_{G,ext})$

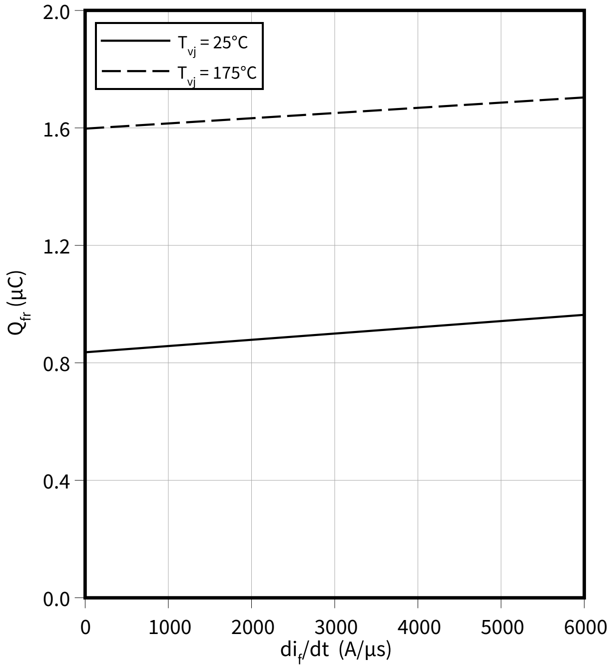
V_{GS} = 0/18 V, I_D = 108 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical reverse recovery charge as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V, MOSFET

$Q_{fr} = f(di_f/dt)$

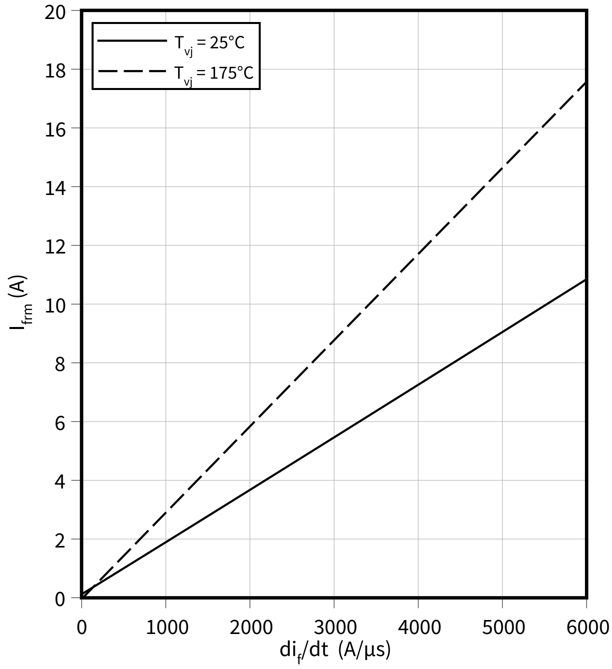
V_{GS} = 0/18 V, I_D = 108 A, V_{DD} = 800 V



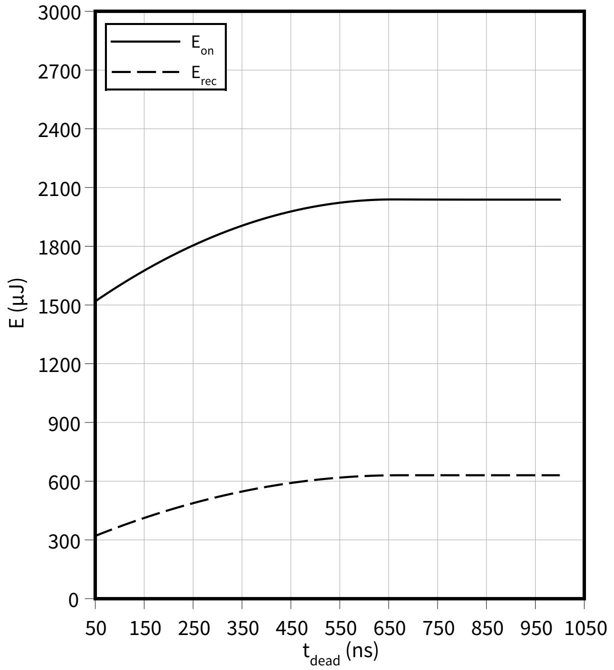
Typical reverse recovery current as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V, MOSFET

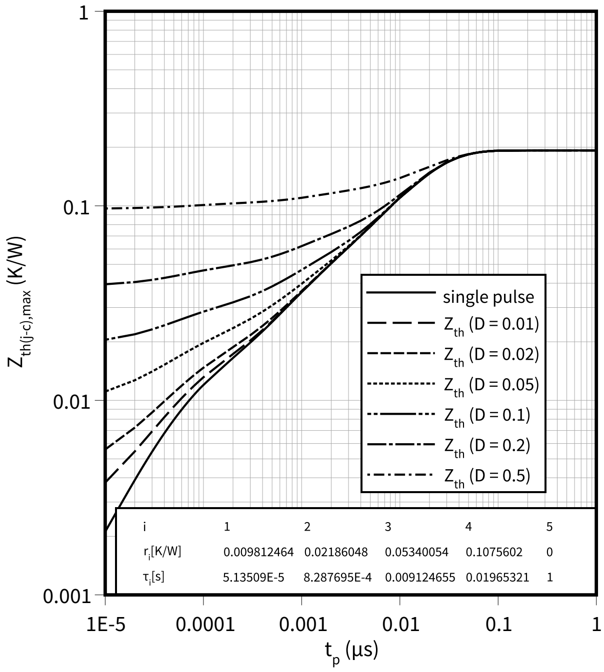
$I_{frm} = f(di_f/dt)$

V_{GS} = 0/18 V, I_D = 108 A, V_{DD} = 800 V



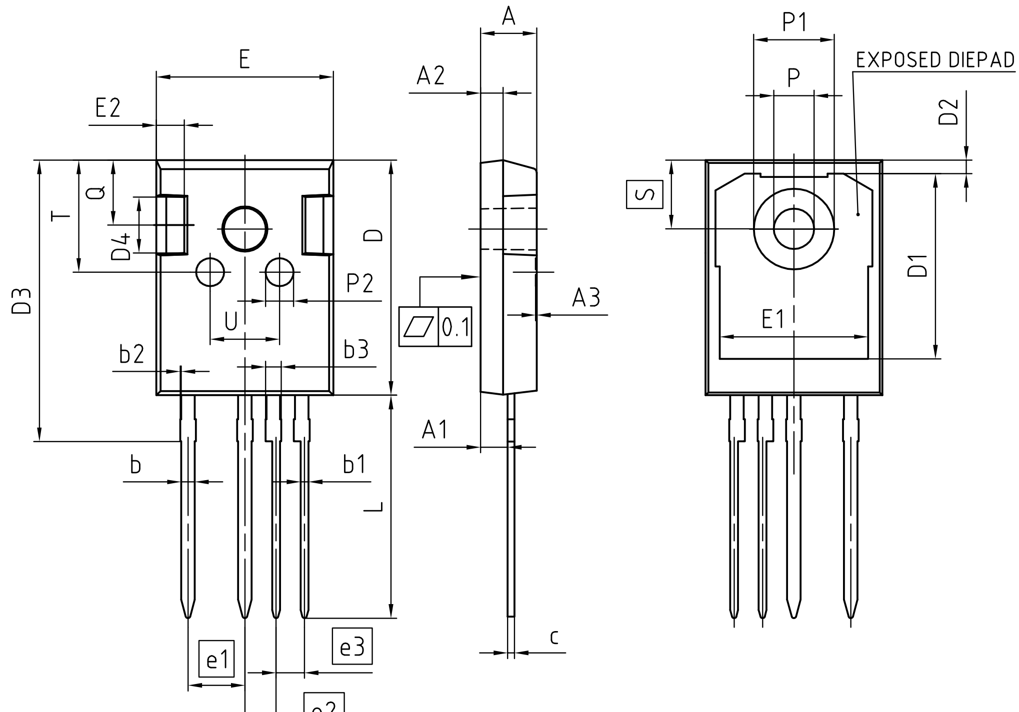
Typical switching energy losses as a function of dead time / blanking time, test circuit in Fig. F, 2nd device own bodydiode: V_{GS} = -5 V, MOSFET	**Max. transient thermal impedance (MOSFET/diode) , MOSFET**
$E = f(t_{dead})$ V_{GS} = -5/18 V, I_D = 108 A, T_{vj} = 175 °C, V_{DD} = 800 V	$Z_{th(j-c),max} = f(t_p)$ $D = t_p/T$

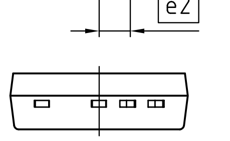




5 Package outlines

PG-TO247-4-STD-T3.7





NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

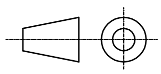
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.90	5.10
A1	2.31	2.51
A2	1.90	2.10
A3	0.05	0.25
b	1.10	1.30
b1	0.65	0.79
b2	-	0.20
b3	1.34	1.44
c	0.58	0.66
D	20.90	21.10
D1	16.25	16.85
D2	1.05	1.35
D3	24.97	25.27
D4	4.90	5.10
E	15.70	15.90
E1	13.10	13.50
E2	2.40	2.60
e1	5.08	
e2	2.79	
e3	2.54	
L	19.80	20.10
L1	-	4.30
øP	3.50	3.70
øP1	7.00	7.40
øP2	2.40	2.60
Q	5.60	6.00
S	6.15	
T	9.80	10.20
U	6.00	6.40

DOCUMENT NO.
Z8B00184785

REVISION
03

SCALE 2:1

EUROPEAN PROJECTION



ISSUE DATE
21.08.2017

Figure 1

6 Testing conditions

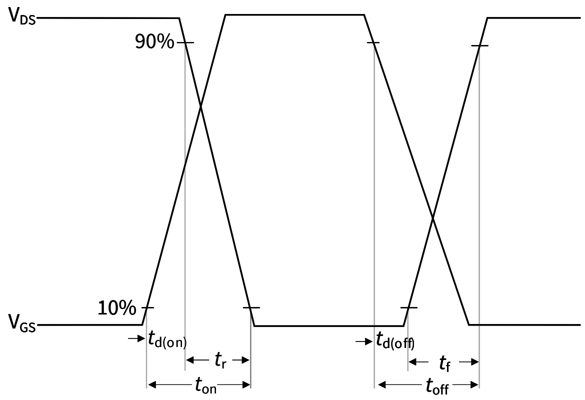


Figure A. **Definition of switching times**

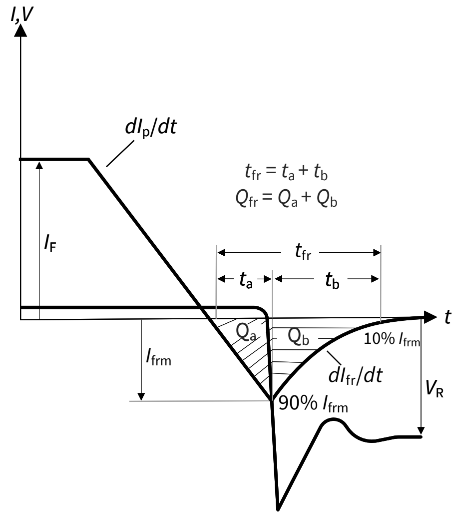


Figure B. **Definition of diode switching characteristics**

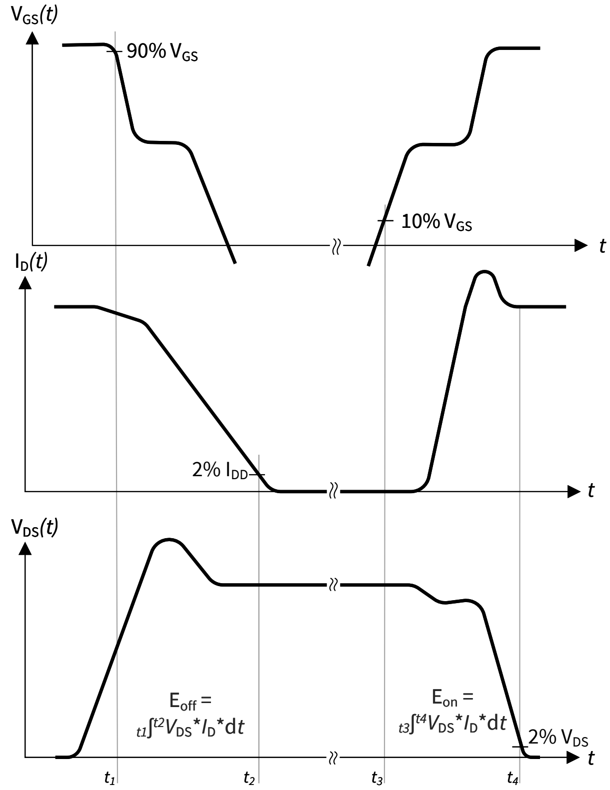


Figure C. **Definition of switching losses**

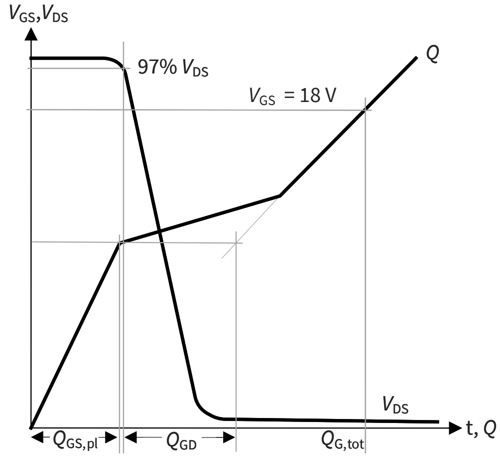


Figure D. **Definition of QGD**

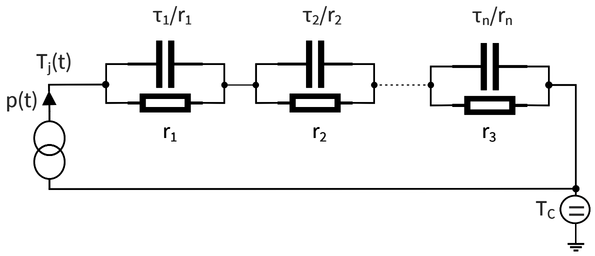


Figure E. **Thermal equivalent circuit**

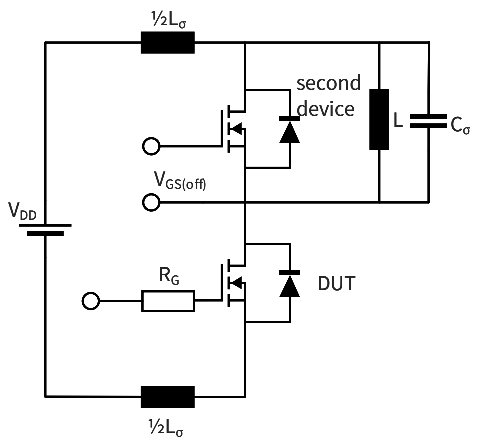


Figure F. **Dynamic test circuit**
Parasitic inductance L_{σ},
Parasitic capacitor C_{σ},

Figure 2

Revision history

Document revision	Date of release	Description of changes
1.00	2022-01-31	Final datasheet

Edition 2022-01-31

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-ABB961-001