NXS0108-Q100

Dual supply translating transceiver; open drain; auto direction sensing

Rev. 1 — 15 September 2020 Product data sheet

1. General description

The NXS0108-Q100 is an 8-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 8-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.2 V and 3.6 V and $V_{CC(B)}$ can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.2 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range:
  - $V_{CC(A)}$: 1.2 V to 3.6 V and $V_{CC(B)}$: 1.65 V to 5.5 V
- Maximum data rates:
  - Push-pull: 110 Mbps
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - HBM JESD22-A114E Class 2 exceeds 2.5 kV for A port
  - HBM JESD22-A114E Class 3B exceeds 15 kV for B port
  - CDM JESD22-C101E exceeds 1.5 kV
  - IEC61000-4-2 contact discharge exceeds 8 kV for B port
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NXS0108PW-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
NXS0108BQ-Q100	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

nexperia

4. Functional diagram

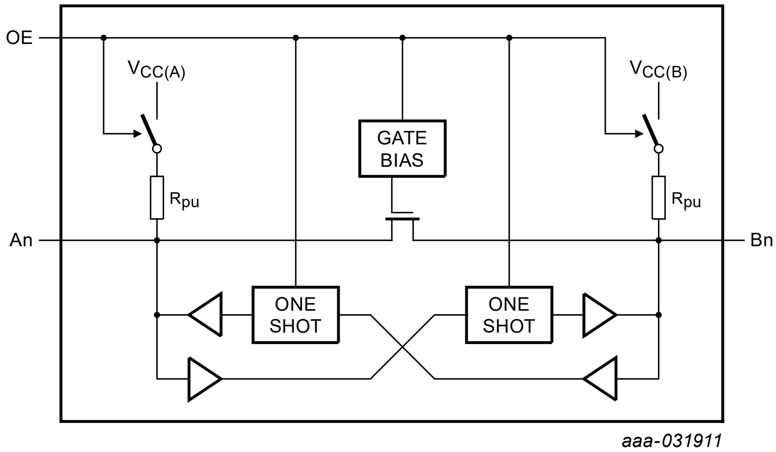


Fig. 1. Functional diagram (one channel)

5. Pinning information

5.1. Pinning

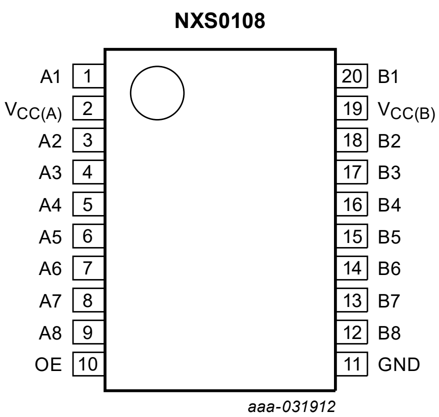
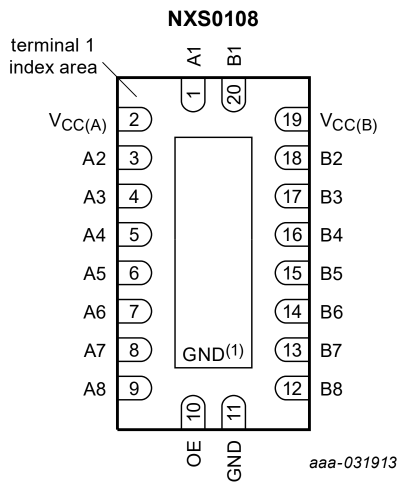


Fig. 2. Pin configuration SOT360-1 (TSSOP20)



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 3. Pin configuration SOT764-1 (DHVQFN20)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A1, A2, A3, A4, A5, A6, A7, A8	1, 3, 4, 5, 6, 7, 8, 9	data input or output (referenced to $V_{CC(A)}$)
$V_{CC(A)}$	2	supply voltage A
OE	10	output enable input (active HIGH; referenced to $V_{CC(A)}$)
GND	11	ground (0 V)
B1, B2, B3, B4, B5, B6, B7, B8	20, 18, 17, 16, 15, 14, 13, 12	data input or output (referenced to $V_{CC(B)}$)
$V_{CC(B)}$	19	supply voltage B

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage		Input	Input/output	
$V_{CC(A)}$ [1]	**$V_{CC(B)}$**	**OE**	**A**	**B**
1.2 V to 3.6 V	1.65 V to 5.5 V	L	Z	Z
1.2 V to 3.6 V	1.65 V to 5.5 V	H	input or output	output or input
GND	1.65 V to 5.5 V	X	Z	Z
1.2 V to 3.6 V	GND	X	Z	Z

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B			-0.5	+6.5	V
V_I	input voltage	OE	[1]	-0.5	+6.5	V
		An, Bn; Power-down or 3-state mode	[1]	-0.5	+6.5	V
		An, Bn; Active mode	[1] [2] [3]	-0.5	V_{CCI} + 0.5	V
V_O	output voltage	An, Bn; Power-down or 3-state mode	[1]	-0.5	+6.5	V
		An, Bn; Active mode	[1] [3] [4]	-0.5	V_{CCO} + 0.5	V

Symbol	Parameter	Conditions	Min	Max	Unit
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	$V_O = 0$ V to V_{CCO} [4]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [5]	-	500	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCI} is the supply voltage associated with the input.
[3] V_{CCI} + 0.5 V or V_{CCO} + 0.5 V should not exceed 6.5 V.
[4] V_{CCO} is the supply voltage associated with the output.
[5] For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions [1] [2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.2	3.6	V
$V_{CC(B)}$	supply voltage B		1.65	5.5	V
V_I	input voltage	OE	0	5.5	V
		Power-down or 3-state mode			
		An	0	3.6	V
		Bn	0	5.5	V
		Active mode			
		An, Bn [3]	0	V_{CCI}	V
V_O	output voltage	Power-down or 3-state mode			
		An	0	3.6	V
		Bn	0	5.5	V
		Active mode			
		An, Bn [4]	0	V_{CCO}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving			
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	10	ns/V
		OE input			
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.
[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.
[3] V_{CCI} is the supply voltage associated with the input.
[4] V_{CCO} is the supply voltage associated with the output.

9. Static characteristics

Table 6. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	A port; $V_I \leq 0.15$ V; $V_{CC(B)}$ = 1.65 V to 5.5 V; $V_{CC(A)}$ = 1.2 V; I_O = -135 μA		-	0.25	-	V
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	-	±1	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	[2]	-	-	±1	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V		-	-	±1	μA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V		-	-	±1	μA
C_I	input capacitance	OE input; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V		-	2.6	-	pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V					
		enabled		-	9	-	pF
		disabled		-	5.2	-	pF
		B port; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V					
		enabled		-	10.5	-	pF
		disabled		-	9	-	pF

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.
[2] V_{CCO} is the supply voltage associated with the output.

Table 7. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.8 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.2 V	0.1	0.3	0.1	0.9	0.1	1.9	0.1	5.6	μA
1.5 V	0.1	0.1	0.1	0.7	0.1	1.7	0.1	5	μA
1.8 V	0.1	0.1	0.1	0.5	0.1	1.5	0.1	4.6	μA
2.5 V	-	-	0.1	0.1	0.1	0.8	0.1	3.8	μA
3.3 V	-	-	-	-	0.1	0.1	0.1	2.8	μA

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A port					
		$V_{CC(A)}$ = 1.2 V to 1.95 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$V_{CC(A)}$ - 0.2	-	$V_{CC(A)}$ - 0.2	-	V
		$V_{CC(A)}$ = 1.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$V_{CC(A)}$ - 0.4	-	$V_{CC(A)}$ - 0.4	-	V
		B port					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$V_{CC(B)}$ - 0.4	-	$V_{CC(B)}$ - 0.4	-	V
		OE input					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
V_{IL}	LOW-level input voltage	A or B port					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	0.15	-	0.15	V
		OE input					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	A port; I_O = -20 μA; $V_I \geq V_{CC(B)}$ - 0.4 V					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$0.67V_{CC(A)}$	-	$0.67V_{CC(A)}$	-	V
		B port; I_O = -20 μA; $V_I \geq V_{CC(A)}$ - 0.2 V					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	$0.67V_{CC(B)}$	-	$0.67V_{CC(B)}$	-	V
V_{OL}	LOW-level output voltage	A port; $V_I \leq$ 0.15 V; $V_{CC(B)}$ = 1.65 V to 5.5 V					
		$V_{CC(A)}$ = 1.4 V; I_O = -180 μA	-	0.4	-	0.4	V
		$V_{CC(A)}$ = 1.65 V; I_O = -220 μA	-	0.4	-	0.4	V
		$V_{CC(A)}$ = 2.3 V; I_O = -300 μA	-	0.4	-	0.4	V
		$V_{CC(A)}$ = 3.0 V; I_O = -400 μA	-	0.55	-	0.55	V
		B port; $V_I \leq$ 0.15 V; $V_{CC(A)}$ = 1.2 V to 3.6 V					
		$V_{CC(B)}$ = 1.65 V; I_O = -220 μA	-	0.4	-	0.4	V
		$V_{CC(B)}$ = 2.3 V; I_O = -300 μA	-	0.4	-	0.4	V
		$V_{CC(B)}$ = 3.0 V; I_O = -400 μA	-	0.55	-	055	V
		$V_{CC(B)}$ = 4.5 V; I_O = -620 μA	-	0.55	-	055	V
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	±2	-	±12	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V [2]	-	±2	-	±12	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V	-	±2	-	±12	μA
		B port; V_I or V_O = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 5.5 V	-	±2	-	±12	μA

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_{CC}	supply current	OE = 0 V or $V_{CC(A)}$; An, Bn open					
		$I_{CC(A)}$					
		$V_{CC(A)}$ = 1.2 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-5	0.5	-5	1	μA
		$V_{CC(A)}$ = 1.5 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-2	1.2	-2	2	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-	1.0	-	2	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	-1	-	-1	-	μA
		$I_{CC(B)}$					
		$V_{CC(A)}$ = 1.2 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	22	-	60	μA
		$V_{CC(A)}$ = 1.5 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	20	-	20	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-1	-	-1	-	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	-	2	-	12	μA
		$I_{CC(A)} + I_{CC(B)}$					
		$V_{CC(A)}$ = 1.2 ; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	17	-	65	μA
		$V_{CC(A)}$ = 1.5 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	-	20	-	20	μA

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.
[2] V_{CCO} is the supply voltage associated with the output.

10. Dynamic characteristics

Table 9. Typical dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 4 and Fig. 6.

Symbol	Parameter	Conditions		$V_{CC(B)}$				Unit
				1.8 V ± 0.15 V	2.5 V ± 0.2 V	3.3 V ± 0.3 V	5.0 V ± 0.5 V	
$V_{CC(A)}$ = 1.2 V; T_{amb} = 25 °C								
t_{PHL}	HIGH to LOW propagation delay	A to B		6.5	5.9	5.7	5.5	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		7.1	6.3	6.2	6.6	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		6.2	5.4	5.1	5	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		5.6	4.1	3.6	3.2	ns
t_{en}	enable time	OE to A; B	[1]	200	200	200	200	ns
t_{dis}	disable time	OE to A; no external load	[1] [2]	12	12	12	12	ns
		OE to B; no external load	[2]	12	12	12	12	ns
		OE to A; see Fig. 5		90	90	90	90	ns
		OE to B; see Fig. 5		95	75	100	75	ns
t_{TLH}	LOW to HIGH output transition time	A port		6.5	5.2	4.8	4.4	ns
		B port		6.6	4.3	2.1	1.5	ns
t_{THL}	HIGH to LOW output transition time	A port		5.8	4.8	4.3	3.8	ns
		B port		3.6	2.2	1.8	1.5	ns
$t_{sk(o)}$	output skew time	between channels	[3]	1	1	1	1	ns
t_W	pulse width	data inputs		20	16.7	16.7	16.7	ns
f_{data}	data rate			50	60	60	60	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] These values are guaranteed by design.
[3] Skew between any two outputs of the same package switching in the same direction.

Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 4 and Fig. 6.

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	-	11	-	9.2	-	8.6	-	8.6	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	12.6	-	10	-	9.8	-	9.7	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	12.7	-	11.1	-	11	-	12	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	10.5	-	6.9	-	5.6	-	4.6	ns
t_{en}	enable time	OE to A; B [1]	-	200	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [1] [2]	-	17	-	17	-	17	-	17	ns
		OE to B; no external load [2]	-	18	-	17	-	17	-	17	ns
		OE to A; see Fig. 5	-	120	-	120	-	120	-	125	ns
		OE to B; see Fig. 5	-	170	-	125	-	175	-	125	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.6	13.1	2.8	9.8	2.0	9.0	2.0	8.3	ns
		B port	2.9	11.4	1.9	8.1	0.9	5.3	0.7	3	ns
t_{THL}	HIGH to LOW output transition time	A port	2.1	9.9	1.5	7.7	1.2	6.8	0.8	6.0	ns
		B port	1.5	8.7	1.0	5.5	0.9	3.8	0.8	3.1	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	1	-	1	-	1.1	-	1	ns
t_W	pulse width	data inputs	20	-	20	-	20	-	20	-	ns
f_{data}	data rate		-	50	-	50	-	50	-	50	Mbps
$V_{CC(A)}$ = 1.8 V ± 0.15 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	-	9.7	-	7.3	-	6.5	-	5.9	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	11.3	-	8.4	-	7.4	-	6.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	9.8	-	8.0	-	7.4	-	7.0	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	10.2	-	7.0	-	5.8	-	5.0	ns
t_{en}	enable time	OE to A; B [1]	-	200	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [1] [2]	-	13	-	13	-	13	-	13	ns
		OE to B; no external load [2]	-	16	-	13	-	13	-	13	ns
		OE to A; see Fig. 5	-	140	-	140	-	140	-	145	ns
		OE to B; see Fig. 5	-	165	-	125	-	175	-	125	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.2	11.9	2.0	8.6	1.9	7.8	1.9	7.2	ns
		B port	2.8	12.2	1.8	7.7	1.2	5.3	0.7	2.9	ns
t_{THL}	HIGH to LOW output transition time	A port	1.8	8.8	1.3	6.6	0.9	5.7	0.6	4.9	ns
		B port	1.3	8.3	1.0	5.4	0.9	3.9	0.7	3.0	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	1	-	1	-	1	-	1	ns
t_W	pulse width	data inputs	22.2	-	16.7	-	16.7	-	16.7	-	ns
f_{data}	data rate		-	45	-	60	-	60	-	60	Mbps

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 2.5 V ± 0.2 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	-	-	-	6.2	-	5.3	-	4.7	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	-	-	6.8	-	5.9	-	5.2	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	-	-	5.9	-	4.8	-	4.2	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	-	-	6.2	-	4.6	-	3.6	ns
t_{en}	enable time	OE to A; B [1]	-	-	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [1] [2]	-	-	-	9	-	9	-	9	ns
		OE to B; no external load [2]	-	-	-	11	-	9	-	9	ns
		OE to A; see Fig. 5	-	-	-	105	-	105	-	105	ns
		OE to B; see Fig. 5	-	-	-	125	-	175	-	120	ns
t_{TLH}	LOW to HIGH output transition time	A port	-	-	1.7	7.3	1.7	6.4	1.8	5.8	ns
		B port	-	-	1.8	7.3	1.3	5.4	0.8	3.3	ns
t_{THL}	HIGH to LOW output transition time	A port	-	-	1.3	5.7	0.8	4.7	0.6	3.8	ns
		B port	-	-	1.1	5.4	0.9	4.1	0.7	3.0	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	1	-	1.2	-	1	ns
t_W	pulse width	data inputs	-	-	14	-	11	-	11	-	ns
f_{data}	data rate		-	-	-	70	-	90	-	90	Mbps

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 3.3 V ± 0.3 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	-	-	-	-	-	4.9	-	4.2	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	-	-	-	-	5.2	-	4.6	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	-	-	-	-	4.7	-	3.8	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	-	-	-	-	4.7	-	4.3	ns
t_{en}	enable time	OE to A; B [1]	-	-	-	-	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [1] [2]	-	-	-	-	-	8	-	8	ns
		OE to B; no external load [2]	-	-	-	-	-	8	-	8	ns
		OE to A; see Fig. 5	-	-	-	-	-	150	-	150	ns
		OE to B; see Fig. 5	-	-	-	-	-	170	-	120	ns
t_{TLH}	LOW to HIGH output transition time	A port	-	-	-	-	1.6	5.7	1.8	5.0	ns
		B port	-	-	-	-	1.5	5.4	0.9	3.9	ns
t_{THL}	HIGH to LOW output transition time	A port	-	-	-	-	1.0	4.5	0.6	3.5	ns
		B port	-	-	-	-	1.0	4.2	0.8	3.1	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	-	-	1	-	1	ns
t_W	pulse width	data inputs	-	-	-	-	11	-	9	-	ns
f_{data}	data rate		-	-	-	-	-	90	-	110	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] These values are guaranteed by design.
[3] Skew between any two outputs of the same package switching in the same direction.

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 4 and Fig. 6.

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	-	13.8	-	11.5	-	10.8	-	10.8	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	15.8	-	12.5	-	12.3	-	12.1	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	15.9	-	13.9	-	13.8	-	15.0	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	13.1	-	8.6	-	7.0	-	5.8	ns
t_{en}	enable time	OE to A; B [1]	-	200	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [1] [2]	-	18	-	18	-	18	-	18	ns
		OE to B; no external load [2]	-	19	-	18	-	18	-	18	ns
		OE to A; see Fig. 5	-	120	-	120	-	120	-	125	ns
		OE to B; see Fig. 5	-	170	-	125	-	175	-	125	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.6	16.4	2.8	12.3	2.0	11.3	2.0	10.4	ns
		B port	2.9	16.1	1.9	10.1	0.9	6.6	0.7	3.8	ns
t_{THL}	HIGH to LOW output transition time	A port	2.1	12.4	1.5	9.6	1.2	8.5	0.8	7.5	ns
		B port	1.5	10.9	1.0	6.9	0.9	4.8	0.8	3.9	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	1.1	-	1.1	-	1.2	-	1.1	ns
t_W	pulse width	data inputs	25	-	25	-	25	-	25	-	ns
f_{data}	data rate		-	40	-	40	-	40	-	40	Mbps
$V_{CC(A)}$ = 1.8 V ± 0.15 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	-	12.1	-	9.1	-	8.1	-	7.4	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	14.1	-	10.5	-	9.3	-	8.1	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	12.3	-	10.0	-	9.3	-	8.8	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	12.8	-	8.8	-	7.3	-	6.3	ns
t_{en}	enable time	OE to A; B [1]	-	200	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [1] [2]	-	14	-	14	-	14	-	14	ns
		OE to B; no external load [2]	-	17	-	14	-	14	-	14	ns
		OE to A; see Fig. 5	-	140	-	140	-	140	-	145	ns
		OE to B; see Fig. 5	-	165	-	125	-	175	-	125	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.2	14.9	2.0	10.8	1.9	9.8	1.9	9.0	ns
		B port	2.8	15.3	1.8	9.6	1.2	6.6	0.7	3.6	ns
t_{THL}	HIGH to LOW output transition time	A port	1.8	11.0	1.3	8.3	0.9	7.1	0.6	6.1	ns
		B port	1.3	10.4	1.0	6.8	0.9	4.9	0.7	3.8	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	1.1	-	1.1	-	1.1	-	1.1	ns
t_W	pulse width	data inputs	25	-	20	-	20	-	20	-	ns
f_{data}	data rate		-	40	-	50	-	50	-	50	Mbps

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 2.5 V ± 0.2 V											
t_{PHL}	HIGH to LOW propagation delay	A to B	-	-	-	7.8	-	6.6	-	5.9	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	-	-	-	8.5	-	7.4	-	6.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	-	-	-	7.4	-	6.0	-	5.3	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	-	-	-	7.8	-	5.8	-	4.5	ns
t_{en}	enable time	OE to A; B [1]	-	-	-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load [1] [2]	-	-	-	10	-	10	-	10	ns
		OE to B; no external load [2]	-	-	-	12	-	10	-	10	ns
		OE to A; see Fig. 5	-	-	-	105	-	105	-	105	ns
		OE to B; see Fig. 5	-	-	-	125	-	175	-	120	ns
t_{TLH}	LOW to HIGH output transition time	A port	-	-	1.7	9.1	1.7	8.0	1.8	7.3	ns
		B port	-	-	1.8	9.1	1.3	6.8	0.9	4.1	ns
t_{THL}	HIGH to LOW output transition time	A port	-	-	1.3	7.1	0.8	5.9	0.6	4.8	ns
		B port	-	-	1.1	6.8	0.9	5.1	0.7	3.8	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	1.1	-	1.3	-	1.1	ns
t_W	pulse width	data inputs	-	-	16.7	-	12.5	-	12.5	-	ns
f_{data}	data rate		-	-	-	60	-	80	-	80	Mbps

Symbol	Parameter	Conditions		$V_{CC(B)}$								Unit
				1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 3.3 V ± 0.3 V												
t_{PHL}	HIGH to LOW propagation delay	A to B		-	-	-	-	-	6.1	-	5.3	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		-	-	-	-	-	6.5	-	5.8	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		-	-	-	-	-	5.9	-	4.8	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		-	-	-	-	-	5.9	-	5.4	ns
t_{en}	enable time	OE to A; B	[1]	-	-	-	-	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load	[1] [2]	-	-	-	-	-	9	-	9	ns
		OE to B; no external load	[2]	-	-	-	-	-	9	-	9	ns
		OE to A; see Fig. 5		-	-	-	-	-	150	-	150	ns
		OE to B; see Fig. 5		-	-	-	-	-	170	-	120	ns
t_{TLH}	LOW to HIGH output transition time	A port		-	-	-	-	1.6	7.1	1.8	6.3	ns
		B port		-	-	-	-	1.5	6.8	0.9	4.9	ns
t_{THL}	HIGH to LOW output transition time	A port		-	-	-	-	1.0	5.6	0.7	4.4	ns
		B port		-	-	-	-	1.0	5.3	0.8	3.9	ns
$t_{sk(o)}$	output skew time	between channels	[3]	-	-	-	-	-	1.1	-	1.1	ns
t_W	pulse width	data inputs		-	-	-	-	13	-	10	-	ns
f_{data}	data rate			-	-	-	-	-	80	-	100	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] These values are guaranteed by design.
[3] Skew between any two outputs of the same package switching in the same direction.

Table 12. Typical power dissipation capacitance

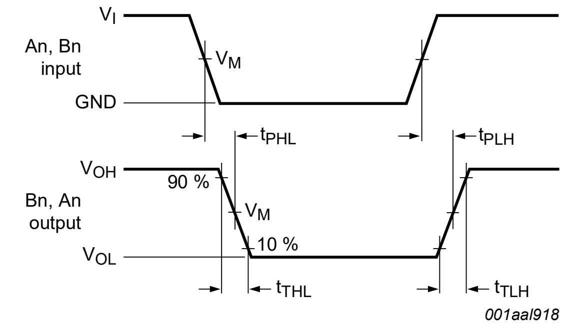
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7 [1] [2]

Symbol	Parameter	Conditions	$V_{CC(A)}$							Unit
			1.2 V	**1.2 V**	**1.5 V**	**1.8 V**	**2.5 V**	**2.5 V**	**3.3 V**	
			$V_{CC(B)}$							
			1.8 V	**5.0 V**	**1.8 V**	**1.8 V**	**2.5 V**	**5.0 V**	**3.3 V to 5.0 V**	
T_{amb} = 25 °C										
C_{PD}	power dissipation capacitance	outputs enabled; OE = $V_{CC(A)}$								
		A port: (direction A to B)	7.7	7.4	8.0	8.3	8.4	8.0	8.7	pF
		A port: (direction B to A)	5.9	6.3	6.6	7.5	8.2	7.0	8.5	pF
		B port: (direction A to B)	20.8	26.6	19.9	19.7	20.0	24.3	22.2	pF
		B port: (direction B to A)	18.9	23.8	18.4	18.4	19.0	21.2	20.3	pF
		outputs disabled; OE = GND								
		A port: (direction A to B)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
		A port: (direction B to A)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
		B port: (direction A to B)	0.01	0.02	0.01	0.01	0.01	0.01	0.01	pF
		B port: (direction B to A)	0.01	0.03	0.01	0.01	0.01	0.01	0.01	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = load capacitance in pF;
V_{CC} = supply voltage in V; N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] f_i = 10 MHz; V_I = GND to V_{CC}; $t_r = t_f$ = 1 ns; C_L = 0 pF; $R_L = \infty\ \Omega$.

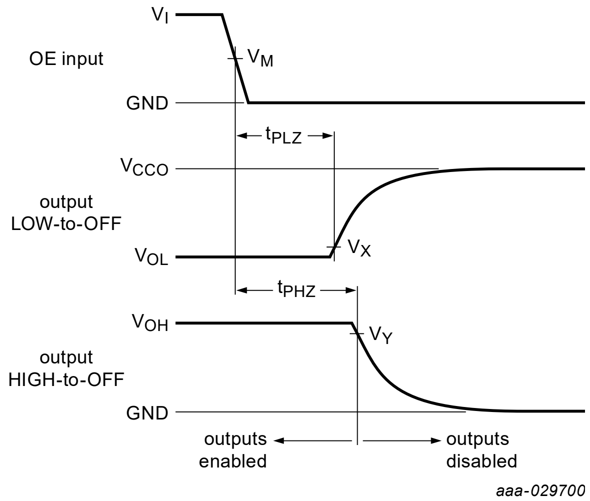
10.1. Waveforms and test circuit



Measurement points are given in Table 13.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The data input (An, Bn) to data output (Bn, An) propagation delay times

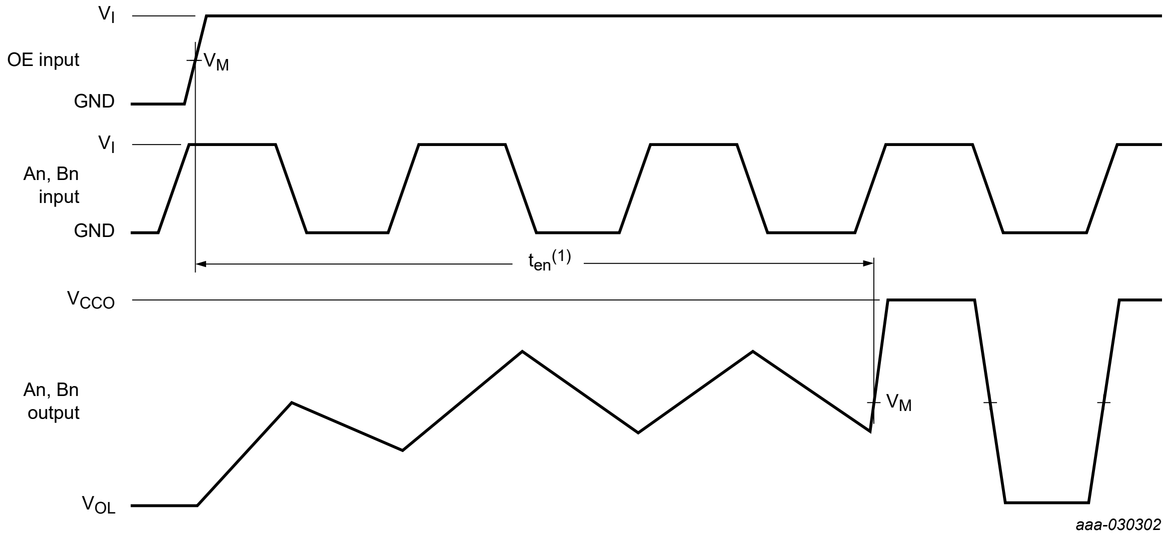


Measurement points are given in Table 13.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

V_{CCO} is the supply voltage associated with the output.

Fig. 5. Disable times



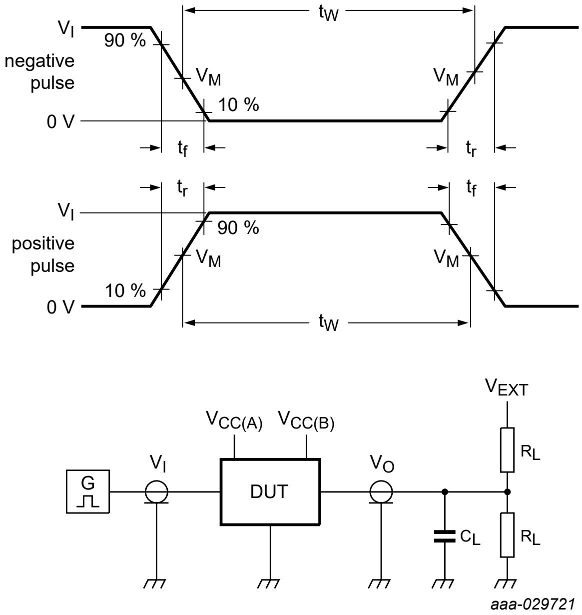
(1) The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. See also Section 11.6.
Measurement points are given in Table 13.
V_{OL} is a typical output voltage level that occur with the output load.
V_{CCO} is the supply voltage associated with the output.

Fig. 6. Enable times

Table 13. Measurement points [1] [2]

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.5 V ± 0.1 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.8 V ± 0.15 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.5 V ± 0.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.3 V ± 0.3 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V
5.0 V ± 0.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 14.

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ns.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 14. Test data

Supply voltage		Input		Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	Δt/ΔV	C_L	R_L [2]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [3]
1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ; for measuring enable and disable times, R_L = 50 kΩ.

[3] V_{CCO} is the supply voltage associated with the output.

11. Application information

11.1. Voltage level-translation applications

The NXS0108-Q100 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I^2C or 1-wire which use open-drain drivers, it may also be used in applications where push-pull drivers are connected to the ports, however the NXB0108-Q100 may be more suitable.

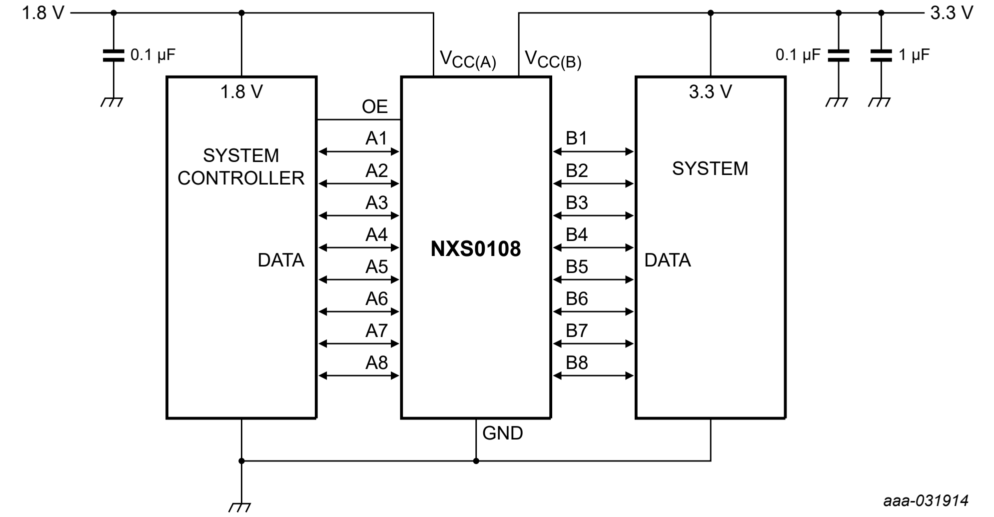


Fig. 8. Typical operating circuit

11.2. Architecture

The architecture of the NXS0108-Q100 is shown in Fig. 9. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

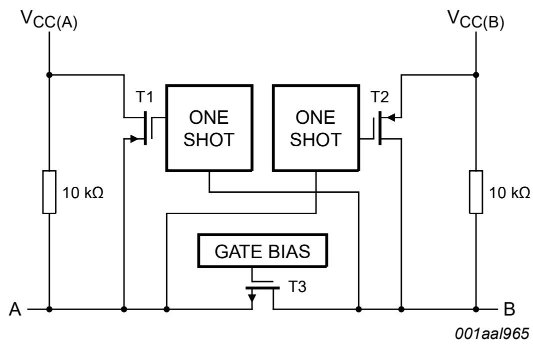


Fig. 9. Architecture of NXS0108-Q100 I/O cell (one channel)

The NXS0108-Q100 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a LOW-to-HIGH transition the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2) bypassing the 10 kΩ pull-up resistors and increasing current drive capability. The one-shot is activated once the input transition reaches approximately $V_{CCI}/2$; it is de-activated approximately 50 ns after the output reaches $V_{CCO}/2$. During the acceleration time the driver output resistance is between approximately 50 Ω and 70 Ω. To avoid signal contention and minimize dynamic I_{CC}, the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

11.3. Input driver requirements

As the NXS0108-Q100 is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system; the max data rate, HIGH-to-LOW output transition time (t_{THL}) and propagation delay (t_{PHL}) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the datasheet assume a driver with output impedance below 50 Ω is used.

11.4. Output load considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading there is a risk that the output will not reach the positive rail within the one-shot pulse duration.To avoid excessive capacitive loading and to ensure correct triggering of the one-shot it's recommended to use short trace lengths and low capacitance connectors on NXS0108-Q100 PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round trip delay of any reflection is within the one-shot pulse duration (approximately 50 ns).

11.5. Power up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NXS0108-Q100 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

11.6. Enable and disable

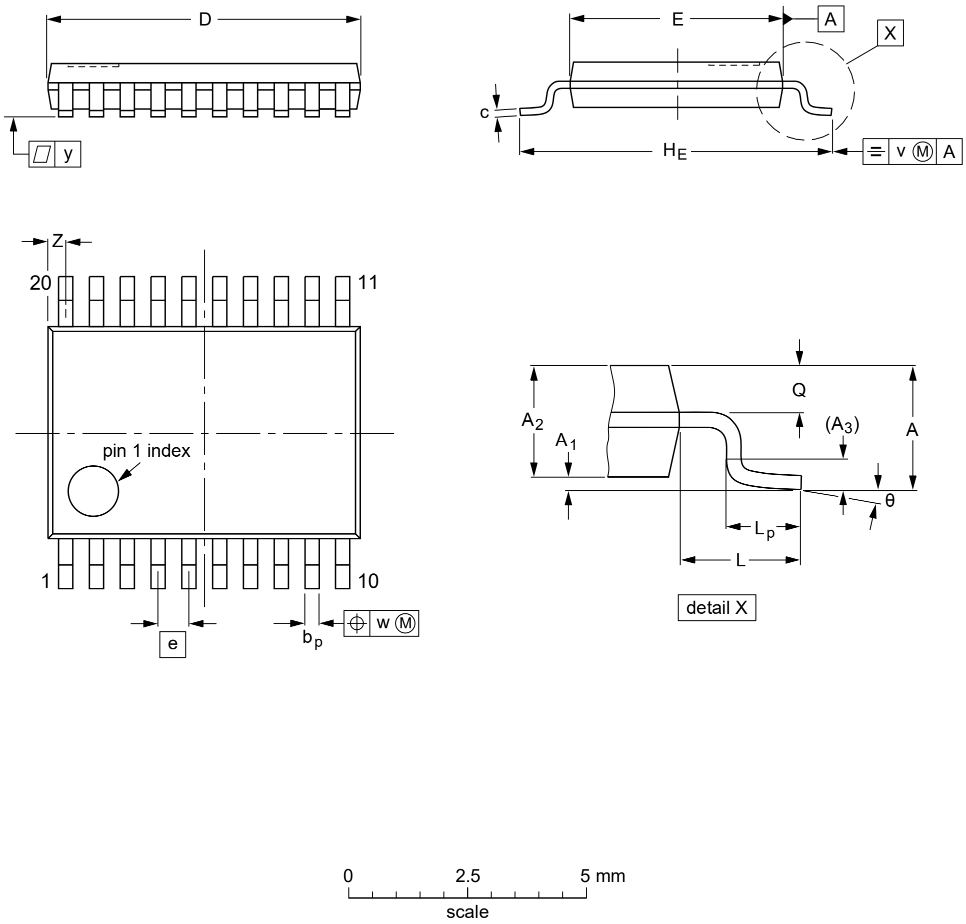
An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

11.7. Pull-up or pull-down resistors on I/O lines

The NXS0108-Q100 has the pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40 kΩ when the output is driving LOW. R_{PUA} and R_{PUB} have a value of 4 kΩ when the output is driving HIGH. R_{PUA} and R_{PUB} are disabled when OE = LOW. This feature provides lower static power consumption (when the I/Os are passing a LOW) and supports lower V_{OL} values for the same size pass-gate transistor and helps improve simultaneous switching performance.

12. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

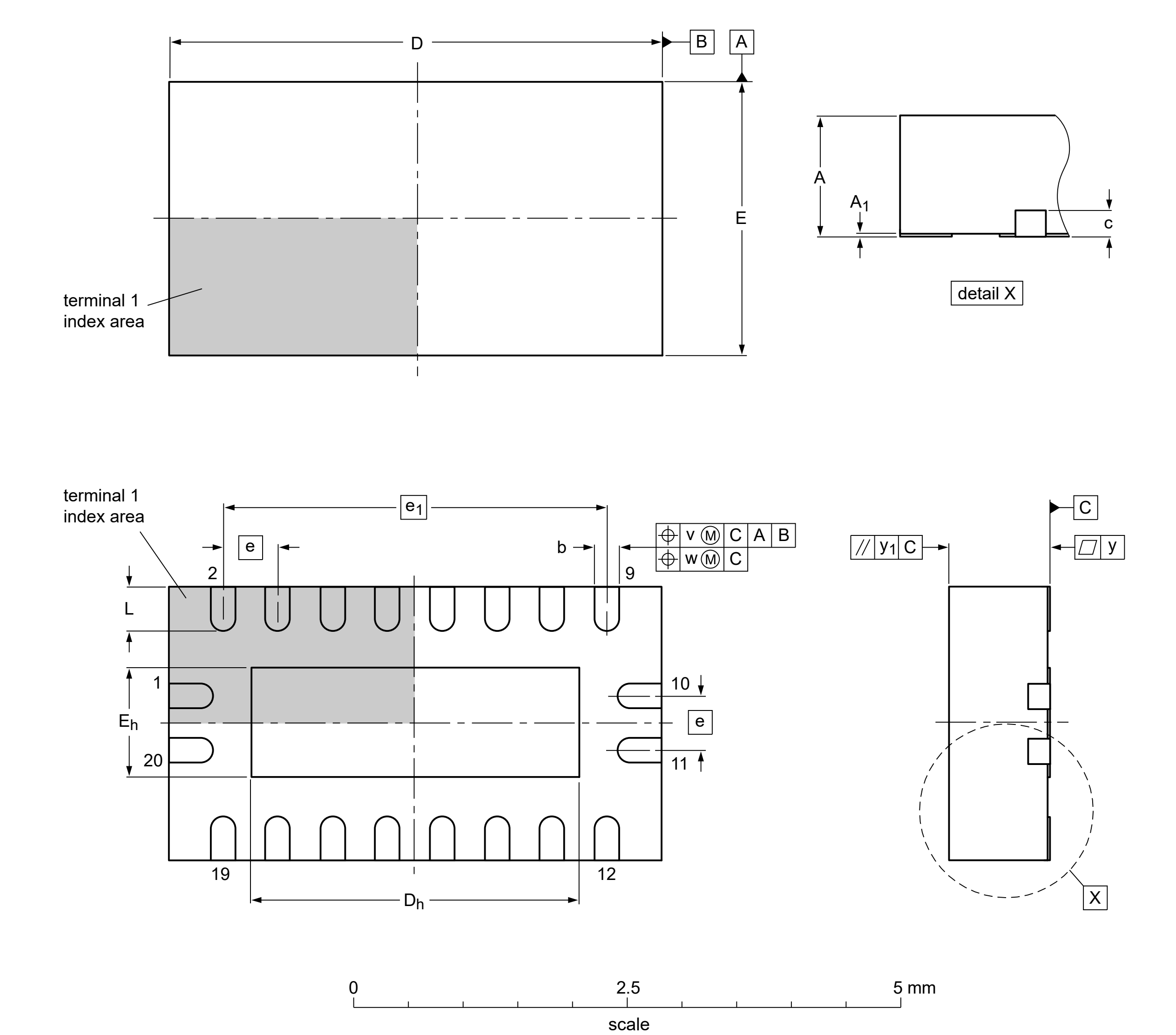
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 10. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
	max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
mm	nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~03-01-27~~ 14-12-12

Fig. 11. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 15. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
MM	Machine Model
SMBus	System Management Bus

14. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXS0108_Q100 v.1	20200915	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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