

4 ch Current Driver Integrated, Built-in MOS for Boost, Boost DC/DC Converter White LED Driver for Automotive

BD83A04EFV-M

General Description

This IC is a white LED driver for LCD backlight. It has MOS for boost and 4 ch current drivers for LED drive, making it ideal for high brightness LED drive. LED pin maximum voltage is 50 V, making it suitable for driving medium LCD panels. The dimming is controlled by the PWM signal and can be set up to 20,000: 1@100 Hz. It also supports analog dimming and can accommodate even higher brightness ranges by combining with PWM dimming. DC/DC converters can be controlled for boost applications, and the input operating voltage range is 4.5 V to 48 V.

Features

- AEC-Q100 Qualified^(Note 1)
- Functional Safety Supportive Automotive Products
- Built-in 4 ch Current Driver for LED Drive
- Built-in MOS for Boost
- Current Mode Boost DC/DC Converter
- Load Switch (M1) Control Pin
- PWM Dimming
(20,000: 1@100 Hz, 100 Hz to 25 kHz)
- Spread Spectrum Function
- DC/DC Converter Oscillation Frequency External Synchronization Function
- LSI Protect Functions (UVLO, OVP, TSD, OCP)
- LED Anode/Cathode Short Circuit Protection Function
- LED Open/Short Protection Function

(Note 1) Grade 1

Key Specifications

- Input Operating Voltage Range: 4.5 V to 48 V
- Output LED Current Absolute Accuracy: $\pm 5.0\%$ @80.1 mA
Ta = -40 °C to +125 °C
- DC/DC Oscillation Frequency: 200 kHz to 2420 kHz
- Operating Temperature: -40 °C to +125 °C
- LED Maximum Current: 120 mA/ ch
- LED Maximum Dimming Ratio: 20,000: 1@100 Hz
- LED1 to LED4 Pin Maximum Voltage: 50 V

Package

HTSSOP-B24

W (Typ) x D (Typ) x H (Max)

7.8 mm x 7.6 mm x 1.0 mm



Applications

- Automotive CID (Center Information Display) Panel
- Navigation
- Cluster Panel
- HUD (Head Up Display)
- Other Small and Medium Sized LCD Panel for Automotive

Typical Application Circuit

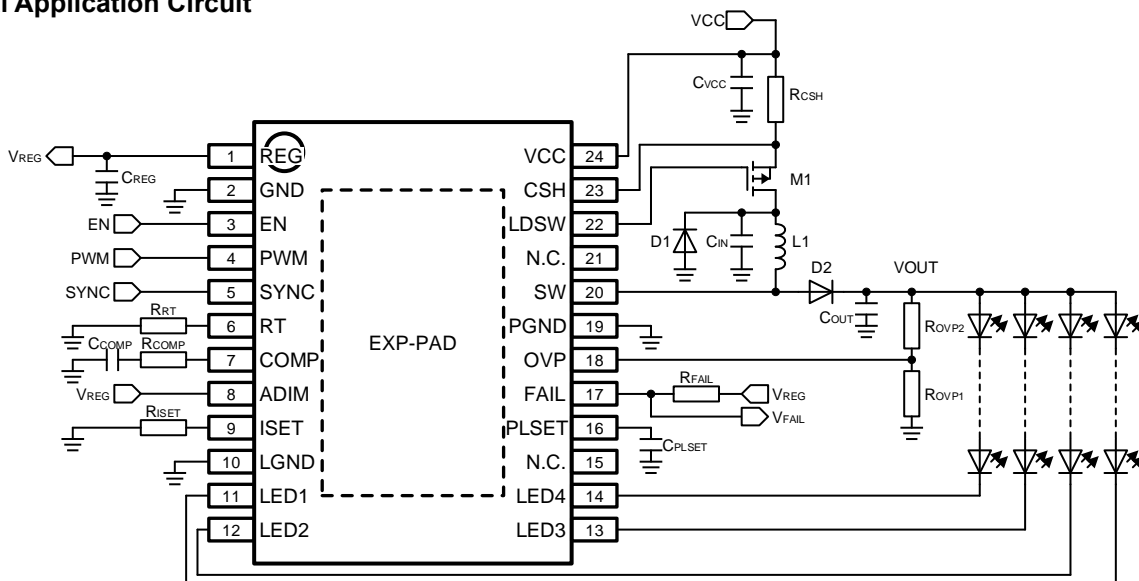


Figure 1. Boost Application Circuit Diagram

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

○This product is protected by U.S. Patent No.7,235,954, No.7,541,785 and No.7,944,189.

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Pin Configuration

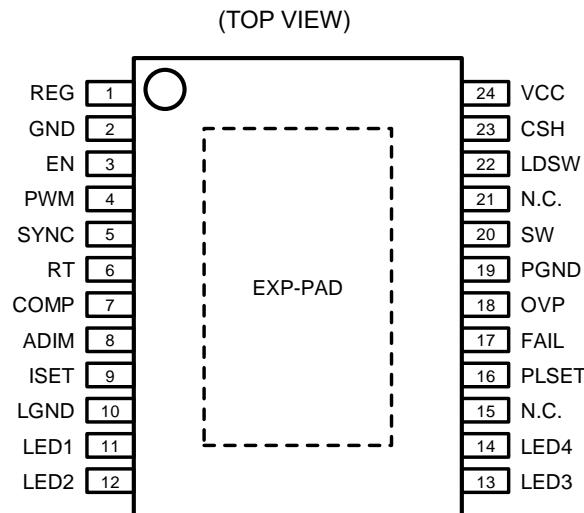


Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Signal Type (Note 1)	Function
1	REG	A	Internal reference voltage: Used as the reference voltage for the internal circuit. 5 V (Typ) is generated and output by setting the EN pin to High. Connect a capacitance of 2.2 μ F for phase compensation.
2	GND	A	Small signal ground: Use this for the ground of external components connected to the REG, RT, COMP, ADIM, ISET, PLSET, OVP, and VCC pins.
3	EN	I	Enable input: The EN pin is turned High to activate the internal circuit. The internal circuit stops and the standby state is set by setting to Low.
4	PWM	I	PWM dimming signal: The LED current can be controlled according to On Duty of the input PWM signal.
5	SYNC	I	External synchronization frequency input / SSCG setting: The internal oscillation frequency can be externally synchronized by inputting an external clock signal to the SYNC pin before the Self Diagnosis is completed. When using spread spectrum mode (SSCG), short the SYNC pin and the REG pin beforehand.
6	RT	A	Resistor connection for oscillation frequency setting: The oscillation frequency (f_{osc}) of DC/DC converter can be set by connecting a resistor (R_{RT}) between the RT pin and the GND pin.
7	COMP	A	Phase compensating capacitor connection: The reference voltage and LED pin voltage generated by REF Voltage block are compared and output by Error AMP. Connect a filter for phase compensation.
8	ADIM	A	DC dimming setting: ISET pin voltage can be changed according to the voltage input to the ADIM pin. When using only PWM dimming, short the ADIM pin with the REG pin.
9	ISET	A	Resistor connection for LED current setting: LED current (I_{LED}) can be set by connecting a resistor (R_{ISET}) between the ISET pin and the GND pin.
10	LGND	P	Large current ground 1: GND of the current driver (the LED1, LED2, LED3, and LED4 pins).
11	LED1	P	LED cathode connection 1: Open drain output of the current driver ch 1 for LED drive. Connect to the LED cathode.
12	LED2	P	LED cathode connection 2: Open drain output of the current driver ch 2 for LED drive. Connect to the LED cathode.
13	LED3	P	LED cathode connection 3: Open drain output of the current driver ch 3 for LED drive. Connect to the LED cathode.
14	LED4	P	LED cathode connection 4: Open drain output of the current driver ch 4 for LED drive. Connect to the LED cathode.

(Note 1) **A:** Sensitive signal such as detect and reference, **I:** Input signal from other units, **P:** Large current signal susceptible to impedance, including transient current.

Pin Descriptions – continued

Pin No.	Pin Name	Signal Type (Note 1)	Function
15	N.C.	-	Not connected internally.
16	PLSET	A	Switching pulse number setting: Pulse addition function is provided to stabilize DC/DC converter output voltage even when PWM Duty is low. The number of switching pulses to be added can be set by the capacitance value connected between the PLSET pin and the GND pin.
17	FAIL	O	Error output flag: Outputs the status of protective operation from the FAIL pin. Since this pin is an open drain output, use a resistor to pull it up to the REG pin, etc.
18	OVP	A	Overvoltage protection and short circuit protection detection input: When OVP pin voltage rises to 1.21 V or more, the overvoltage protection (OVP) is activated, and DC/DC converters are switched OFF. If OVP pin voltage is 0.1 V or less for 3.56 ms, Short Circuit Protection (SCP) is activated, and both DC/DC converter and the current driver are turned OFF.
19	PGND	P	Large current ground 2: GND of DC/DC converter. Use it for C _{OUT} ground.
20	SW	P	FET drain signal for boost: Switching signal output of DC/DC converter. Connect the SW pin to the node between the inductor and the rectifier diode.
21	N.C.	-	Not connected internally.
22	LDSW	P	Output for driving the load switch gate: The signal output for driving the gate of the load switch. When the input overcurrent protection is activated, the load switch is turned OFF as LDSW pin voltage = VCC pin voltage.
23	CSH	A	Input current detection input: The input current is converted to voltage by the input current detection resistor (R _{CSH}) connected between the VCC-CSH pin and detected by the CSH pin. Turns the load switch OFF when the input overcurrent protection is activated.
24	VCC	P	Power supply voltage input: The input operating voltage range is 4.5 V to 48 V, but when the IC is started, start it with VCC ≥ 5.5 V. The decoupling capacitor (C _{VCC}) between the VCC pin and the GND pin should be as close to the IC pin as possible.
-	EXP-PAD	-	The EXP-PAD should be connected to the board ground.

(Note 1) **A:** Sensitive signal such as detect and reference, **I:** Input signal from other units, **O:** Output signal to other units, **P:** Large current signal susceptible to impedance, including transient current.

Block Diagram

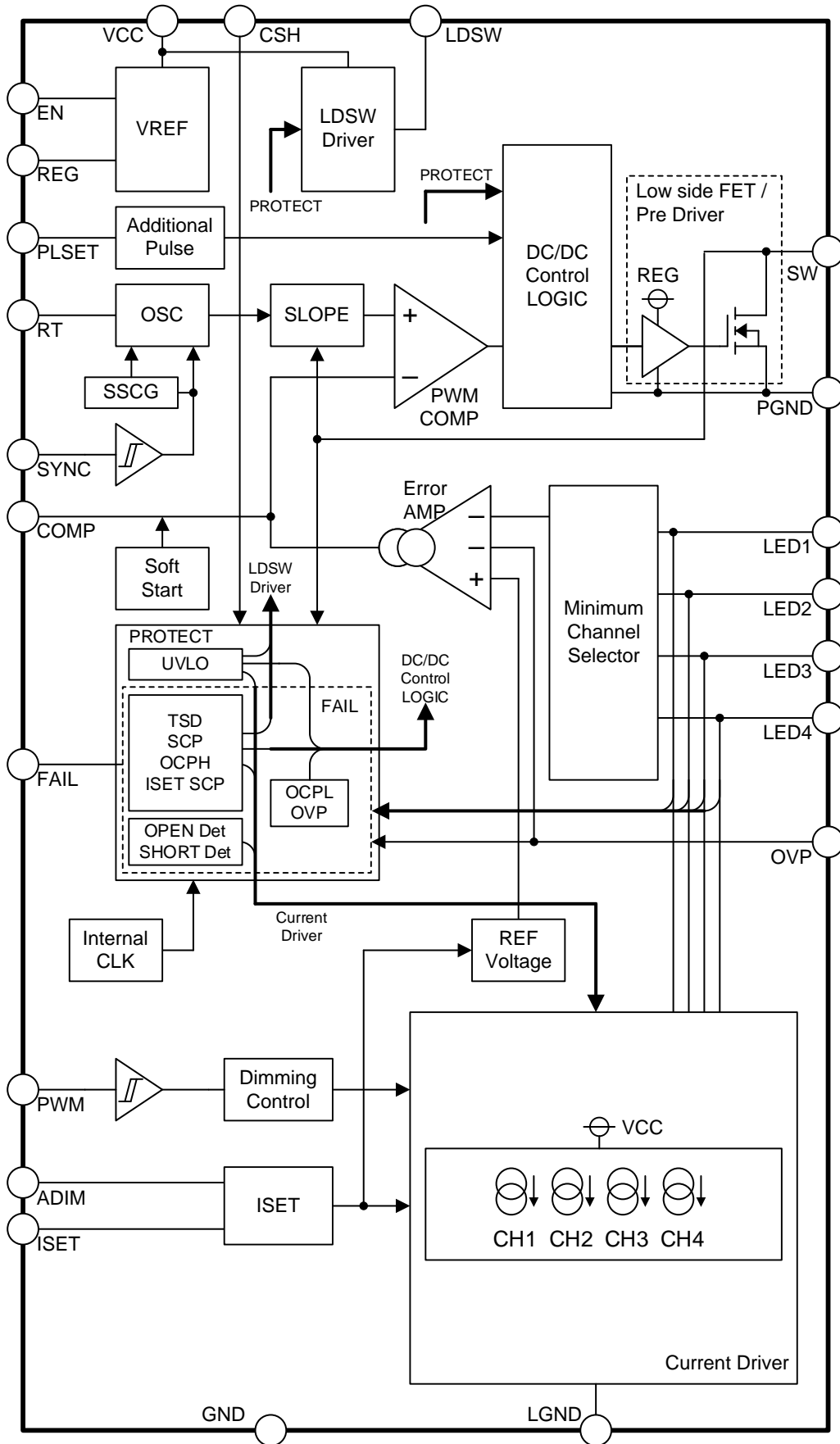


Figure 3. Internal Block Diagram

Description of Blocks

Unless otherwise stated, the value in the sentence is the typical value.

1 VREF

Internal reference voltage circuit. By setting the EN pin to High, 5 V is generated and output to the REG pin. REG voltage is used as the power supply for the internal circuit. Also, this is used to fix each input pin to High voltage outside the IC. Connect [REG capacitance \(\$C_{REG} = 2.2 \mu\text{F}\$ \)](#) to the REG pin for the phase compensation. Note that if C_{REG} is not connected, unstable operation such as oscillation will occur.

2 LDSW Driver

Input overcurrent protection circuit. If the voltage between the VCC-CSH pin is 0.1 V or more and continues for 10 μs or more, the input overcurrent protection is activated, and the load switch (M1) is turned OFF as LDSW pin voltage = VCC pin voltage. Then, after 3.56 ms elapses, the load switch is turned ON. At this time, if the voltage between the VCC-CSH pin is 0.1 V or more, the load switch is turned OFF again. If the voltage between the VCC-CSH pin is less than 0.1 V, [Self Diagnosis](#) is performed and restarted. When the input overcurrent protection is detected, the FAIL pin goes Low. The VCC-LDSW pin is connected by a 3 M Ω resistor inside the IC. Do not connect a resistor between the VCC-LDSW pin because connecting a resistor between the VCC-LDSW pin outside the IC may prevent the load switch from being turned ON. When the VCC voltage is turned ON setting the EN pin to Low, the voltage between the VCC-LDSW pins may open momentarily and an inrush current may flow depending on the VCC startup speed and the type of load switch used. Be sure to check with the actual application.

3 OSC (Oscillator)

Oscillation frequency generator. [The oscillation frequency \(\$f_{osc}\$ \) of DC/DC converter](#) can be set by connecting a resistor for oscillation frequency setting (R_{RT}) between the RT pin and ground. In addition, the oscillation frequency of DC/DC converter can be [externally synchronized](#) by inputting the external synchronization frequency (f_{sync}) to the SYNC pin.

4 SSCG (Spread Spectrum Clock Generator)

Spread spectrum circuit. [The spread spectrum function \(SSCG\)](#) is activated by shorting the SYNC pin and the REG pin. Noise peaks can be reduced by periodically changing the oscillation frequency by SSCG. The fluctuation range of the frequency due to SSCG is from 100 % to 92 % of the set oscillation frequency. The oscillation frequency fluctuation period is 2.3 kHz.

5 SLOPE

This circuit generates a saw wave that serves as the source of the switching pulse of DC/DC converter. SLOPE output signal and COMP pin voltage are compared, and a switching pulse is generated.

6 Minimum Channel Selector

Selector circuit for detecting LED pin voltages. Selects the lowest pin voltage among LED1 to LED4 pin voltages and inputs it in Error AMP.

7 Error AMP (Error Amplifier)

This is an error amplifier that takes LED control voltage and the smallest value of the LED1 to LED4 pin voltages as input. [Phase compensation can be set](#) by connecting a resistor and a capacitor to the COMP pin.

8 Soft Start

Soft start circuit for DC/DC converters. This function is used to suppress a steep increase in the inductor current at startup and an overshoot in the output voltage. Controls the change in switching Duty by limiting the rising edge of the output of Error AMP (COMP pin voltage) with the soft start function.

9 PWM COMP (PWM Comparator)

This comparator compares COMP pin voltage, which is the output of Error AMP, with SLOPE output signal. Controls the Duty of the switching pulse of DC/DC converter.

10 Additional Pulse

This circuit adds switching pulses of DC/DC converter. With the [pulse addition function](#), the LED current can be supplied stably even when the PWM dimming ratio decreases.

11 DC/DC Control LOGIC

This circuit generates the logic of the built-in Low side FET for boost output from the SW pin.

12 Low side FET / Pre Driver

Built-in Low side FET for boost output from the SW pin and its driving circuit.

Description of Blocks - continued**13 Internal CLK**

This circuit generates the internal reference clock. It is a clock of 2.3 MHz and used as a counter.

14 Dimming Control

This circuit controls the dimming rate during PWM dimming.

15 Current Driver / ISET

Current driver circuit for lighting LED. [LED current can be set](#) by connecting a resistor to the ISET pin.

16 PROTECT

Outputs the status of protective operation from the FAIL pin. Since this pin is an open drain output, connect it to the REG pin with a resistor. If the status of protective operation is not monitored, turn the FAIL pin to OPEN or connect to the GND pin.

16.1 UVLO (Under Voltage Lockout)

Under Voltage Lockout. When VCC pin voltage is 4.10 V or less or REG pin voltage is 3.95 V or less, Under Voltage Lockout (UVLO) is activated, and the load switch (M1), DC/DC switching, and current driver turn OFF. When VCC pin voltage is 4.25 V or more and REG pin voltage is 4.10 V or more, UVLO is released and the IC restarts from [Self Diagnosis](#). When UVLO is detected, output of the FAIL pin does not change. When the FAIL pin is pulled up to REG, FAIL pin voltage will also drop as REG decreases.

16.2 TSDLED (Thermal Shutdown for Current Driver)

This is a temperature protection circuit that monitors the vicinity of the current driver on the chip. Prevents chip temperature from rising due to output current fault. When the chip temperature rises to 175 °C or more, the temperature protection circuit (TSDLED) is activated, the load switch (M1), DC/DC switching, and current driver are turned OFF. When the chip temperature falls 150 °C or less, TSDLED is released, the IC restarts from [Self Diagnosis](#). When TSDLED is detected, the output of the FAIL pin does not change.

16.3 TSDREG (Thermal Shutdown for REG)

This is a temperature protection circuit that monitors the vicinity of the REG pin on the chip. Prevents chip temperature rising due to the REG pin failure. When the chip temperature rises to 175 °C or more, the temperature protection circuit (TSDREG) is activated, and REG pin voltage, load switch (M1), DC/DC switching, and current driver turn OFF. When the FAIL pin is pulled up to the REG pin, FAIL pin voltage drops as REG pin voltage is turned OFF, and it is output to Low. When the FAIL pin is pulled up to an external power supply, the FAIL pin is output to High. When the chip temperature falls 150 °C or less, TSDREG is released and the IC restarts from [Self Diagnosis](#).

16.4 OCPL (Over Current Protection for Low side)

When the current flowing through Low side FET (the SW pin) becomes 3.6 A or more, the overcurrent protection (OCPL) is activated and only DC/DC switching is stopped. If the current is less than 3.6 A, the overcurrent protection is released, and switching is resumed. When OCPL is detected, output of the FAIL pin does not change.

16.5 OVP (Over Voltage Protection)

Output overvoltage protection circuit. When OVP pin voltage (resistor division of DC/DC converter output voltage) becomes to 1.21 V or more, the overvoltage protection circuit (OVP) activates and only DC/DC switching is stopped. When OVP pin voltage falls 1.16 V or less, OVP is released. When OVP is detected, the output of the FAIL pin goes Low.

16.6 OPEN Det (LED Open Detection)

LED open protection circuit. When any of LED1 to LED4 pin voltages is 0.2 V or less and OVP pin voltage is 1.21 V or more, LED open protection (OPEN Det) is activated, and the current driver is latched OFF only for the LED row that is open. OPEN Det is released when V_{EN} = Low or UVLO is detected. When OPEN Det is detected, the FAIL pin goes Low.

16 PROTECT – continued**16.7 SHORT Det (LED Short Detection)**

LED short protection circuit. When LED pin voltage is 5 V or more for 3.56 ms (counter), LED short protection (SHORT Det) is activated, and the current driver is latched OFF only for the corresponding LED row. However, the counter is reset when LED pin voltage does not satisfy the detection condition prior to SHORT Det being activated. SHORT Det is released when $V_{EN} = \text{Low}$ or UVLO is detected. Since the 3.56 ms counter is counted up only when PWM = High, the time until SHORT Det is detected varies depending on PWM Duty. When SHORT Det is detected, the FAIL pin goes Low. SHORT Det can be detected when the PWM pulse width is 20 μs (MIN) or more.

16.8 SCP (Short Circuit Protection)

Short Circuit Protection circuit. If any of the LED1 to LED4 pin voltages are 0.2 V or less or OVP pin voltage is 0.1 V or less for 3.56 ms (counter), the Short Circuit Protection (SCP) is activated, and the load switch (M1), DC/DC switching, and current driver turn OFF. However, the counter is reset when each pin voltage does not satisfy the condition prior to SCP being activated. The SCP is released when $V_{EN} = \text{Low}$ or UVLO is detected. When SCP is detected, the FAIL pin goes Low. Also, DC/DC converter attempts to output higher voltage because the grounded LED pin voltage (lowest LED pin voltage) is controlled to be V_{LEDCTL} . Depending on the power supply voltage and the load condition, OVP pin voltage may become 1.21 V or more prior to SCP being activated, and LED open protection may be activated first. In this case, current driver turns OFF only for the grounded LED pin, but the LED continues to light in a state where the current control is lost because it has been grounded. Even when LED open protection is detected, the FAIL pin goes Low. Therefore, abnormality can be detected by monitoring this.

16.9 OCPH (Over Current Protection for High side) / LDSW Driver

Input overcurrent protection circuit. If a condition in which the voltage between the VCC-CSH pin is 0.1 V or more continues for 10 μs or more, the input overcurrent protection (OCPH) is activated. It becomes LDSW pin voltage = VCC pin voltage and the load switch (M1), DC/DC switching, and current driver turn OFF. Then, after 3.56 ms (counter) elapses, the load switch is turned ON. At this time, if the voltage between VCC-CSH is 0.1 V or more, the load switch, DC/DC switching, and current driver are turned OFF again. Also, if the voltage between VCC-CSH is less than 0.1 V, [Self Diagnosis](#) is performed and restarted. When OCPH is detected, the FAIL pin goes Low. The components on the overcurrent path may generate current again with restart, resulting in heat generation. Check the calorific value on the actual device.

16.10 ISET Pin Fault (ISET-GND Short Protection)

ISET pin fault protection circuit. When the resistance value connected to the ISET pin falls 3.5 k Ω or less (when ADIM = REG), ISET pin fault protection is activated, and the load switch (M1), DC/DC switching, and current driver are turned OFF. If the resistance value connected to the ISET pin is more than 3.5 k Ω (when ADIM = REG), ISET pin fault protection is released, and the load switch, DC/DC switching, and current driver are turned ON. When ISET pin fault is detected, the FAIL pin goes Low.

Description of Blocks – continued

Detect Conditions and Operation at Detection of Each Protection Function (All values in the table are Typ values)

No.	Protection Function (Block Name)	Detect Condition		Operation at Detection			
		[Detect]	[Release]	Load Switch	DC/DC Switching	Current Driver	FAIL
1	Under Voltage Lockout (UVLO)	$V_{CC} \leq 4.10 \text{ V}$ or $V_{REG} \leq 3.95 \text{ V}$	$V_{CC} \geq 4.25 \text{ V}$ and $V_{REG} \geq 4.10 \text{ V}$	OFF	OFF	OFF	High (Note 5)
2	Thermal Shutdown LED (TSDLED)	$T_j \geq 175 \text{ }^\circ\text{C}$	$T_j \leq 150 \text{ }^\circ\text{C}$	OFF	OFF	OFF	High (Note 5)
3	Thermal Shutdown REG (TSDREG)	$T_j \geq 175 \text{ }^\circ\text{C}$	$T_j \leq 150 \text{ }^\circ\text{C}$	OFF	OFF	OFF	High (Note 5) (Note 6)
4	Overcurrent Protection (OCPL)	$I_{SW} \geq 3.6 \text{ A}$	$I_{SW} < 3.6 \text{ A}$	ON	OFF	ON	High (Note 5)
5	Overvoltage Protection (OVP)	$V_{OVP} \geq 1.21 \text{ V}$	$V_{OVP} \leq 1.16 \text{ V}$	ON	OFF	ON	Low
6	LED Open Protection (OPEN Det)	$V_{LEDn} \leq 0.2 \text{ V}$ (Note 1) and $V_{OVP} \geq 1.21 \text{ V}$	$V_{EN} = \text{Low}$ or Detects UVLO	ON	ON	Only detection LED pin is OFF	Latch Low
7	LED Short Protection (SHORT Det)	Detects $V_{LEDn} \geq 5.0 \text{ V}$ for 3.56 ms or more (Note 2)	$V_{EN} = \text{Low}$ or Detects UVLO	ON	ON	Only detection LED pin is OFF	Latch Low
8	Short Circuit Protection (SCP) (Note 3)	Detects $V_{LEDn} \leq 0.2 \text{ V}$ or $V_{OVP} \leq 0.1 \text{ V}$ for 3.56 ms or more	$V_{EN} = \text{Low}$ or Detects UVLO	OFF	OFF	OFF	Latch Low
9	Input Overcurrent Protection (OCPH) (Note 3)	Detects voltage between the VCC-CSH pin $\geq 0.1 \text{ V}$ for 10 μs or more	Voltage between the VCC-CSH pin $< 0.1 \text{ V}$ (Note 4)	OFF	OFF	OFF	Low
10	ISET-GND Short Protection (ISET Pin Fault)	ISET resistor $\leq 3.5 \text{ k}\Omega$ (when ADIM = REG)	ISET resistor $> 3.5 \text{ k}\Omega$ (when ADIM = REG)	OFF	OFF	OFF	Low

(Note 1) LEDn indicates one of the LED1 to LED4 pins.

(Note 2) LED pin voltage of at least 1 channel shall be less than $V_{LEDCTL(MIN)} \times 1.2$. When LED pin voltages of all channels are 2.4 V or more, the LED short protection does not operate. Since the 3.56 ms counter is counted up only when PWM = High, the time until SHORT Det is detected varies depending on PWM Duty.

(Note 3) When Short Circuit Protection (SCP) and Input Overcurrent Protection (OCPH) are detected at the same time, the operation of Input Overcurrent Protection takes precedence.

(Note 4) When 3.56 ms elapses after the load switch is turned OFF, the load switch turns ON. At this time, when the voltage between VCC-CSH $\geq 0.1 \text{ V}$, the load switch, DC/DC switching, and current driver are turned OFF again. Also, when the voltage between VCC-CSH $< 0.1 \text{ V}$, [Self Diagnosis](#) is performed and restarted.

(Note 5) When pulled up to any voltage, it becomes High output.

(Note 6) REG is also turned OFF during TSDREG, so if pulled up to the REG pin, FAIL pin voltage drops with REG pin voltage.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
VCC, LDSW, CSH, SW Pin Voltage	VCC, VLDSW, VCSH, VSW	-0.3 to +50.0	V
Voltage Between VCC-LDSW, VCC-CSH Pin	VCC-VLDSW, VCC-VCSH	-0.3 to +7.0	V
LED1, LED2, LED3, LED4 Pin Voltage	VLED1, VLED2, VLED3, VLED4	-0.3 to +50.0	V
RT, COMP, ISET, PLSET, OVP, ADIM, FAIL Pin Voltage	VRT, VCOMP, VISET, VPLSET, VOVP, VADIM, VFAIL	-0.3 to VREG	V
EN, REG, SYNC, PWM Pin Voltage	VEN, VREG, VSYNC, VPWM	-0.3 to +7.0	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance^(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 3)	2s2p ^(Note 4)	
HTSSOP-B24				
Junction to Ambient	θ_{JA}	90.9	30.1	°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ_{JT}	6	4	°C/W

(Note 1) Based on JESD51-2A (Still-Air). The BD83A04EFV-M chip is used.

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μ m

Layer Number of Measurement Board	Material	Board Size	Thermal Via ^(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ 0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μ m	74.2 mm x 74.2 mm	35 μ m	74.2 mm x 74.2 mm	70 μ m

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Operating Range		Unit
		Min	Max	
Power Supply Voltage ^(Note 1)	VCC	4.5	48.0	V
DC/DC Oscillation Frequency Range (SSCG = OFF)	f _{OSC}	200	2420	kHz
PWM Frequency Range ^(Note 2)	f _{PWM}	0.1	25.0	kHz
ADIM Input Voltage Range ^(Note 3)	V _{ADIM}	0.4	V _{REG}	V
External Synchronized Frequency Range ^(Note 4)	f _{SYNC}	Higher of 200 or f _{OSC} x 0.9	Lower of 700 or f _{OSC} x 1.1	kHz
External Synchronized Pulse Duty Range ^(Note 5)	f _{SDUTY}	40	60	%
LED Current Setting Range ^(Note 6)	I _{LED}	20	120	mA
Operating Temperature	Topr	-40	+125	°C

(Note 1) When IC is started, the voltage must be UVLO release voltage or more. Therefore, consider the power supply drop caused by the parasitic resistor and start the IC at VCC ≥ 5.5 V.

VCC(MIN) = 4.5 V is the minimum value of VCC that can operate the IC alone. The minimum value of power supply voltage that can be set depends on the connected LED load and external components.

(Note 2) Generally, flickering of LEDs is easier to see when the dimming frequency is set lower than 100 Hz. Set after confirming with the actual device evaluation.

(Note 3) Even if 1.21 V or more is input to the ADIM pin, it is fixed at 1.21 V inside the IC.

(Note 4) When the external synchronization function is not used, connect the SYNC pin to V_{REG} (SSCG = ON) or GND (SSCG = OFF).

(Note 5) When using the external synchronization function, switching from the external synchronization state to the internal oscillation frequency is not possible during stable operation.

(Note 6) The amount of current per channel. Set the LED current so that the maximum junction temperature (T_{Jmax}) is not exceeded.

Operating Conditions (External Constant Range)

Parameter	Symbol	Operating Range			Unit
		Min	Typ	Max	
REG Capacitance	C _{REG}	1.0	2.2	4.7	μF
LED Current Setting Resistor	R _{ISSET}	11	-	53	kΩ
Oscillation Frequency Setting Resistor	R _{RT}	4.6	-	51.0	kΩ
PLSET Capacitance	C _{PLSET}	-	-	10	nF
Input Capacitance 1	C _{VCC}	1 ^(Note 7)	-	-	μF
Input Capacitance 2	C _{INVCC} ^(Note 8)	10 ^(Note 7)	-	-	μF
Output Capacitance	C _{OUT}	20 ^(Note 7)	-	100	μF

(Note 7) Set the capacitance so that it does not fall below the minimum value in consideration of temperature characteristics, DC bias characteristics, etc.

(Note 8) C_{INVCC} means the total capacitance of C_{IN} and C_{VCC}.

Electrical Characteristics

(Unless otherwise specified, VCC = 12 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I _{CC}	-	-	10	mA	V _{EN} = 5 V, V _{SYNC} = 0 V, V _{PWM} = 0 V, C _{IN} = 10 μF, R _T = OPEN, I _{SET} = OPEN, V _{ADIM} = V _{REG} , Resistance between LEDn-GND = 10 kΩ
Standby Current	I _{ST}	-	0	10	μA	V _{EN} = Low
[VREF]						
Reference Voltage	V _{REG}	4.7	5.0	5.3	V	I _{REG} = -5 mA, C _{REG} = 2.2 μF
[DC/DC Converter]						
SW Pin ON Resistor	R _{ON_SW}	-	0.2	0.4	Ω	I _{SW} = 50 mA
LED Control Voltage	V _{LEDCTL}	0.66	0.76	0.86	V	R _{ISET} = 15.1 kΩ, V _{ADIM} = V _{REG}
COMP Sink Current	I _{COMPSINK}	150	220	290	μA	R _{ISET} = 15.1 kΩ, V _{COMP} = 1.0 V, V _{LED} = 1.5 V, V _{ADIM} = V _{REG}
COMP Source Current	I _{COMPSOURCE}	-290	-220	-150	μA	R _{ISET} = 15.1 kΩ, V _{COMP} = 1.0 V, V _{LED} = 0 V, V _{ADIM} = V _{REG}
Oscillation Frequency 1	f _{OSC1}	306	340	374	kHz	R _{RT} = 33.3 kΩ
Max Duty 1	D _{UTY_MAX1}	95	-	-	%	R _{RT} = 33.3 kΩ
Oscillation Frequency 2	f _{OSC2}	1980	2200	2420	kHz	R _{RT} = 4.6 kΩ
PLSET Charge Current	I _{PLSET}	35	50	65	μA	V _{PLSET} = 0 V
PLSET Set Voltage	V _{PLSET}	0.4	0.5	0.6	V	

Electrical Characteristics – continued

(Unless otherwise specified, VCC = 12 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
[Current Driver]						
LED Current Absolute Variation	I _{LEDn}	76.1	80.1	84.1	mA	R _{ISSET} = 15.1 kΩ, V _{ADIM} = V _{REG}
LED Current Relative Variation (Note 1)	I _{LEDREL}	0	-	5	%	R _{ISSET} = 15.1 kΩ, V _{ADIM} = V _{REG}
ISET-GND Short Protection Resistor	R _{ISSETLIM}	-	3.5	-	kΩ	V _{ADIM} = V _{REG}
ADIM Pin Input Current	I _{ADIM}	-1.0	0	+1.0	μA	V _{ADIM} = 5 V
PWM Dimming Minimum Pulse Width	t _{PWMMIN}	0.5	-	-	μs	f _{PWM} = 100 Hz to 25 kHz, I _{LED} = 80.1 mA
PWM Dimming Frequency	f _{PWM}	0.1	-	25.0	kHz	
PWM Low Section Detect Time	t _{PWML}	21.4	28.5	35.6	ms	
[Logic Input (EN)]						
Input High Voltage	V _{INH1}	2.1	-	-	V	
Input Low Voltage	V _{INL1}	-	-	0.5	V	
Input Resistor	R _{IN1}	50	100	150	kΩ	V _{EN} = 5 V
[Logic Input (PWM, SYNC)]						
Input High Voltage	V _{INH2}	2.1	-	-	V	
Input Low Voltage	V _{INL2}	-	-	0.5	V	
Input Resistor	R _{IN2}	50	100	150	kΩ	V _{PWM} = V _{SYNC} = 5 V

(Note 1) I_{LEDREL} = (I_{LEDn(MAX)} - I_{LEDn(MIN)}) / I_{LEDn(Ave)} × 100

Electrical Characteristics – continued

(Unless otherwise specified, VCC = 12 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
[PROTECT]						
VCCUVLO Detect Voltage	V _{UVLOVCC1}	3.90	4.10	4.30	V	VCC = Sweep down
VCCUVLO Release Voltage	V _{UVLOVCC2}	4.05	4.25	4.45	V	VCC = Sweep up
REGUVLO Detect Voltage	V _{UVLOREG1}	3.75	3.95	4.15	V	V _{REG} = Sweep down
REGUVLO Release Voltage	V _{UVLOREG2}	3.90	4.10	4.30	V	V _{REG} = Sweep up
OVP Detect Voltage	V _{OVPDET}	1.16	1.21	1.26	V	V _{OVP} = Sweep up
OVP Detect Voltage Hysteresis Width	V _{OVPHYS}	-	50	-	mV	V _{OVP} = Sweep down
Input OCP Detect Voltage	V _{OCPH}	80	100	120	mV	VCC-V _{C_{SH}} = Sweep up
LDSW Operation Voltage at Input OCP Release	V _{LDSW}	4.4	5.4	6.4	V	V _{C_{SH}} = VCC VCC-V _{LDSW}
OCPL Detect Current	I _{OCPL}	3.14	3.60	4.06	A	
LED Open Protection Detect Voltage	V _{OPEN}	0.1	0.2	0.3	V	V _{LED} = Sweep down V _{OVP} ≥ V _{OVPDET}
LED Anode SCP Detect Voltage	V _{SCP1}	0.05	0.10	0.15	V	V _{OVP} = Sweep down
LED Cathode SCP Detect Voltage	V _{SCP2}	0.1	0.2	0.3	V	V _{LED} = Sweep down
LED Anode SCP Detect Delay Time	t _{SCP1}	2.67	3.56	4.45	ms	
LED Cathode SCP Detect Delay Time	t _{SCP2}	2.67	3.56	4.45	ms	
LED Short Protection Detect Voltage	V _{SHORT}	4.7	5.0	5.3	V	V _{LED} = Sweep up
Initial Check Time	t _{INICK}	5.34	7.12	8.90	ms	
FAIL Pin ON Resistor	R _{FAIL}	-	1.0	2.0	kΩ	I _{FAIL} = 1 mA

Typical Performance Curves

(Reference data, unless otherwise specified VCC = 12 V)

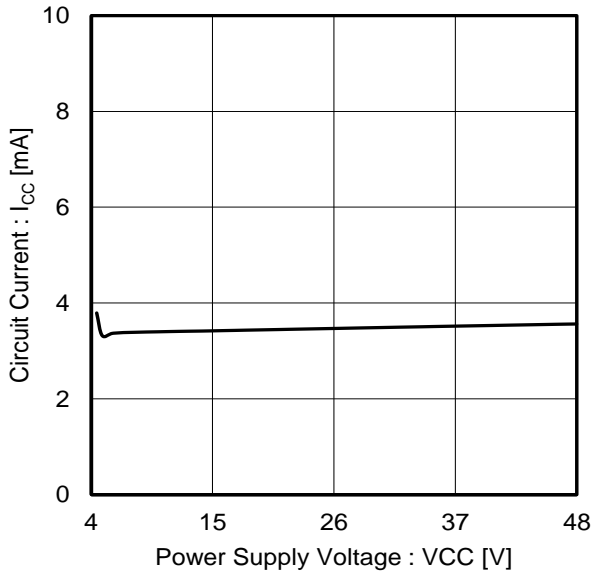


Figure 4. Circuit Current vs Power Supply Voltage

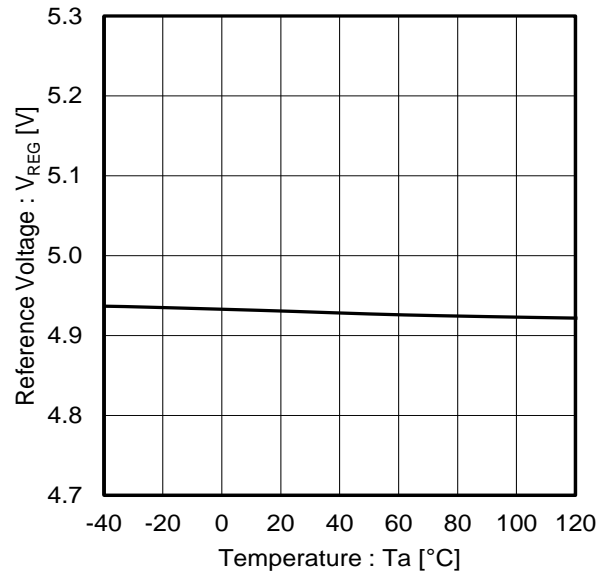


Figure 5. Reference Voltage vs Temperature

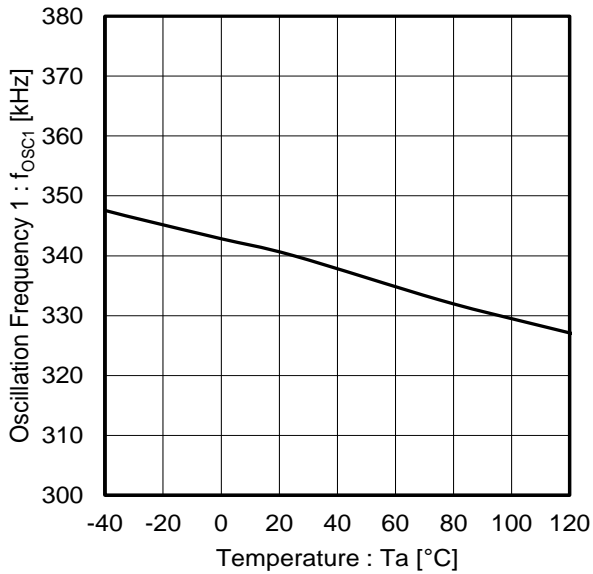


Figure 6. Oscillation Frequency 1 vs Temperature
($R_{RT} = 33.3 \text{ k}\Omega$)

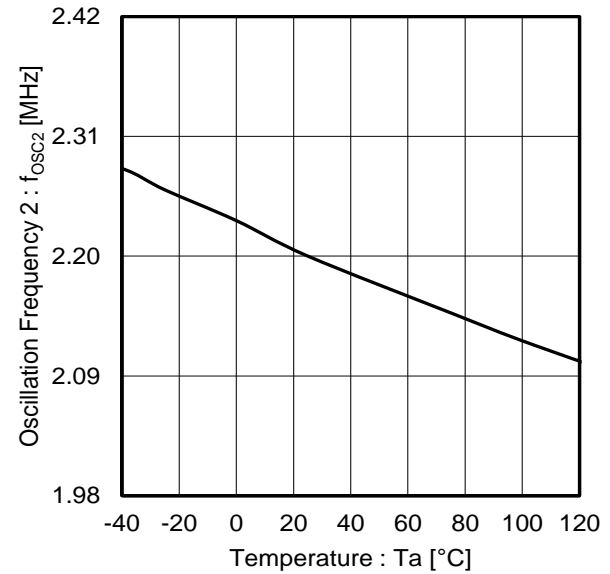


Figure 7. Oscillation Frequency 2 vs Temperature
($R_{RT} = 4.6 \text{ k}\Omega$)

Typical Performance Curves – continued
(Reference Data)

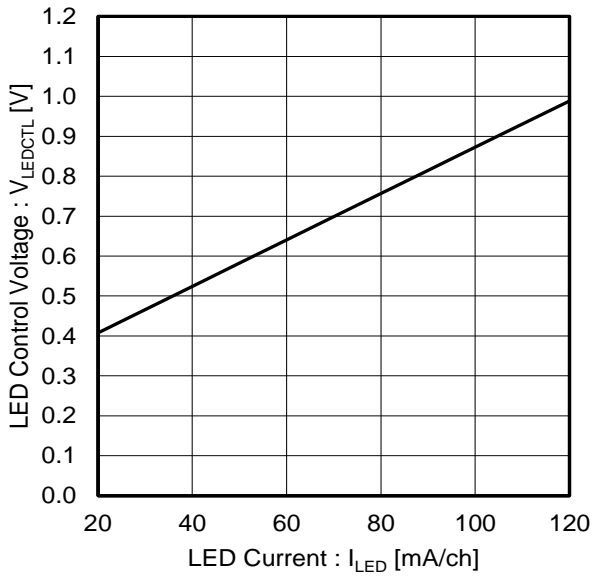


Figure 8. LED Control Voltage vs LED Current

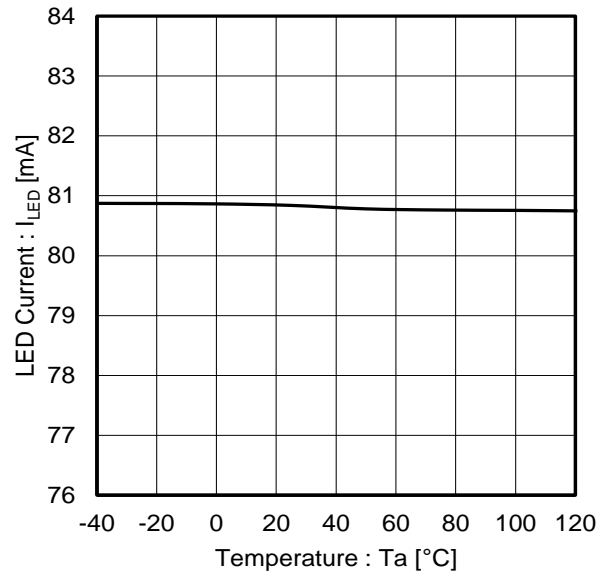


Figure 9. LED Current vs Temperature

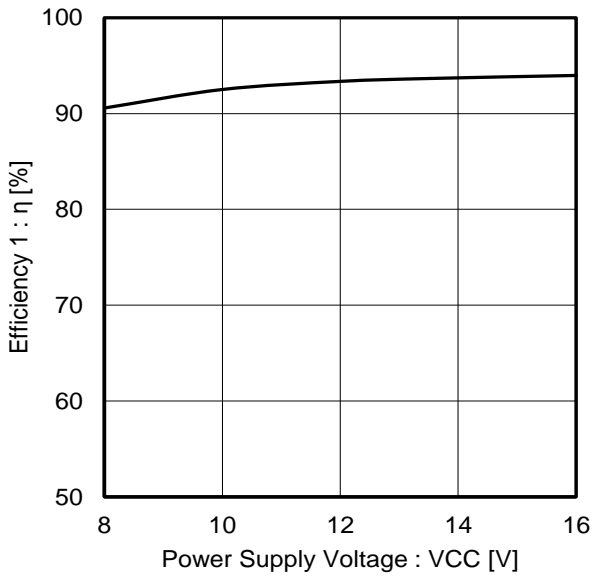


Figure 10. Efficiency 1 vs Power Supply Voltage
($R_{RT} = 33.3 \text{ k}\Omega$, $R_{SET} = 15.1 \text{ k}\Omega$,
Number of LED Series = 10, Number of LED Parallels = 4)

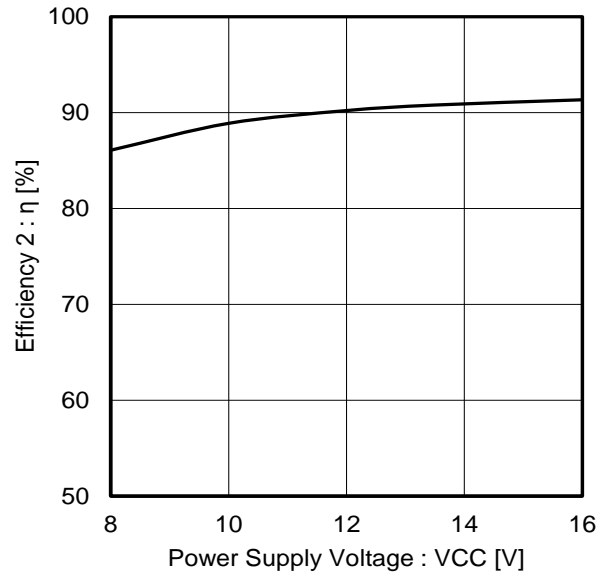


Figure 11. Efficiency 2 vs Power Supply Voltage
($R_{RT} = 4.6 \text{ k}\Omega$, $R_{SET} = 15.1 \text{ k}\Omega$,
Number of LED Series = 10, Number of LED Parallels = 4)

Function Descriptions

Unless otherwise stated, the value in the sentence is the Typ value.

1 Current Driver

This model has a built-in 4 ch current driver. The LED current setting range per channel is 20 mA to 120 mA, and the LED current can be adjusted by the resistance value between the ISET pin and GND.

[1.1 How to Set LED Current](#)

[1.2 When Using Analog Dimming](#)

[1.3 When Using PWM Dimming](#)

[1.4 PWM Low Section Detect Function](#)

[1.5 LED Pin Handling of Unused Channels](#)

[1.6 When Setting the LED Current Above 120 mA](#)

1.1 How to Set LED Current

The LED current I_{LED} can be calculated using the following equation.

$$I_{LED} = \frac{V_{ISET}}{R_{ISET}} \times 10^6 \quad [\text{mA}]$$

I_{LED} : Output current per channel (LED current)
(Recommended operating condition:
20 mA to 120 mA)

V_{ISET} : ISET pin voltage 1.21 V
(When ADIM pin voltage $V_{ADIM} = V_{REG}$)

R_{ISET} : LED current setting resistor
(Recommended operating condition:
11 kΩ to 53 kΩ)

Resistance Value Setting Example ($V_{ADIM} = V_{REG}$)

ISET Resistor [kΩ]	LED Current [mA]
53	22.8
30	40.3
15.1	80.1
11	110.0

When $R_{ISET} \leq 3.5 \text{ k}\Omega$, ISET pin short protection detect is activated and, output of the LED current is stopped.

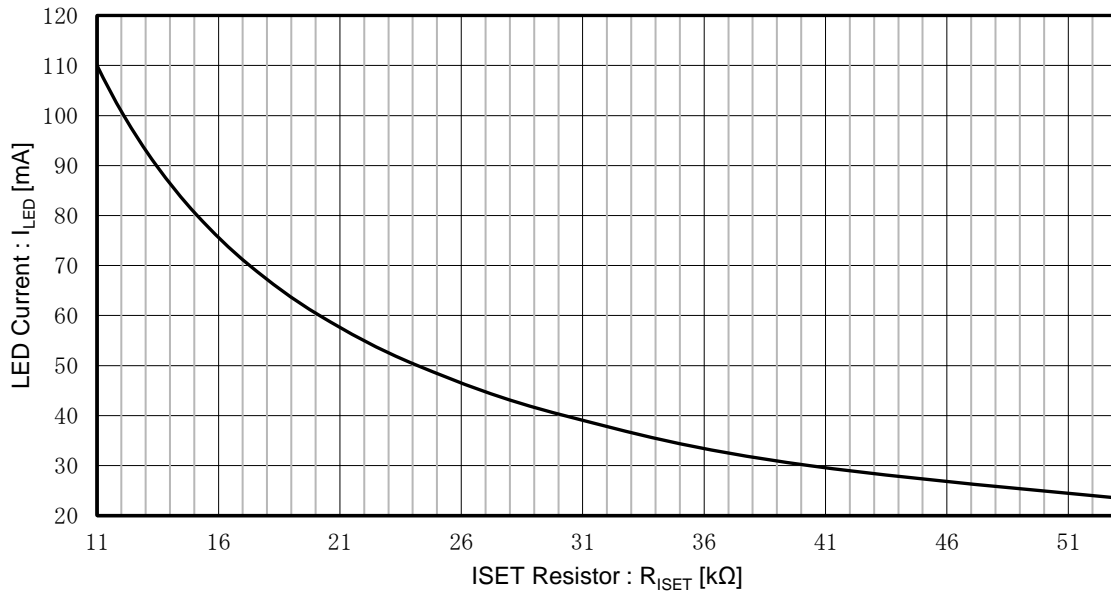


Figure 12. I_{LED} vs R_{ISET} ($V_{ADIM} = V_{REG}$)

1 Current Driver – continued

1.2 When Using Analog Dimming

ISET pin voltage can be adjusted according to the voltage input to the ADIM pin. The LED current I_{LED} can be calculated from the following equation as described above.

$$I_{LED} = \frac{V_{ISET}}{R_{ISET}} \times 10^6 \quad [\text{mA}]$$

However, V_{ISET} can be adjusted according to ADIM pin voltage V_{ADIM} as follows:

$$V_{ISET} = 1.21 \text{ [V]} \quad (1.21 \text{ V} \leq V_{ADIM} \leq V_{REG})$$

$$V_{ISET} = V_{ADIM} \text{ [V]} \quad (0.40 \text{ V} < V_{ADIM} < 1.21 \text{ V})$$

I_{LED}: Output current per channel (LED current)
(Recommended operating condition:
20 mA to 120 mA)

V_{ISET}: ISET pin voltage 1.21 V
(ADIM pin voltage V_{ADIM} = V_{REG})

R_{ISET}: LED current setting resistor
(Recommended operating conditions:
11 kΩ to 53 kΩ)

V_{ADIM}: ADIM pin Input voltage
(Recommended operating conditions:
0.40 V to V_{REG})

Note that I_{LED} set by R_{ISET} and V_{ADIM} can't be set to less than 20 mA.

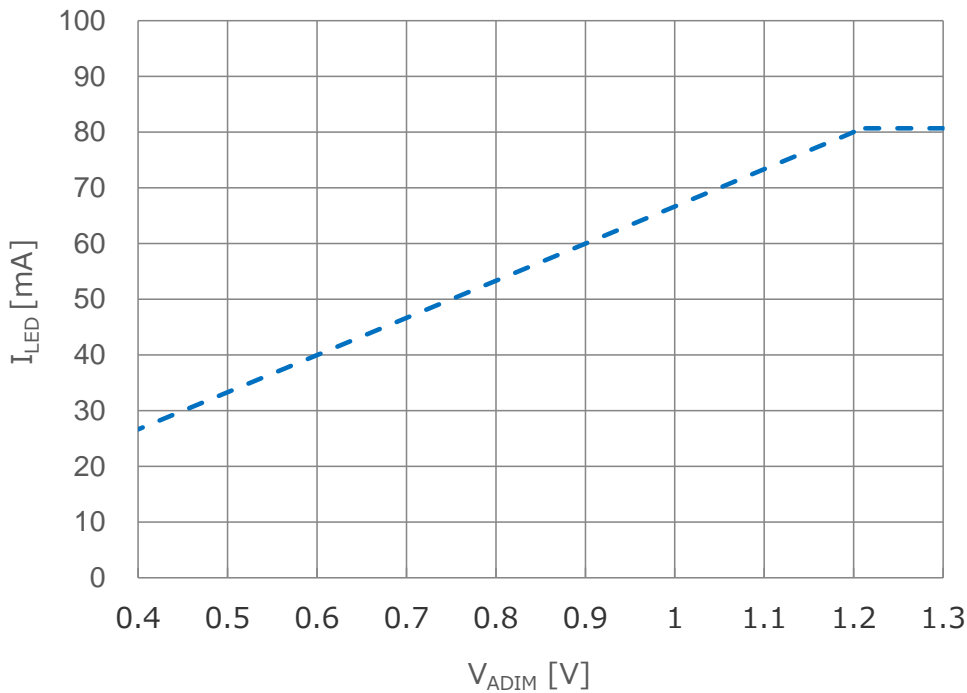


Figure 13. I_{LED} vs V_{ADIM} (R_{ISET} = 15.1 kΩ)

1.3 When Using PWM Dimming

The LED current can be controlled according to On Duty of the PWM signal input to the PWM pin. However, in the region where the ON time of the LED current is less than 0.5 μs or the OFF time is less than 0.5 μs, the pulse time is shorter than [PWM dimming minimum pulse width](#), so it cannot be used regularly. It is okay to use this region transiently, so it is also possible to set PWM Duty = 0 % and 100 %.

1 Current Driver – continued

1.4 PWM Low Section Detect Function

Counting starts when PWM = High is switched to Low in the V_{EN} = High state. When PWM Low section reaches 28.5 ms, the operation is regarded as OFF state. After that, when PWM input is turned High, switching operation (pre-boost) is restarted.

1.5 LED Pin Handling of Unused Channels

This model has four built-in constant current circuits. The current can be supplied to the LED by setting the PWM pin to High, and the LED current can be set by inserting a resistor between the ISET pin and GND. The LED current that can be supplied per row is 20 mA to 120 mA.

Pull down the LED pin of the unused channel to GND with 10 kΩ.

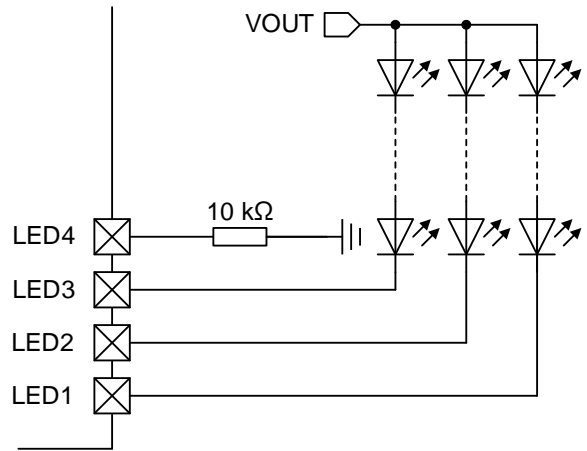


Figure 14. When Setting LED4 Unused

1.6 When Setting the LED Current Above 120 mA

The LED1 to LED4 pins can be used in bundles.

For example, as shown in the figure on the right, if LED1, LED2, LED3, and LED4 are shorted, 4 times the current set by the ISET pin can be passed.

When using only 2 channels in a bundle, mount a resistor for each LED pin for unused channels (2 channels).

When connected to multiple LED pins with a resistor, the voltage may deviate from the set value and may not be recognized as an unused channel. In this case, the unintentional protection function may be activated, so perform the LED pin handling correctly.

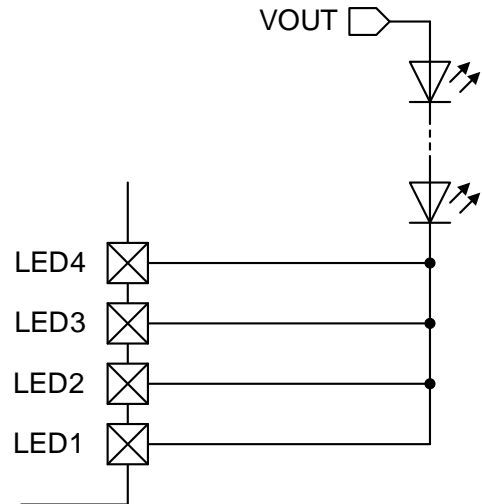


Figure 15. Application Example When LED Pins are Shorted

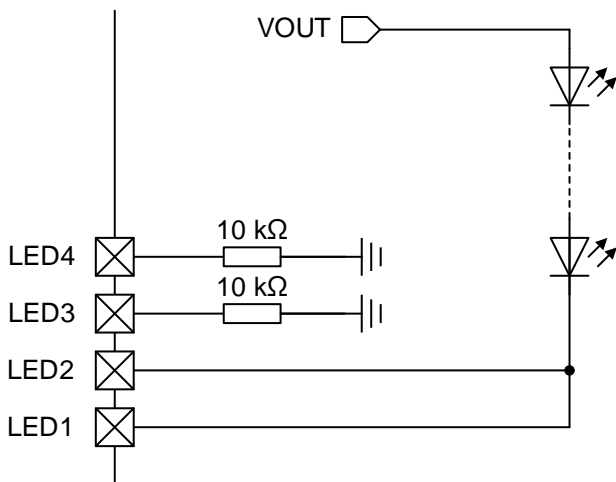


Figure 16. Correct LED Pin Handling When Multiple Channels are Unused

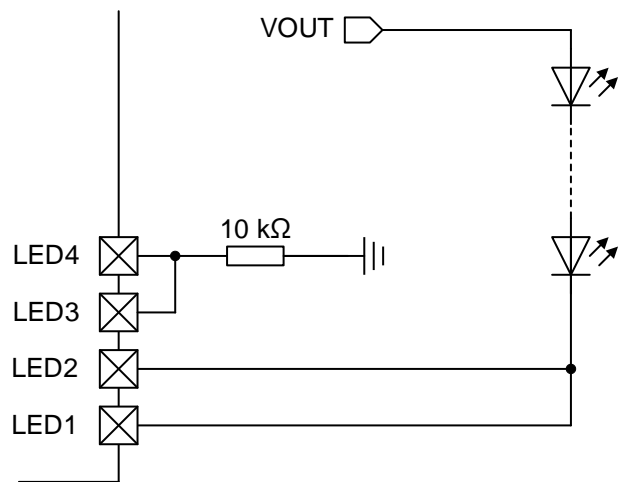


Figure 17. Wrong LED Pin Handling When Multiple Channels are Unused

Functional Descriptions – continued

Unless otherwise stated, the value in the sentence is the Typ value.

2 DC/DC Converter

Detects the lowest voltage among LED1 to LED4 pin voltages (LED cathode voltages) in Minimum Channel Selector block and inputs it to Error AMP. The reference voltage of Error AMP is generated in REF Voltage block based on R_{ISSET} resistance value, which becomes LED pin control voltage. The output of Error AMP is compared with the output of SLOPE block by PWM COMP block, and a switching signal is output to the SW pin through DC/DC Control LOGIC.

[2.1 LED Pin Control Voltage V_{LEDCTL}](#)

[2.2 VCC Input Voltage and Number of LED Series](#)

[2.3 LED Variation and Series Number](#)

[2.4 Overvoltage Protection Function OVP](#)

[2.5 DC/DC Converter Oscillation Frequency f_{osc}](#)

[2.6 Pulse Addition Function](#)

[2.7 External Synchronization / Spread Spectrum Function \(SSCG\)](#)

[2.8 LSDET Function](#)

2.1 LED Control Voltage V_{LEDCTL}

DC/DC converter operates so that the lowest voltage among LED1 to LED4 pin voltages (LED cathode voltages) is equal to the LED control voltage (V_{LEDCTL}). Power dissipation can be minimized by optimizing the LED control voltage (V_{LEDCTL}) according to the LED current (I_{LED}).

LED Control Voltage Reference Value (ADIM = REG)

ISET Resistor R _{ISSET} [kΩ]	LED Current I _{LED} [mA]	LED Control Voltage V _{LEDCTL} [V]
53	22.8	0.42
30	40.3	0.52
15.1	80.1	0.76
11	110.0	0.93

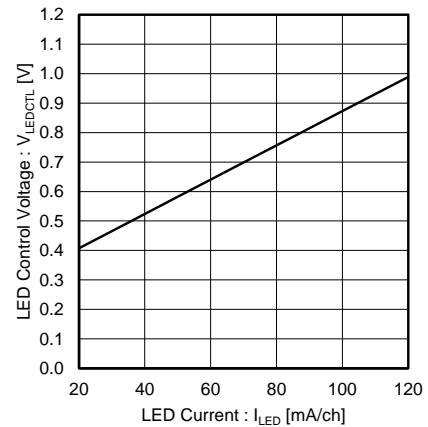


Figure 18. V_{LEDCTL} vs I_{LED}

2.2 VCC Input Voltage and Number of LED Series

To drive the boost DC/DC converter, the LED must be selected so that the output voltage (V_{OUT}) is higher than the input voltage (V_{CC}).

$$V_{CC(MAX)} < V_{OUT(MIN)}$$

$$V_{CC(MAX)} < V_{f(MIN)} \times N + V_{LEDCTL(MIN)}$$

- V_{CC} : Input voltage
- V_{OUT} : DC/DC converter output voltage
- N : Number of LED series
- V_f : LED Vf voltage
- V_{LEDCTL} : LED control voltage

Select the number of LED series and Vf characteristics that satisfy the above equation.

2.3 LED Variation and Series Number

When operating multiple LED outputs, the LED anode voltages in each row are commonly connected to DC/DC converter output V_{OUT}. LED pin voltage (LED cathode voltage) in the row where the Vf voltage of the LED is the highest is the lowest, and this is controlled to be V_{LEDCTL}. Therefore, the voltage of other LED pin outputs will be higher by the amount of Vf variation. Select the number of LED series and Vf characteristics so that the LED short protection (V_{LEDn} ≥ 5.0 V) does not operate.

$$N \times (V_{f(MAX)} - V_{f(MIN)}) < V_{SHORT(MIN)} - V_{LEDCTL(MAX)}$$

- V_{SHORT} : LED short protection voltage

2 DC/DC Converter – continued

2.4 Overvoltage Protection Function OVP

Inputs the resistor division of the output voltage VOUT in the OVP pin. When OVP pin voltage rises the overvoltage protection detect voltage V_{OVP} (1.21 V) or more, the overvoltage protection is activated, and the switching of DC/DC converter is turned OFF. After that when OVP pin voltage drops to 1.16 V, OVP is released.

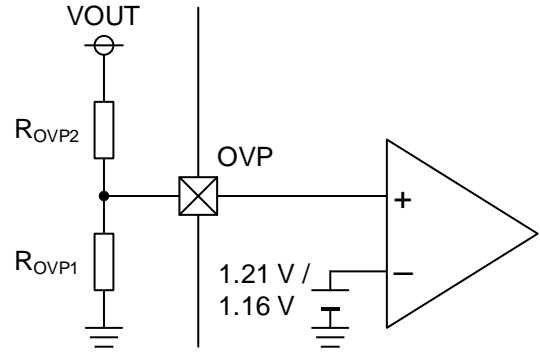


Figure 19. OVP Pin Voltage Setting Sample

$$VOUT_{OVP} = \{(R_{OVP1} + R_{OVP2}) / R_{OVP1}\} \times V_{OVP} \quad [V]$$

$VOUT_{OVP}$: DC/DC converter output voltage (VOUT) during overvoltage protection operation
 V_{OVP} : Overvoltage protection detect voltage

2.5 DC/DC Converter Oscillator Frequency f_{osc}

The oscillation frequency (f_{osc}) of DC/DC converter can be set by connecting R_{RT} between the RT pin and GND. The oscillator frequency of DC/DC converter is generated in the OSC block. Set the resistor of R_{RT} referring to the data and theoretical formula below.

$$f_{osc} = (1.132 \times 10^7 / R_{RT}) \times \alpha \quad [kHz]$$

f_{osc} : Oscillation frequency of DC/DC converter
 1.132×10^7 : Constants determined inside the circuit
 R_{RT} : RT pin connecting resistor
 α : Correction factor

α is the correction factor. For the relation between f_{osc} and R_{RT} including the correction factor, refer to f_{osc} vs R_{RT} below. Note that operation cannot be guaranteed if f_{osc} setting value exceeds the recommended range of 200 kHz to 2420 kHz. Determine f_{osc} setting value in consideration of the variation in electrical characteristics, variation in R_{RT} , and ON/OFF of spread spectrum

Example of Resistance Value for f_{osc} Setting

R_{RT} [k Ω]	α
51	1.013
33.3	1.000
20	0.980
10	0.947
4.6	0.894

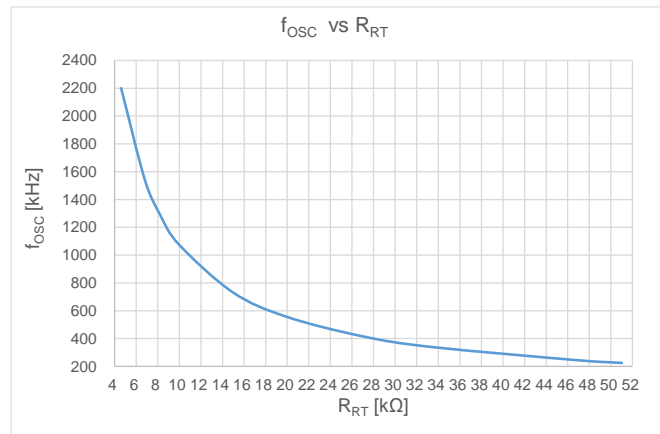


Figure 20. f_{osc} vs R_{RT}

2 DC/DC Converter – continued

2.6 Pulse Addition Function

A pulse addition function is provided to output a stable DC/DC converter output voltage and LED current even when PWM Duty is low. The output voltage can be held by outputting additional switching of several pulses after the falling edge of the PWM input signal, and the LED can be turned on normally. When the pulse addition function is not used, set the PLSET pin to OPEN

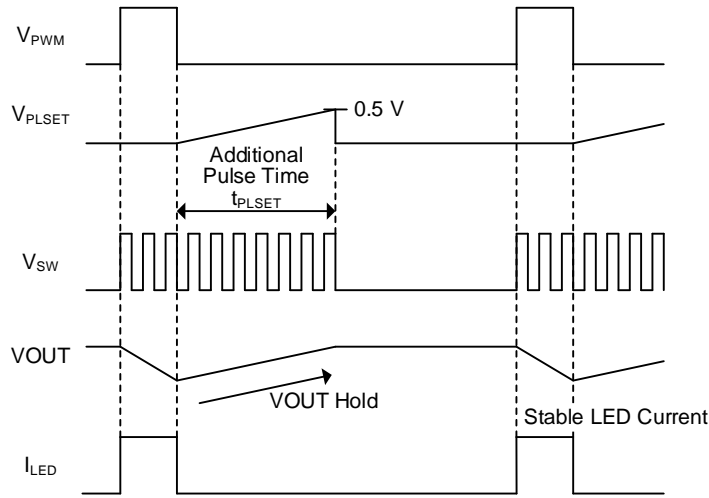


Figure 21. Pulse Addition Function

The number of additional switching pulses is set in the capacitance value C_{PLSET} connected to the PLSET pin. The additional pulse time t_{PLSET} is calculated as follows:

$$t_{PLSET} = 10^{10} \times C_{PLSET} \quad [\mu s]$$

t_{PLSET} : Additional pulse time
 C_{PLSET} : PLSET pin capacitance

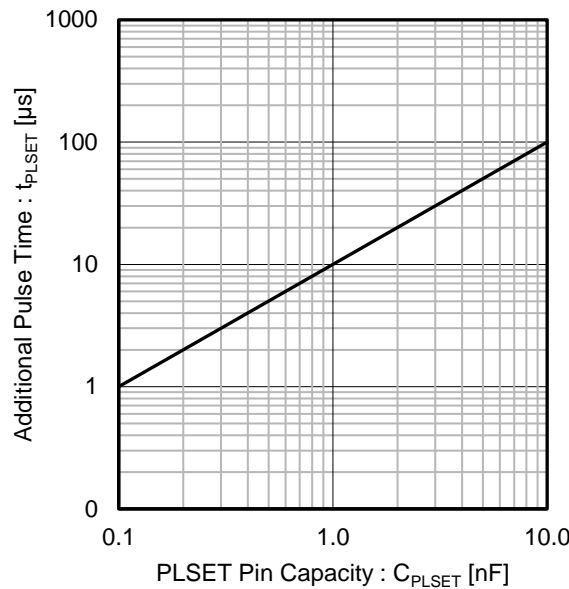


Figure 22. t_{PLSET} VS C_{PLSET}

The additional pulse time required to hold the output voltage V_{OUT} varies depending on various factors such as PWM frequency, output voltage, output capacitance, LED current, as well as the minimum value of PWM Duty used for dimming. Contact your sales representative when you request design verification of the required additional pulse time for your usage conditions.

2 DC/DC Converter – continued

2.7 External Synchronization /Spread Spectrum Function (SSCG)

Three switching modes can be selected according to the voltage input to the SYNC pin.

Mode	V _{SYNC}	DC/DC Switching Frequency
1	Low	Fixed Frequency Mode Determined by R _{RT}
2	High (= V _{REG})	Spread Spectrum Mode of the Frequency Determined by R _{RT}
3	Pulse Input	Mode to Synchronize with the Frequency Input to the SYNC Pin

Mode 1:

When the SYNC pin is fixed Low, DC/DC converter switches at [a fixed frequency determined by R_{RT}](#).

Mode 2:

By shorting the SYNC pin and the REG pin, operation in spread spectrum mode (SSCG) is enabled. With SSCG, noise peaks can be reduced by periodically changing the oscillation frequency. The fluctuation range (Δf) of the frequency due to SSCG is -8 % of the set oscillation frequency from the set oscillation frequency. The oscillation frequency fluctuation period (t_{SSCG}) is 1/(2.3 kHz).

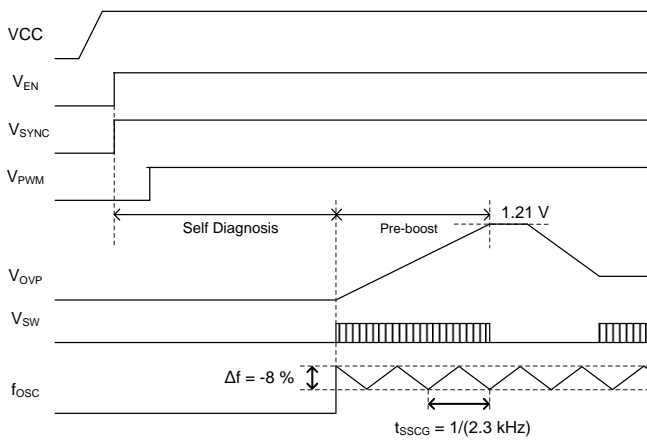


Figure 23. Spread Spectrum Function Timing Chart

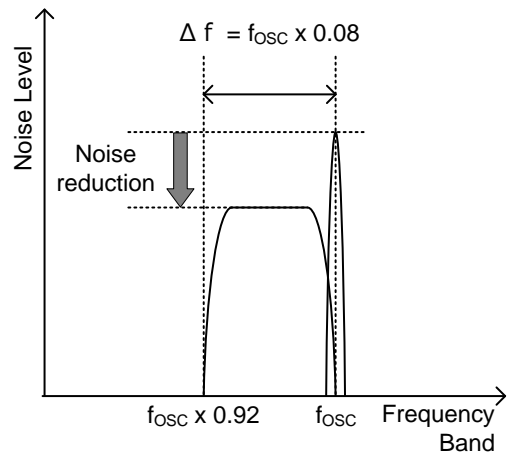


Figure 24. Spread Spectrum Function

$$\Delta f = f_{OSC} \times 0.08$$

$$t_{SSCG} = 1/(2.3 \text{ kHz})$$

Δf : Fluctuation range of the oscillation frequency by SSCG

f_{OSC} : DC/DC oscillation frequency

t_{SSCG} : The oscillation frequency fluctuation period by SSCG

When not using SSCG function, short the SYNC pin and the GND pin. SSCG function cannot be turned ON/OFF during operation.

2.7 External Synchronization / Spread Spectrum Function (SSCG) – continued

Mode 3:

By inputting an external clock signal to the SYNC pin, the internal oscillation frequency can be externally synchronized. However, note the following points.

- Since Mode is judged during [Self Diagnosis \(Initial Check\)](#), input the clock signal to the SYNC pin prior to turning the EN pin to High.
- After the clock signal is input to the SYNC pin and the EN pin is turned High, it is not possible to switch between internal oscillation and external synchronization. Operation may become unstable. Similarly, after turning the EN pin to High, the frequency of external synchronization cannot be switched.
- When using the external synchronization function, connect an RC filter with a cutoff frequency equivalent to the input external synchronization frequency to the SYNC terminal as a countermeasure against interference with the RT terminal. Be sure to check whether the output voltage of the RC filter satisfies the input threshold of the SYNC pin.
- When using external synchronization, SSCG cannot be used.
- For the external synchronization frequency, input a frequency within $\pm 10\%$ of the theoretical value of the oscillation frequency f_{OSC} set by the RT pin.

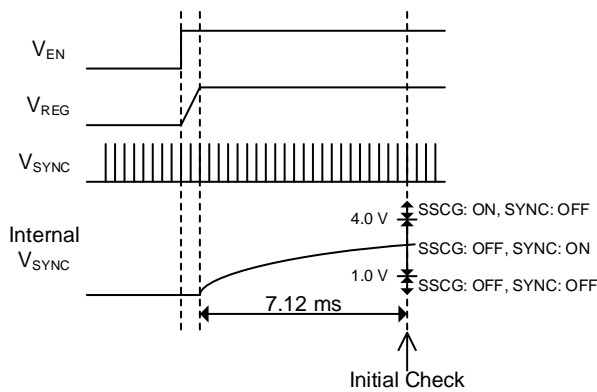


Figure 25. Synchronous Signal (V_{SYNC}) Input and Mode Check (Initial Check) Timing

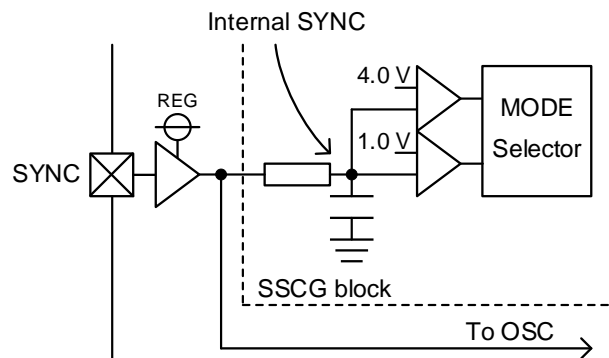


Figure 26. SYNC Pin Equivalence Circuit

2.8 LSDET Function

When the lowest LED pin voltage among LED pins is 2.4 V or more, DC/DC converter is turned OFF, and COMP voltage is held. DC/DC converter resumes switching when the lowest LED pin voltage is less than $V_{LEDCTL} \times 1.2$. LSDET function is intended to reduce the voltage quickly when the output is over boosted. It also prevents the LEDs from flickering by resuming the switching of DC/DC converter just before returning to normal operation.

- ① The LED4 pin becomes open and LED4 pin voltage becomes 0.2 V or less (A). DC/DC converter output begins boosting further to raise LED4 pin voltage. In conjunction with this, OVP pin voltage also rises (B).
- ② When OVP pin voltage reaches 1.21 V (C) due to the boost of DC/DC converter, the LED open protection is activated. When the LED open protection is activated, the LED4 pin that was open is pulled up to REG pin voltage V_{REG} inside the IC (D). LSDET function operates because LED4 pin voltage, which is the lowest LED pin voltage in the LED pins, is 2.4 V or more (D). LSDET function turns OFF DC/DC converters and holds COMP voltage (E).
- ③ DC/DC converter turns OFF, the output voltage drops, and OVP pin voltage also drops (F).
- ④ When the lowest LED pin voltage is less than $V_{LEDCTL} \times 1.2$ (G), DC/DC converter resumes switching (H).

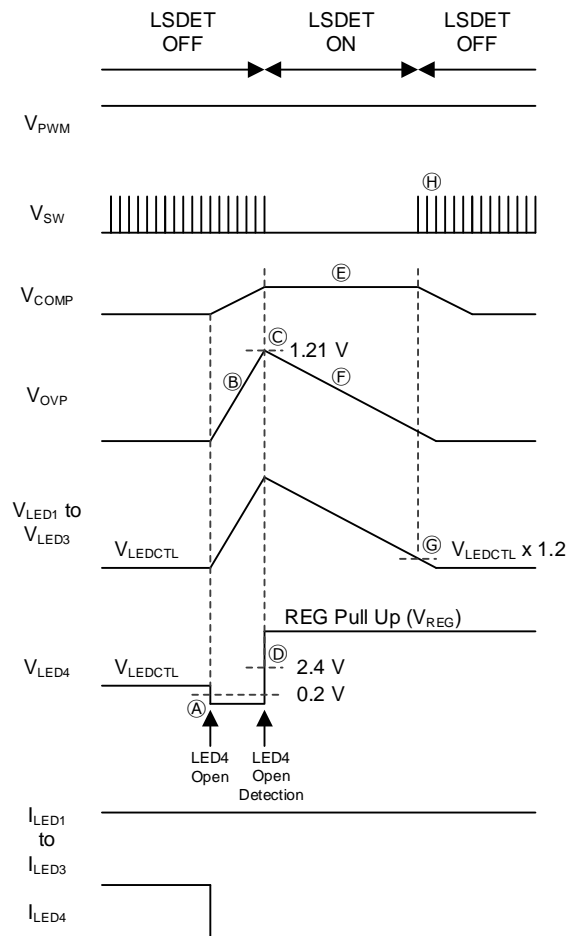


Figure 27. LSDET Function When LEDs are Open

Functional Descriptions – continued

Unless otherwise stated, the value in the sentence is the Typ value.

3 Starting Sequence and Effective Section of Each Protection Function

The timing chart at startup and the effective section of each protection function are shown in the figure below.

- ① Power ON : Input EN voltage after the VCC voltage is input.
- ② Self Diagnosis (Initial check) : After inputting EN voltage, this IC becomes the Self Diagnosis status, determines the channel to be used, and sets the external synchronization / spread spectrum function, etc. Self Diagnosis is completed after 7.12 ms, and the diagnostic status is latched.
- ③ Pre-boost : After Self Diagnosis, pre-boost starts at $V_{PWM} = \text{High}$, and after 7.12 ms, pre-boost is completed.
- ④ Stable operation transition section : The LED current flows according to On Duty of the PWM signal input to the PWM pin. The output voltage of DC/DC converter with switching turned OFF drops according to the load current.
- ⑤ Stable state : When LED voltage (the lowest voltage in LED1 to LED4) drops to LED control voltage x 1.2, DC/DC converter switches again.

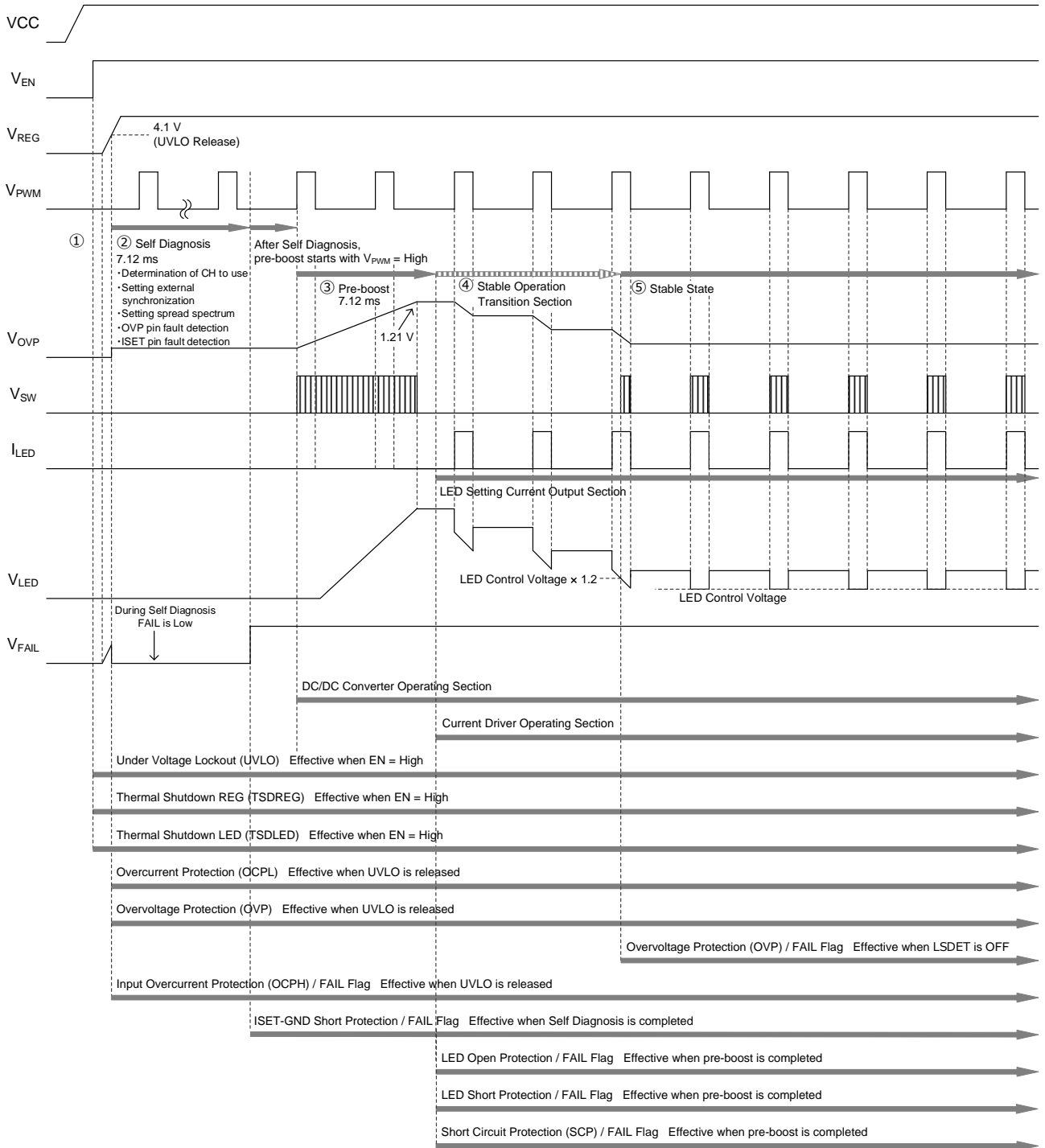


Figure 28. Timing Chart at Startup and Effective Section of Each Protection Function

3 Starting Sequence and Effective Section of Each Protection Function – continued

Unless otherwise stated, the value in the sentence is the Typ value.

3.1 Self Diagnosis (Initial Check)

The contents of Self Diagnosis are as follows.

3.1.1 LED Pin Used/Unused Check

It is possible to check whether the LED pin is used or not by LED pin voltage at the end of Self Diagnosis. If LED pin voltage is 0.2 V or more and 2.0 V or less during Self Diagnosis, the LED pin is diagnosed as unused. If it is diagnosed as unused, the LED pin does not operate and is pulled up to REG pin voltage V_{REG} inside the IC. To select unused channels correctly, the capacitance value to be connected to the LED pin should be 470 pF or less.

3.1.2 SYNC Pin Setting Check

[ON/OFF of the external synchronization or spread spectrum function can be set](#) by SYNC pin voltage at the end of Self Diagnosis.

3.1.3 FAIL Pin Connection Check

During Self Diagnosis, the FAIL pin can check the connection between the monitor pin of MCU and the FAIL pin by turning ON the open drain output (ON resistor = 1 k Ω). Determine the pull up voltage and pull up resistor according to FAIL detection voltage on the MCU. Also, be careful of startup failure when starting by pulling up to the external power supply, not REG pin voltage. The pull up resistor must satisfy the following conditions.

Pull Up Voltage (V)	Example of External Power Supply		REG Pin Voltage
	5.0	3.3	
Minimum Value of Pull Up Resistor (k Ω)	20	10	10

3.1.4 ISET-GND Short Check

In Self Diagnosis, ISET-GND Short Check is done under the same conditions as [ISET pin fault \(ISET-GND short protection\)](#). When ISET-GND short is confirmed, the load switch, DC/DC switching, and current driver are latched OFF. It is reset when V_{EN} = Low or UVLO is detected.

3.1.5 OVP Pin Setting Check

Self Diagnosis checks OVP pin setting. The OVP pin during Self Diagnosis is pulled down with IC built-in resistor of 1 M Ω . When an open failure of the OVP pin occurs, OVP pin voltage falls to 0.1 V or less, and the load switch, DC/DC switching, and the current driver latch OFF. It is reset when V_{EN} = Low or UVLO is detected.

Functional Descriptions – continued

4 Stopping Sequence and Effective Section of Each Protection Function

The figure below shows the timing chart when stopping and the effective section of each protection function.

- ⑤ Stable state : When LED voltage (the lowest voltage in LED1 to LED4) drops to the LED control voltage x 1.2, DC/DC converter is switched again.
- ⑥ Standby state : Decrease EN voltage prior to the VCC voltage falling. Internal circuit is stopped by falling EN voltage, and IC is in standby state.

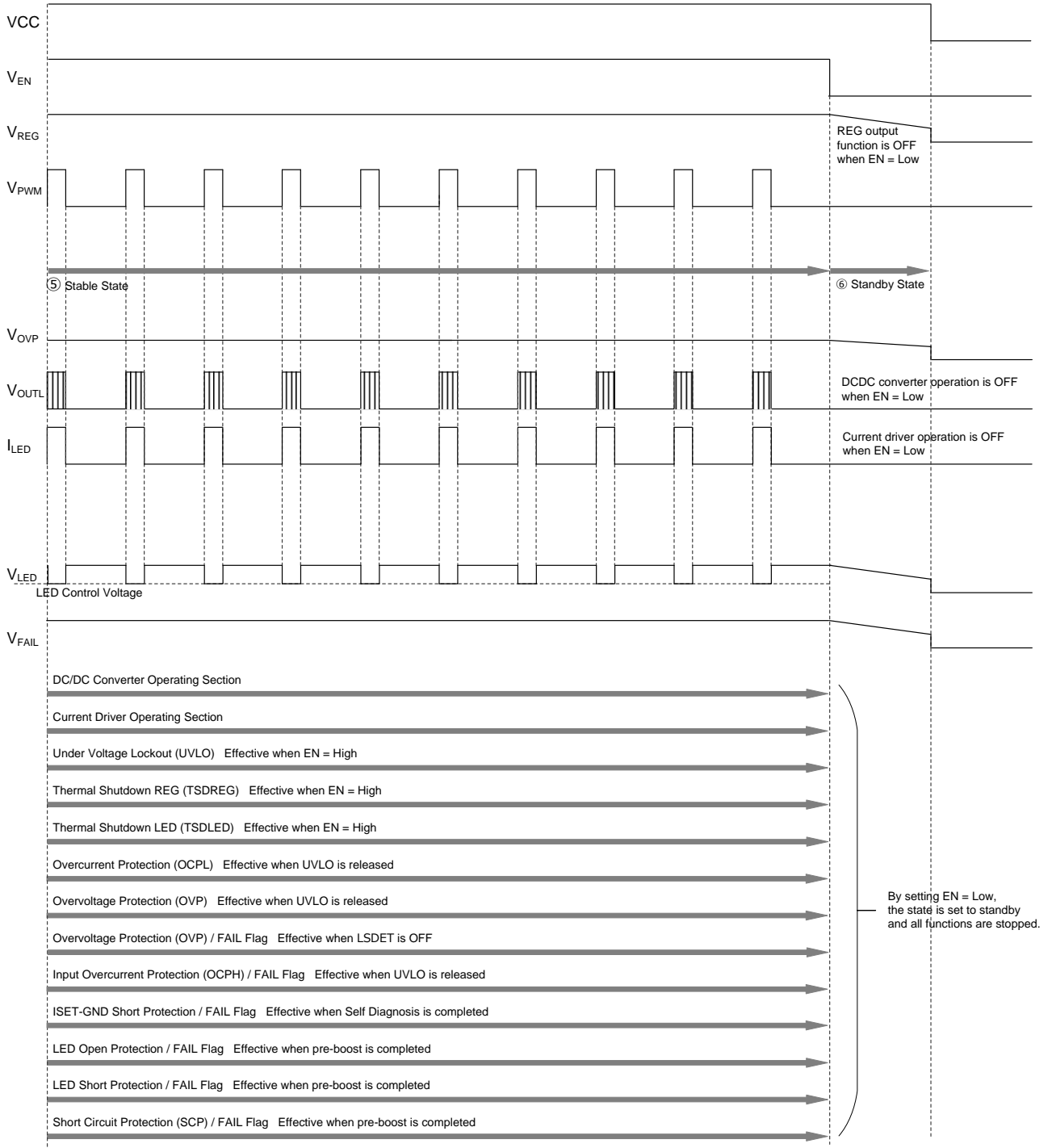


Figure 29. Timing Chart at Stopping and Effective Section of Each Protection Function

PCB Application Circuit Diagram

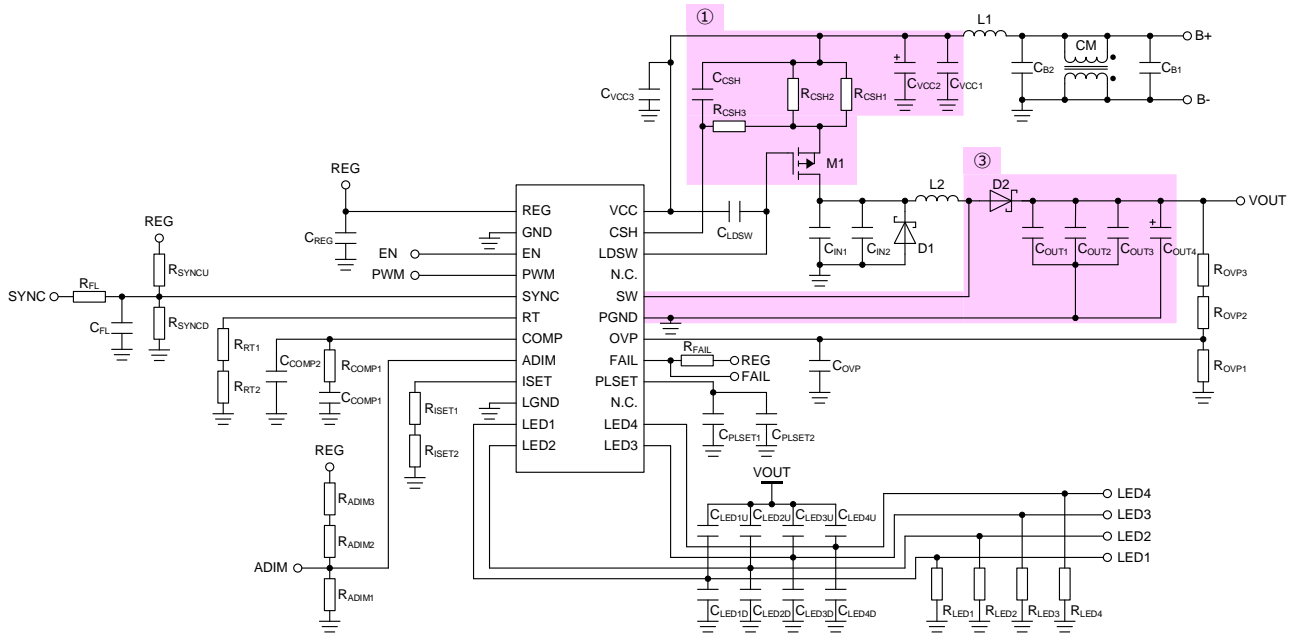


Figure 30. PCB Application Circuit Diagram

- ① Place the current detect resistor R_{CSH1} , R_{CSH2} , VCC pin capacitors C_{VCC1} , C_{VCC2} , and the load switch M1 so that they are shortest. Also, place the input filters R_{CSH3} , C_{CSH} for detecting the input current close to the CSH pin (pin 23). They can be placed on the opposite side of the IC and connected with a via.
- ② Place the input capacitors C_{IN1} , C_{IN2} and the Diode D1 so that they are as short as the components of both the inductor L2 and the load switch M1. Connect the ground of C_{IN1} , C_{IN2} , D1 to the PGND pin via EXP-PAD on the surface layer
- ③ To reduce high frequency noises, the wires of the boost "Loop" must be as short as possible. Do not widen the wiring width more than necessary.
 - Place the SW pin (pin 20), the inductor L2 and the anodes of the diode D2 so that they are the shortest.
 - Place the cathode of D2 and the output decoupling capacitors C_{OUT1} , C_{OUT2} , C_{OUT3} , and C_{OUT4} so that they are the shortest.
 - Place the output decoupling capacitors C_{OUT1} , C_{OUT2} , C_{OUT3} , C_{OUT4} and the PGND pin (pin 19) so that they are the shortest.
 - Place the IC and each component on the same surface layer of the board and make connections in the same layer.
- ④ Place the ground plane on the layer closest to the surface layer where the IC is placed.
- ⑤ Connect the EXP-PAD to the board ground. Wire the ground pattern connected from the EXP-PAD as wide as possible to improve heat dissipation and connect it to the ground plane with many vias. To ensure heat dissipation according to power loss, place the required number of thermal vias directly under the EXP-PAD and connect them to the ground plane.
- ⑥ There is no problem if the GND pin (pin 2), the LGND pin (pin 10) and the PGND pin (pin 19) are connected via the EXP-PAD. However, the power system ground such as the ground of the output decoupling capacitor and the PGND pin contains the noise component of the switching frequency. To reduce this noise component, it is recommended to connect to the ground plane using many vias in the ground pattern around the power system ground.
- ⑦ Place the bypass capacitor (C_{REG}) between the REG pin (pin 1) and the GND pin as close to pin as possible.
- ⑧ The connection from VOUT to the anode of the LED panel and the connection from the cathode of the LED panel to the LED1, LED2, LED3, LED4 pins should be as short as possible. Depending on the parasitic inductance component, the LED current may become unstable.
- ⑨ Do not run the wiring from the cathode of the LED panel to the LED1, LED2, LED3, LED4 pins in parallel with other active lines. Also, place the noise reduction capacitors (C_{LED1D} , C_{LED2D} , C_{LED3D} , C_{LED4D}) so that they are as short as the LED pin. R_{LED1} , R_{LED2} , R_{LED3} , R_{LED4} are pull-down resistors connected to the LED pin of unused channel and is required to generate LED pin voltage that is judged to be unused.
- ⑩ When using the PWM function, the PWM pin (pin 4) is the active line, so keep it away from other sense lines.
- ⑪ When using the external synchronization function, the SYNC pin (pin 5) is an active line, so keep it away from other sense lines. Also, when using the external synchronization function, connect an RC filter with a cutoff frequency equivalent to the input external synchronization frequency to the SYNC terminal as a countermeasure against interference with the RT terminal. Be sure to check whether the output voltage of the RC filter satisfies the input threshold of the SYNC pin.
- ⑫ Place R and C connected to the RT pin (pin 6), the COMP pin (pin 7), the ADIM pin (pin 8), the ISET pin (pin 9), the PLSET pin (pin 16), and the OVP pin (pin 18) as close to the IC as possible. They can be placed on the opposite side of the IC and connected with a via.
- ⑬ Since OVP pin voltage must be 0.1 V or more during Self Diagnosis, when installing the C_{OVP} , use about 1000 pF as a guide.
- ⑭ When the VCC voltage is turned ON with setting the EN pin to Low,, the voltage between the VCC-LDSW pins may open momentarily and an inrush current may flow depending on the VCC startup speed and the type of load switch (M1) used. Be sure to check with the actual application.

List of External Components

Serial No.	Component Name	Component Value	Product Name	Manufacturer
1	C _{B1}	-	-	-
2	CM	Short	-	-
3	C _{B2}	-	-	-
4	L1	Short	-	-
5	C _{VCC1}	1 μF	GCM21BR71H105KA03	murata
6	C _{VCC2}	-	-	-
7	C _{VCC3}	1 μF	GCM21BR71H105KA03	murata
8	R _{C_{SH1}}	15 mΩ	LTR18 Series	Rohm
9	R _{C_{SH2}}	-	-	-
10	R _{C_{SH3}}	100 Ω	MCR03 Series	Rohm
11	C _{CSH}	100 pF	GCM1882C1H101JA01	murata
12	C _{LDSW}	-	-	-
13	M1	60 V / 36 A	SQJ457EP	VISHAY
14	C _{IN1}	10 μF	GCM32EC71H106KA03L	murata
15	C _{IN2}	10 μF	GCM32EC71H106KA03L	murata
16	D1	60 V / 1 A	RBR1MM60ATF	Rohm
17	L2	22 μH	CLF10060NIT-220M-D	TDK
18	D2	60 V / 5 A	RB088LAM-60TF	Rohm
19	C _{OUT1}	10 μF	GCM32EC71H106KA03L	murata
20	C _{OUT2}	10 μF	GCM32EC71H106KA03L	murata
21	C _{OUT3}	-	-	-
22	C _{OUT4}	33 μF	GYA1H330MCQ1GS	nichicon
23	R _{OVP1}	10 kΩ	MCR03 Series	Rohm
24	R _{OVP2}	330 kΩ	MCR03 Series	Rohm
25	R _{OVP3}	Short	-	-
26	C _{OVP}	1000 pF	GCM1882C1H102JA01	murata
27	R _{FAIL}	100 kΩ	MCR03 Series	Rohm
28	C _{PLSET1}	1000 pF	GCM1882C1H102JA01	murata
29	C _{PLSET2}	-	-	-
30	R _{LED1}	-	-	-
31	R _{LED2}	-	-	-
32	R _{LED3}	-	-	-
33	R _{LED4}	-	-	-
34	C _{LED1U}	-	-	-
35	C _{LED2U}	-	-	-
36	C _{LED3U}	-	-	-
37	C _{LED4U}	-	-	-
38	C _{LED1D}	-	-	-
39	C _{LED2D}	-	-	-
40	C _{LED3D}	-	-	-
41	C _{LED4D}	-	-	-

List of External Components – continued

Serial No.	Component Name	Component Value	Product Name	Manufacturer
42	C _{REG}	2.2 μ F	GCM21BR71C225KA49	murata
43	R _{FL}	-	-	-
44	C _{FL}	-	-	-
45	R _{SYNCU}	-	-	-
46	R _{SYNCD}	100 k Ω	MCR03 Series	Rohm
47	R _{RT1}	33 k Ω	MCR03 Series	Rohm
48	R _{RT2}	Short	-	-
49	R _{COMP1}	200 Ω	MCR03 Series	Rohm
50	C _{COMP1}	0.1 μ F	GCM155R11C104KA40D	Murata
51	C _{COMP2}	-	-	-
52	R _{ISSET1}	15 k Ω	MCR03 Series	Rohm
53	R _{ISSET2}	Short	-	-
54	R _{ADIM1}	100 k Ω	MCR03 Series	Rohm
55	R _{ADIM2}	Short	-	-
56	R _{ADIM3}	-	-	-

Note: The component constants vary depending on the operating conditions and the load used.

Application Components Selection Method

Unless otherwise stated, the values in sentences are the values in continuous mode.
 Select the application components according to the following procedure.

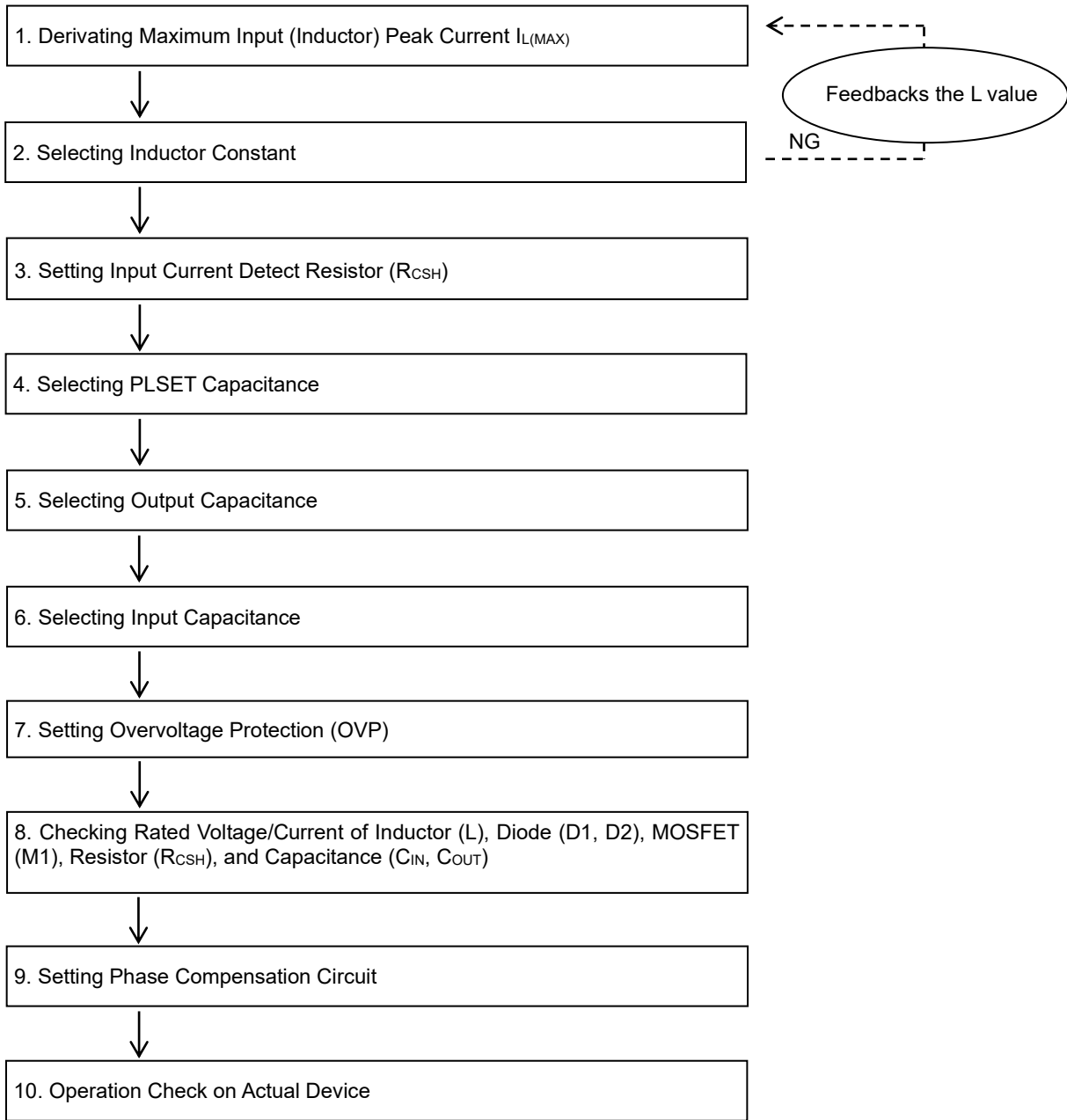


Figure 31. Application Components Selection Procedure

Application Components Selection Method – continued

1 Derivating Maximum Input (Inductor) Peak Current $I_{L(MAX)}$

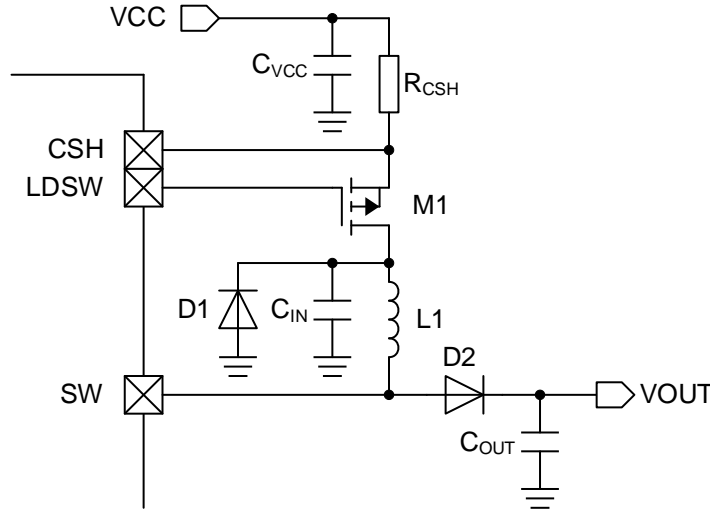


Figure 32. Output Application Circuit Diagram

1.1 Calculating Maximum Output Voltage $V_{OUT(MAX)}$

Calculates $V_{OUT(MAX)}$ in consideration of LED Vf variation and the number of LED stages.

$$V_{OUT(MAX)} = V_{f(MAX)} \times N + V_{LEDCTL(MAX)}$$

- $V_{OUT(MAX)}$: Maximum output voltage
- $V_{f(MAX)}$: Maximum value of LED Vf voltage
- N : Number of LED series
- $V_{LEDCTL(MAX)}$: Maximum value of LED control voltage

1.2 Calculating Maximum Output Current $I_{OUT(MAX)}$

$$I_{OUT(MAX)} = I_{LED(MAX)} \times M$$

- $I_{OUT(MAX)}$: Maximum output current
- $I_{LED(MAX)}$: Maximum value of LED current per channel
- M : Number of LED parallels

1.3 Calculating Maximum Input (Inductor) Peak Current $I_{L(MAX)}$

$$I_{L(MAX)} = I_{LAVG(MAX)} + \frac{1}{2} \Delta I_{L(MAX)}$$

$$\left[\begin{aligned} I_{LAVG(MAX)} &= V_{OUT(MAX)} \times \frac{I_{OUT(MAX)}}{\eta \times V_{CC(MIN)}} \\ \Delta I_{L(MAX)} &= \frac{V_{CC(MIN)}}{L_{(MIN)}} \times \frac{1}{f_{OSC(MIN)}} \times \frac{V_{OUT(MAX)} - V_{CC(MIN)}}{V_{OUT(MAX)}} \end{aligned} \right.$$

- $I_{L(MAX)}$: Maximum input (inductor) peak current
- $I_{LAVG(MAX)}$: Maximum input (inductor) average current
- $\Delta I_{L(MAX)}$: Maximum input (inductor) current amplitude
- $V_{CC(MIN)}$: Minimum power supply voltage
- η : Efficiency (about. 85 %)
- $L_{(MIN)}$: Minimum value of inductance
- $f_{OSC(MIN)}$: Minimum value of DC/DC oscillator frequency

Application Components Selection Method – continued

2 Selecting Inductor Constant

To maintain stable continuous operation of the current mode DC/DC converter, the L (inductance) value must satisfy the following requirements:

$$\frac{V_{OUT}-V_{CC}}{L \times 10^6} \leq \frac{153.3k}{R_{RT}}$$

V_{OUT} : Output voltage
 V_{CC} : Power supply voltage
 L : Inductance value
 R_{RT} : RT pin connecting resistor

Rewriting about L is as follows

$$L \geq \frac{(V_{OUT}-V_{CC}) \times R_{RT}}{153.3k \times 10^6}$$

Consider the variation of the L value and set it with sufficient margin.

3 Setting Input Current Detect Resistor (R_{CSH})

$$I_{OCPH(MIN)} = \frac{V_{OCPH(MIN)}}{R_{CSH(MAX)}} > 4.06A + \frac{V_{CC(MAX)}}{L(MIN)} \times t_{OCPL}$$

$I_{OCPH(MIN)}$: Minimum value of input overcurrent protection detect current
 $V_{OCPH(MIN)}$: Minimum value of input overcurrent protection detect voltage
 $R_{CSH(MAX)}$: Maximum value of input current detect resistor
 t_{OCPL} : OCPL detect delay time (MAX = 150 ns)

Select the R_{CSH} value so that it will be as above.

4 Selecting PLSET Capacitance

$$I_{OFFLOAD(MAX)} = \frac{V_{OUT(MAX)}}{R_{OVP(MIN)}} + I_{SBD(MAX)}$$

$$Q_{OFFLOSS(MAX)} = I_{OFFLOAD(MAX)} \times t_{PWMOFF(MAX)}$$

$$Q_{PWMRISE} = \frac{2.5}{f_{OSC(MIN)}} \times I_{OUT(MIN)}$$

$$Q_{PLSET(MIN)} = \frac{V_{PLSET(MIN)} \times C_{PLSET(MIN)}}{I_{PLSET(MAX)}} \times I_{OUT(MIN)}$$

$$Q_{PLSET(MIN)} > Q_{OFFLOSS(MAX)} + Q_{PWMRISE}$$

Select the C_{PLSET} value so that it will be as above.

$I_{OFFLOAD(MAX)}$: Maximum value of load current when PWM = OFF
 $R_{OVP(MIN)}$: Minimum value of overvoltage protection detect resistor
 $I_{SBD(MAX)}$: Maximum value of rectifier diode leakage current
 $Q_{OFFLOSS(MAX)}$: Maximum value of consumed charge when PWM = OFF
 $t_{PWMOFF(MAX)}$: Maximum value of PWM = OFF time
 $Q_{PWMRISE}$: Insufficient charge after PWM rise
 $Q_{PLSET(MIN)}$: Minimum value of additional pulse output supply charge
 $V_{PLSET(MIN)}$: Minimum value of PLSET threshold voltage
 $C_{PLSET(MIN)}$: Minimum value of PLSET pin capacitance
 $I_{PLSET(MAX)}$: Maximum value of PLSET charging current
 $I_{OUT(MIN)}$: Minimum output current

Application Components Selection Method – continued

5 Selecting Output Capacitance

The capacitor C_{OUT} used for the output is determined by the allowable amount of V_{OUTPP} which is the ripple voltage of V_{OUT} .

$$V_{OUTPP(MAX)} = \frac{V_{PLSET(MAX)} \times C_{PLSET(MAX)} \times I_{OUT(MAX)}}{I_{PLSET(MIN)} \times C_{OUT(MIN)}} + \frac{I_{OUT(MAX)} \times D_{ON(MAX)}}{C_{OUT(MIN)} \times f_{OSC(MIN)}} + I_{L(MAX)} \times R_{ESR(MAX)}$$

$V_{OUTPP(MAX)}$: Maximum value of V_{OUT} ripple voltage	$V_{PLSET(MAX)}$: Maximum value of PLSET threshold voltage
$I_{PLSET(MIN)}$: Minimum value of PLSET charging current	$C_{PLSET(MAX)}$: Maximum value of PLSET pin capacitance
$I_{OUT(MAX)}$: Maximum output current	$D_{ON(MAX)}$: Maximum value of DCDC-Duty
$C_{OUT(MIN)}$: Minimum value of V_{OUT} capacitance	$f_{OSC(MIN)}$: Minimum value of DC/DC oscillator frequency
$I_{L(MAX)}$: Maximum input (inductor) peak current	$R_{ESR(MAX)}$: Maximum value of equivalence serial resistor for output capacitance C_{OUT}

The actual V_{OUT} ripple voltage is affected by board layout and component characteristics. Be sure to check on the actual device and set the capacitance value considering sufficient margin so that it will be within the allowable ripple voltage. The maximum value of C_{OUT} that can be set is 100 μ F.

6 Selecting Input Capacitance

A ceramic capacitor with an input capacitance of 10 μ F or more and a low ESR is recommended. If a capacitor outside this range is selected, an excessive ripple voltage may be superimposed on the input voltage, causing IC malfunction. In addition, the capacitor C_{IN} used for the input is determined by the allowable amount of V_{INPP} which is the ripple voltage of V_{IN} .

7 Setting Overvoltage Protection (OVP)

Overvoltage protection (OVP) is set by an external resistors R_{OVP1} , R_{OVP2} . When the OVP pin becomes 1.21 V or more, it detects overvoltage and stops DC/DC switching. Also, when the OVP pin is 1.21 V or more and the LED1 to LED4 pin voltage is 0.2 V or less, the open state is detected, and the circuit is latched off (Reference [protection function](#)).

To prevent an open false detection, the resistor division voltage of the maximum value of the output voltage must be below the minimum value of open detection voltage.

Set R_{OVP1} , R_{OVP2} so that they satisfy the following formulas.

$$V_{OUT(MAX)} \times \frac{R_{OVP1}}{(R_{OVP1} + R_{OVP2})} < V_{OVPDET(MIN)} \quad (1)$$

e.g.) When using 8 series of LEDs with $R_{ISET} = 15.1$ k Ω and $V_f = 3.2$ V ± 0.2 V.

$$\begin{aligned} V_{OUT(MAX)} &= (3.2 + 0.2) \times 8 + V_{LEDCTL(MAX)} \\ &= 28.06 \text{ [V]} \end{aligned}$$

$$V_{OVPDET(MIN)} = 1.16 \text{ [V]}$$

If $R_{OVP1} = 20$ k Ω , it is necessary to set $R_{OVP2} > 464$ k Ω from equation (1).

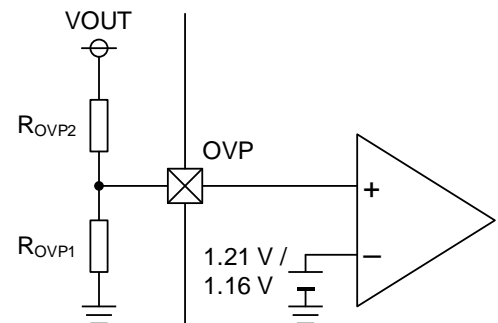


Figure 33. OVP Application Circuit Diagram

$V_{OUT(MAX)}$: Maximum output voltage
R_{OVP1} : Overvoltage protection detect resistor (GND side)
R_{OVP2} : Overvoltage protection detect resistor (VCC side)
$V_{OVPDET(MIN)}$: Minimum value of overvoltage protection detect voltage
R_{ISET} : Resistor for LED current setting
$V_{OUT(MAX)}$: Maximum output voltage
$V_{LEDCTL(MAX)}$: Maximum value of LED control voltage
R_{OVP1} : Overvoltage protection detect resistor (GND side)
R_{OVP2} : Overvoltage protection detect resistor (VCC side)
$V_{OVPDET(MIN)}$: Minimum value of overvoltage protection detect voltage

Application Components Selection Method – continued

8 Checking Rated Voltage/Current of Inductor (L), Diode (D1, D2), MOSFET (M1), Resistor (R_{CSH}), and Capacitance (C_{IN}, C_{OUT})

(Note 1)	Rated Current	Rated Voltage	Power Dissipation
Current Detect Resistor R _{CSH}	-	-	> I _{OCPH(MAX)} ² × R _{CSH(MIN)}
MOSFET M1	> I _{OCPH(MAX)} (Note 2)	> V _{CC(MAX)} (Note 3)	-
Diode D1 (Note 3)	(Note 4)	> V _{CC(MAX)}	-
Input Capacitance C _{IN}	-	> V _{CC(MAX)}	-
Inductor L	> I _{A(MAX)} (Note 5)	-	-
Diode D2	> I _{A(MAX)} (Note 5)	> V _{OUT_OVP(MAX)} (Note 6)	-
Output Capacitance C _{OUT}	-	> V _{OUT_OVP(MAX)}	-

(Note 1) Consider the variation of external components and make setting with sufficient margin.
 (Note 2) $I_{OCPH(MAX)} = V_{OCPH(MAX)} / R_{CSH(MIN)}$
 (Note 3) If diode D1 is not mounted, ringing will occur on the drain side of MOSFET M1 when MOSFET M1 is turned OFF due to input overcurrent protection. Ringing causes the drain side of MOSFET M1 to have a negative potential, which may cause the IC to malfunction. It is recommended to mount the diode D1 when using the input overcurrent protection function.
 (Note 4) Set so that the rated value of the peak forward surge current > D1 generated current when input overcurrent protection is detected. When the input overcurrent protection is detected, check the D1 generated current on the actual device.
 (Note 5) $I_{A(MAX)} = I_{OCPL(MAX)} + \frac{V_{CC(MAX)}}{L_{(MIN)}} \times t_{OCPL}$ t_{OCPL} : OCPL detect delay time (MAX = 150 ns)
 Since the inductor current reaches I_{OCPL} at startup, the recommended setting is Rated Current > I_{A(MAX)}. However, it is possible to set Rated Current > I_{L(MAX)} after confirming that no damage occurs in the actual device.
 (Note 6) DC reverse voltage

9 Setting Phase Compensation Circuit

About application stability conditions

The stability conditions of the LED voltage feedback system are as follows.

- (1) Phase delay when gain is 1 (0 dB) is 150° or less (i.e., phase margin is 30° or more)
- (2) Frequency (unity gain frequency) when gain is 1 (0 dB) is 1/10 or less of switching frequency

By inserting phase lead fz near the unity gain frequency, stability can be ensured by phase compensation. The phase delay fp1 is determined by C_{OUT} and the output impedance R_L. Each is as follows.

Phase lead $fz = 1 / (2\pi \times R_{PC} \times C_{PC})$ [Hz]

Phase delay $fp1 = 1 / (2\pi \times R_L \times C_{OUT})$ [Hz]

* Output impedance calculated by $R_L = V_{OUT} / I_{OUT}$

Good results can be obtained by setting fz from 1 kHz to 10 kHz. Substitute the value at maximum load for R_L.

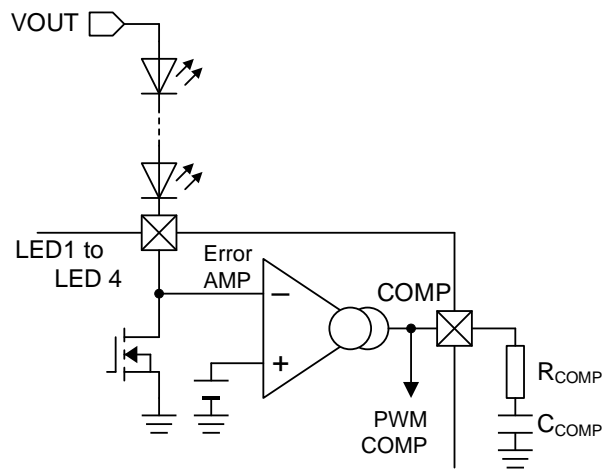


Figure 34. Error AMP Block Application Circuit Diagram

In addition, this setting is a simple calculation and is not calculated exactly, so it may be necessary to make adjustments on the actual device. Also, these characteristics will change depending on the board layout, load conditions, etc., so when designing for mass production, make sure to check the actual device before setting.

Application Components Selection Method – continued

10 Operation Check on Actual Device

Select the constant according to the above procedure and precautions regarding constant setting. In addition, since this selection is calculated by theoretical calculation, it does not include variations in external components or changes in their characteristics and is not guaranteed. The parameters that affect the characteristics of the product will change depending on the actual layout pattern, such as power supply voltage, LED current / number of lamps, inductor, output capacitance, and switching frequency, so be sure to check with the actual device.

Additional Components for EMC Countermeasure

The figure below shows the examples of EMC countermeasure components.

- (1) Capacitor for built-in FET current loop noise reduction
- (2) Capacitor for output current loop noise reduction
- (3) Capacitor for power line high frequency noise reduction
- (4) Low-pass filter for power line noise reduction
- (5) Common mode filter for power line noise reduction
- (6) Snubber circuit for built-in FET high frequency noise reduction
- (7) Snubber circuit for ringing reduction during built-in FET switching

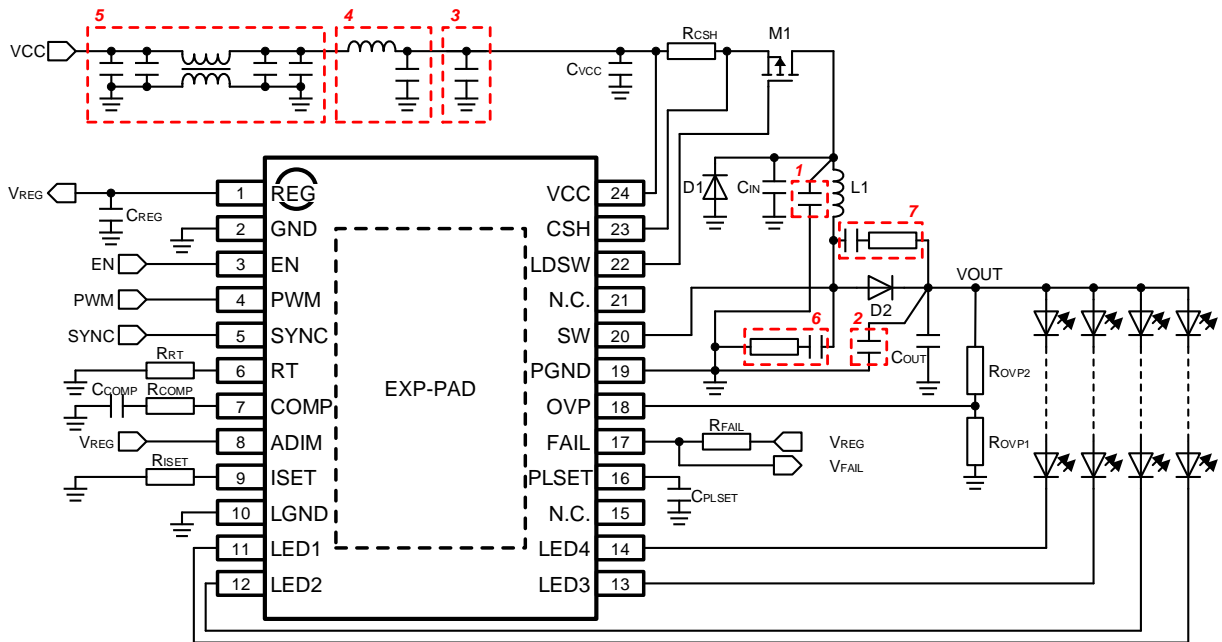


Figure 35. Application Circuit Diagram Reference Example (including EMC countermeasure components)

Precautions for PCB Layout

PCB layout patterns have a significant impact on efficiency and ripple characteristics, so care must be taken when designing. In the boost configuration, there is a "Loop" as shown in the figure on the right. Place the components in the Loop as close as possible (e.g., place GND of C_{OUT} and PGND as close together). Also, make sure that the wiring in each loop is as low impedance as possible. Refer to "[page 28 PCB Application Circuit Diagram](#)" for other detailed precautions regarding PCB layout.

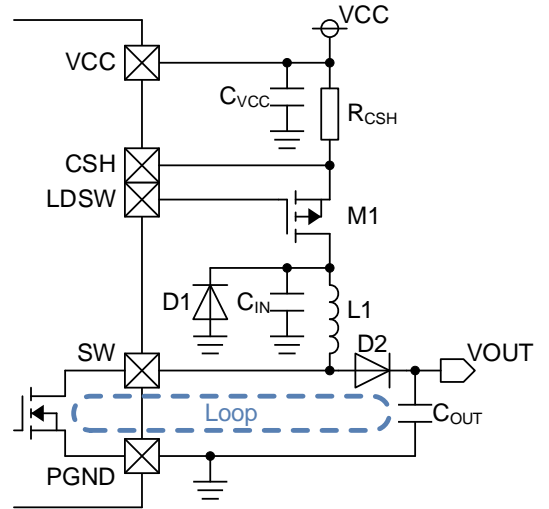


Figure 36. Circuit of DC/DC Block

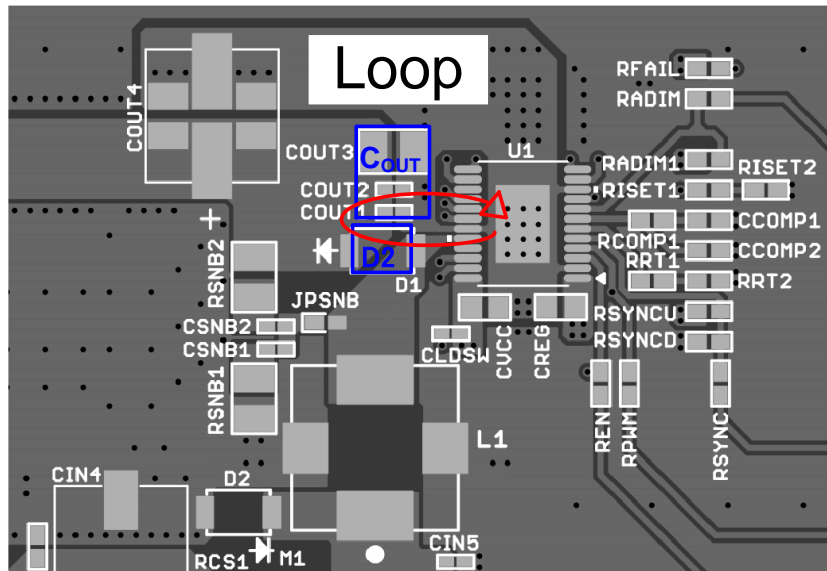


Figure 37. BD83A04EFV-M PCB TOP-layer

Power Consumption Calculation Example

The maximum value of IC power consumption can be easily calculated by the following procedure. Take heat dissipation measures so that the rise in chip temperature due to this power consumption does not exceed T_{jmax} under the environmental conditions (ambient temperature, heat dissipation fins, etc.) used by the customer.

$$P_{C(MAX)} = I_{CC(MAX)} \times V_{CC(MIN)} \quad (1) \text{ Circuit power}$$

$$+ C_{ISS(MAX)} \times V_{REG(MAX)} \times f_{OSC(MAX)} \times V_{REG(MAX)} \quad (2) \text{ SW FET drive stage power}$$

$$+ \{V_{LEDCTL(MAX)} \times M + (V_{f(MAX)} - V_{f(MIN)}) \times N \times (M - 1)\} \times I_{LED(MAX)} \quad (3) \text{ Current driver power}$$

$$+ \frac{(V_{OUT(MAX)} - V_{CC(MIN)})}{V_{OUT(MAX)}} \times R_{ON_SW(MAX)} \times I_{LAVG(MAX)} \times I_{LAVG(MAX)} \quad (4) \text{ Power during SW FET ON}$$

$$+ I_{LAVG(MAX)} \times V_{OUT(MAX)} \times \frac{1}{6} \times (T_{r(MAX)} + T_{f(MAX)}) \times f_{OSC(MAX)} \quad (5) \text{ SW FET switching power}$$

$$\left[\begin{array}{l} V_{OUT(MAX)} = V_{f(MAX)} \times N + V_{LEDCTL(MAX)} \quad (6) \text{ Output voltage} \\ I_{OUT(MAX)} = I_{LED(MAX)} \times M \quad (7) \text{ Output current} \\ I_{LAVG(MAX)} = V_{OUT(MAX)} \times I_{OUT(MAX)} / (\eta \times V_{CC(MIN)}) \quad (8) \text{ Input (inductor) average current} \end{array} \right.$$

$P_{C(MAX)}$: Maximum value of IC power consumption	N	: Number of LED series
$I_{CC(MAX)}$: Maximum value of circuit current	$I_{LED(MAX)}$: Maximum value of LED current per channel
$V_{CC(MIN)}$: Minimum value of power supply voltage	$R_{ON_SW(MAX)}$: Maximum value of SW pin ON resistor
$C_{ISS(MAX)}$: Maximum value of SW FET gating capacitance	$V_{OUT(MAX)}$: Maximum output voltage
$f_{OSC(MAX)}$: Maximum value of oscillation frequency	$T_{r(MAX)}$: Maximum value of SW rise time
$V_{REG(MAX)}$: Maximum value of reference voltage	$T_{f(MAX)}$: Maximum value of SW fall time
$V_{LEDCTL(MAX)}$: Maximum value of LED control voltage	$I_{OUT(MAX)}$: Maximum value of output current
M	: Number of LED parallels	$I_{LAVG(MAX)}$: Maximum value of input (inductor) average current
$V_{f(MAX)}$: Maximum value of LED Vf voltage	η	: Efficiency (about 85 %)
$V_{f(MIN)}$: Minimum value of LED Vf voltage		

Power Consumption Calculation Example – continued

<Calculation Example>

Calculate IC power consumption using the following conditions as an example.

$I_{CC(MAX)}$	Maximum value of circuit current	10 mA	$V_{f(MAX)}$	Maximum value of LED Vf voltage	3.4 V
$V_{CC(MIN)}$	Minimum value of power supply voltage	10.5 V	$V_{f(MIN)}$	Minimum value of LED Vf voltage	3.0 V
$C_{ISS(MAX)}$	Maximum value of SW FET gating capacitance	100 pF	N	Number of LED series	8 stages
$f_{OSC(MAX)}$	Maximum value of oscillation frequency	374 kHz	$I_{LED(MAX)}$	Maximum value of LED current per channel	65 mA
$V_{REG(MAX)}$	Maximum value of reference voltage	5.3 V	$R_{ON_SW(MAX)}$	Maximum value of SW pin ON resistor	0.4 Ω
$V_{LEDCTL(MAX)}$	Maximum value of LED control voltage	0.74 V	$T_r(MAX)$	SW rise time	20 ns
M	Number of LED parallels	4 rows	$T_f(MAX)$	SW fall time	20 ns
			η	Efficiency (about 90 %)	0.9

From equation (6),

$$\begin{aligned} V_{OUT(MAX)} &= V_{f(MAX)} \times N + V_{LEDCTL(MAX)} \\ &= 3.4 \text{ V} \times 8 + 0.74 \text{ V} \\ &= 27.94 \text{ [V]} \end{aligned}$$

From equation (7),

$$\begin{aligned} I_{OUT(MAX)} &= I_{LED(MAX)} \times M \\ &= 65 \text{ mA} \times 4 \\ &= 260 \text{ [mA]} \end{aligned}$$

Substituting the values obtained in equations (6) and (7) into equation (8),

$$\begin{aligned} I_{LAVG(MAX)} &= V_{OUT(MAX)} \times I_{OUT(MAX)} / (\eta \times V_{CC(MIN)}) \\ &= 27.94 \text{ V} \times 260 \text{ mA} / (0.9 \times 10.5 \text{ V}) \\ &= 0.77 \text{ [A]} \end{aligned}$$

Therefore, the maximum value of IC power consumption $P_{C(MAX)}$ is calculated as follows:

$$\begin{aligned} P_{C(MAX)} &= 10 \text{ mA} \times 10.5 \text{ V} \\ &\quad + 100 \text{ pF} \times 5.3 \text{ V} \times 374 \text{ kHz} \times 5.3 \text{ V} \\ &\quad + \{0.74 \text{ V} \times 4 + (3.4 \text{ V} - 3.0 \text{ V}) \times 8 \times (4 - 1)\} \times 65 \text{ mA} \\ &\quad + \{(27.9 \text{ V} - 10.5 \text{ V}) / 27.9 \text{ V}\} \times 0.4 \text{ } \Omega \times 0.77 \text{ A} \times 0.77 \text{ A} \\ &\quad + 0.77 \text{ A} \times 27.9 \text{ V} / 6 \times (20 \text{ ns} + 20 \text{ ns}) \times 374 \text{ kHz} \\ &= 1.12 \text{ [W]} \end{aligned}$$

From thermal resistance $\theta_{ja} = 30.1 \text{ }^\circ\text{C/W}$, the maximum calorific value $\Delta t_{(MAX)}$ can be estimated by the following equation.

$$\Delta t_{(MAX)} = P_{C(MAX)} \times \theta_{ja} = 1.12 \text{ W} \times 30.1 \text{ }^\circ\text{C/W} = 33.7 \text{ [}^\circ\text{C]}$$

When the ambient temperature is $85 \text{ }^\circ\text{C}$, the maximum chip temperature $t_{C(MAX)}$ is following.

$$t_{C(MAX)} = 85 \text{ }^\circ\text{C} + 33.7 \text{ }^\circ\text{C} = 118.7 \text{ [}^\circ\text{C]}$$

Make sure that $t_{C(MAX)}$ calculated here is less than $T_{jmax} = 150 \text{ }^\circ\text{C}$.

The above is a simple calculation example only. The value of thermal resistance varies depending on the actual board conditions and layout. Confirm the calculation here as a guide for thermal design.

Application Circuit Example

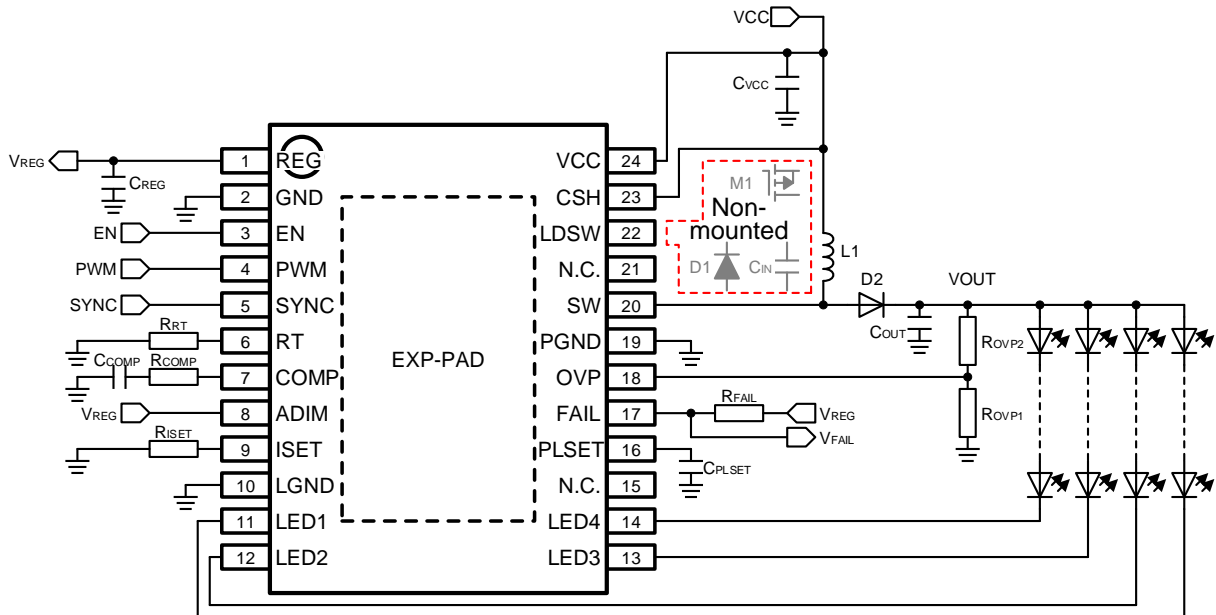
1 Peripheral Circuit When PMOS Is Not Used

When the load switch M1 is not required, such as when using FUSE on the input side, connect the CSH pin and inductor L1 and open the LDSW pin.

Also, set FUSE rating to I_{FUSE} or more.

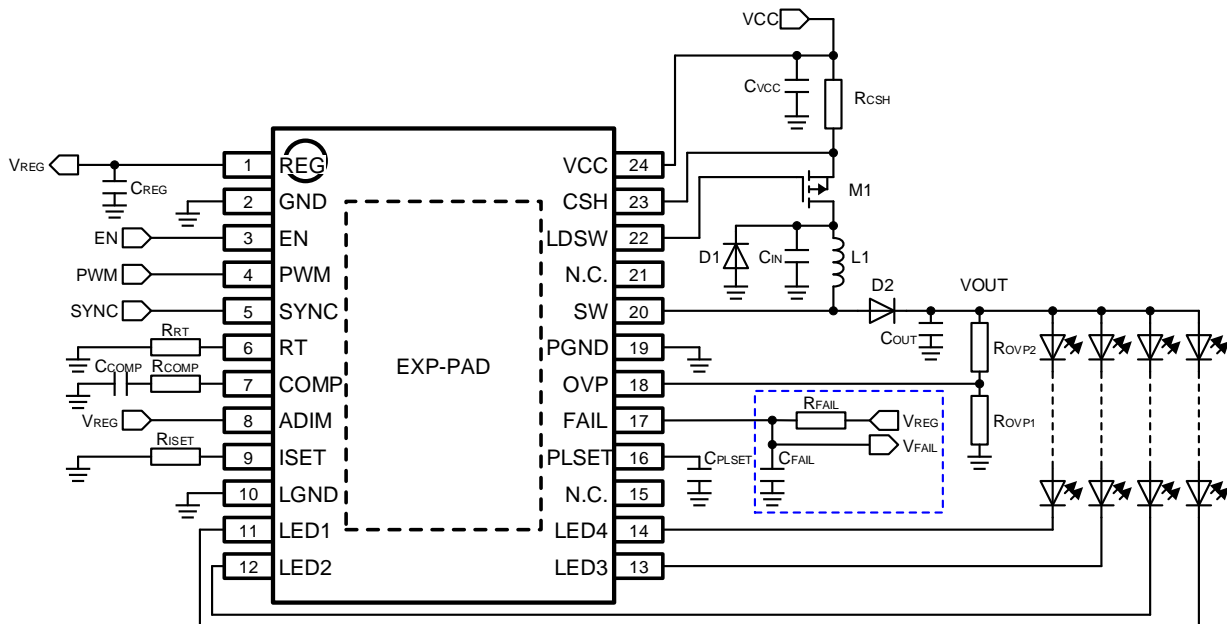
$$I_{FUSE} > 4.06 A + \frac{V_{CC(MAX)}}{L_{(MIN)}} \times t_{OCPL}$$

I_{FUSE} : FUSE rated current
 V_{CC(MAX)} : Maximum value of power supply voltage
 L_(MIN) : Minimum value of inductance
 t_{OCPL} : OCPL detect delay time (MAX = 150 ns)



2 Monitoring the Status of the FAIL Pin with Microcontroller

OCPL function starts operation again after stopping operation for the specified timer time. Therefore, the FAIL pin periodically outputs the detect/release flag until the error is cleared. In the case of a system configuration that monitors the FAIL pin with a microcontroller, there is a possibility that it will be erroneously determined as a normal state even though it is in an abnormal state. By adding C_{FAIL} as shown below, it is possible to fix the FAIL output to Low in an abnormal state.



I/O Equivalence Circuit

<p>1.REG, 24.VCC</p>	<p>2.GND, 10.LGND, 19.PGND</p>	<p>3.EN</p>
<p>4.PWM, 5.SYNC</p>	<p>6.RT</p>	<p>7.COMP</p>
<p>8.ADIM</p>	<p>9.ISET</p>	<p>11 - 14.LED1 - LED4</p>
<p>16.PLSET</p>	<p>17.FAIL</p>	<p>18.OVP</p>
<p>20.SW</p>	<p>22.LDSW</p>	<p>23.CSH</p>

All values are Typ values.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

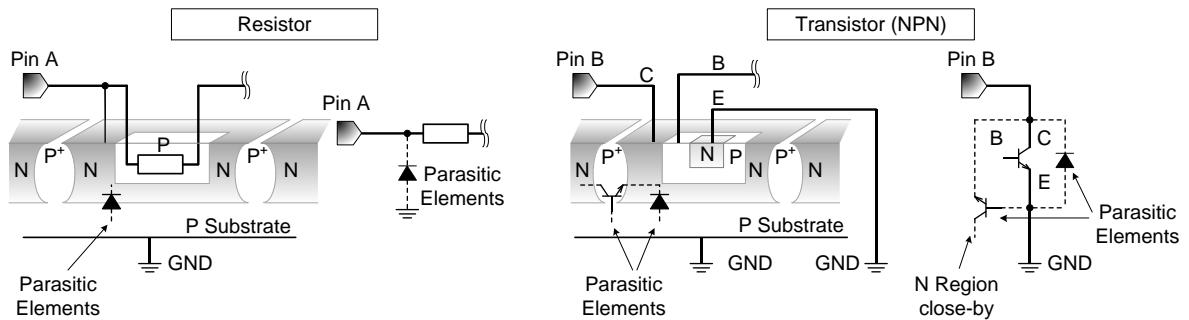


Figure 38. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"

A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"

A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"

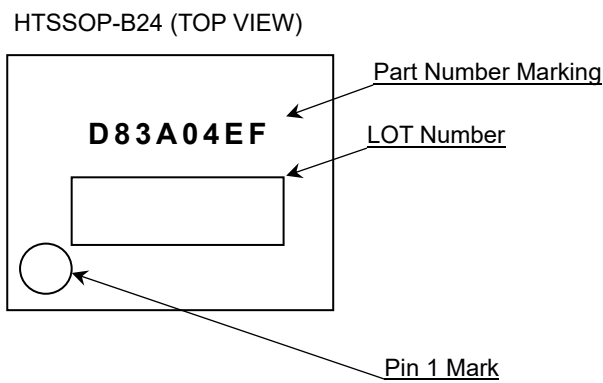
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

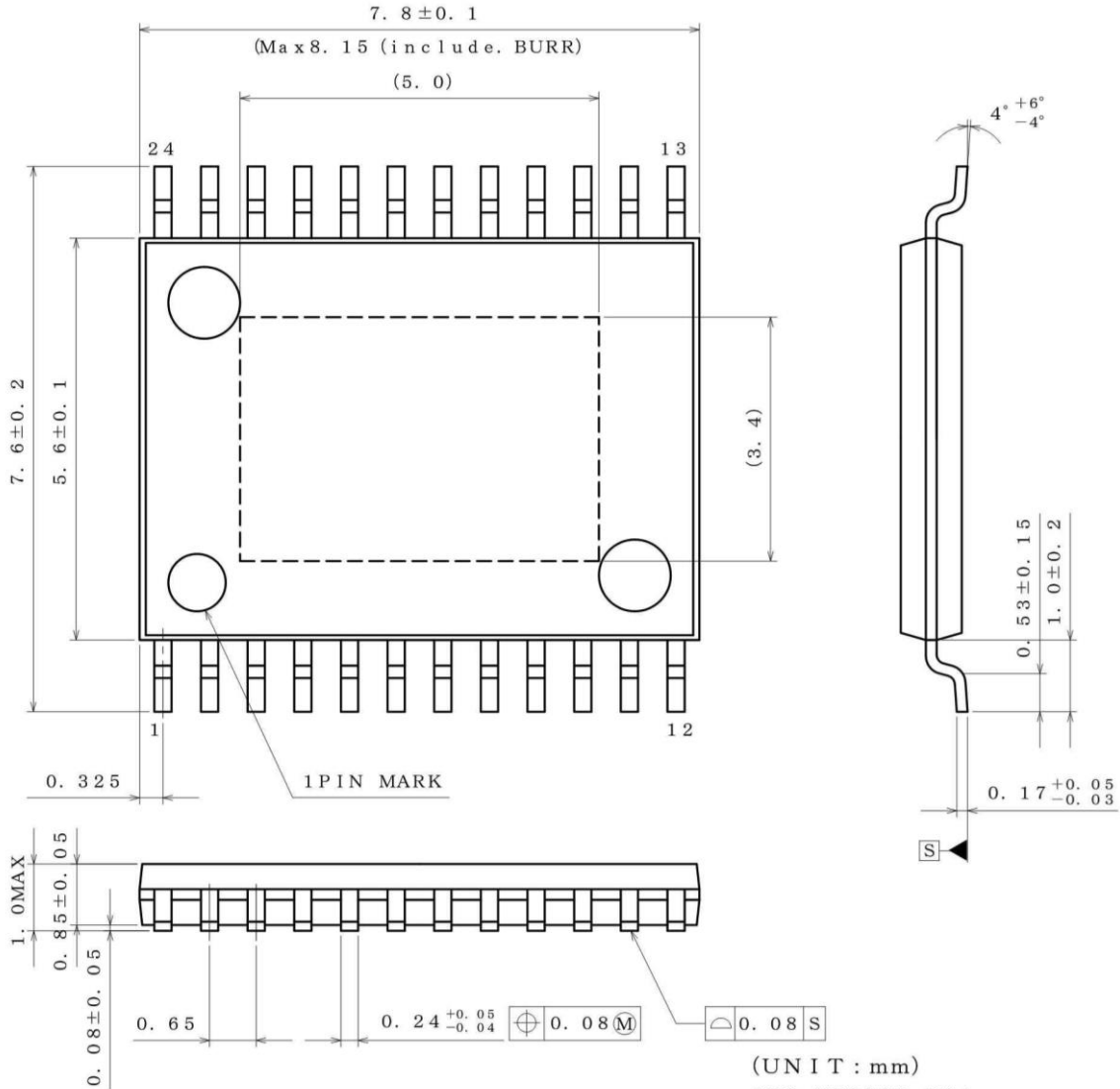


Marking Diagram



Physical Dimension and Packing Information

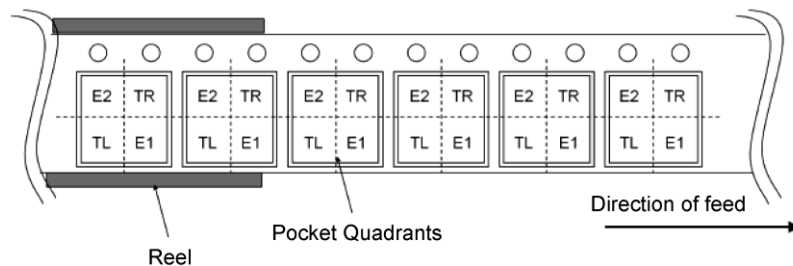
Package Name	HTSSOP-B24
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(UNIT : mm)
 PKG : HTSSOP-B24
 Drawing No. EX191-5002-1

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
17.Feb.2022	005	New Release
18.Aug.2022	006	P.6, 28 Added a note about the possibility of inrush current flowing when VCC is turned on with EN=L. P.24, 28 Changed description about RC filter for external synchronization and corrected typos.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
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5. Please verify and confirm characteristics of the final or mounted products in using the Products.
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7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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