Click here for production status of specific part numbers.

MAX17686

4.5V to 60V Input, High-Efficiency, Iso-Buck DC-DC Converter

General Description

The Rainier series of isolated DC-DC products enable small, efficient solutions with a lower BOM cost. The MAX17686 is a high-voltage, high-efficiency, iso-buck DC-DC converter designed to provide isolated power up to 5W. The device operates over a wide 4.5V to 60V input and uses primary-side feedback to regulate the output voltage.

The MAX17686 uses peak-current-mode control. The low-resistance, on-chip MOSFETs ensure high efficiency at full load while simplifying the PCB layout.

The device generates a well regulated primary side voltage which is then scaled by a suitable transformer turns ratio to derive isolated secondary output rails. The MAX17686 features robust overcurrent protection on both the primary and secondary side.

The MAX17686 is available in a compact 10-pin (3mm x 2mm) TDFN package. Simulation model and design automation are available in EE-Sim

Applications

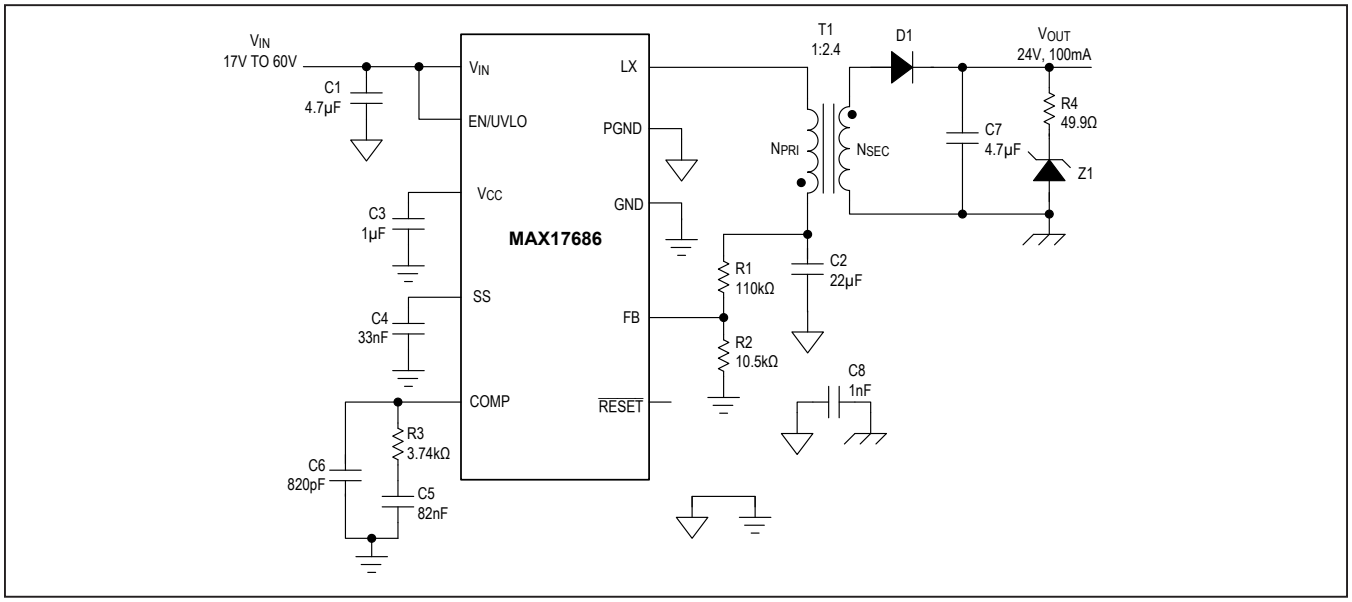
- Isolated Fieldbus Interfaces
- PLC I/O Modules
- Smart Meters
- Isolated Power Supplies in Medical Equipment
- Floating Power Supply Generation

Benefits and Features

- Reduces External Components and Total Cost
  - No Optocoupler
  - Synchronous Primary Operation
  - All-Ceramic Capacitors, Compact Layout
- Supports Numerous Isolated DC-DC Applications
  - Wide 4.5V to 60V Input
  - Delivers Up to 5W Output Power
- Reduces Power Dissipation
  - Peak Efficiency > 90%
  - 0.9µA (typ) Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Peak and Sink Current-Limit Protection
  - Robust Secondary-Side Output Overcurrent Protection
  - ±1.7% Feedback Accuracy
  - Programmable EN/UVLO Threshold
  - Adjustable Soft-Start
  - Overtemperature Protection
  - -40°C to +125°C Operation

***Ordering Information* appears at end of data sheet.**

Application Circuit



maxim integrated™

Absolute Maximum Ratings

V_{IN} to GND .....-0.3V to +65V
EN/UVLO to GND..... -0.3V to (V_{IN} + 0.3V)
LX to PGND..... -0.3V to (V_{IN} + 0.3V)
V_{CC}, FB, $\overline{RESET}$, COMP, SS to GND .....-0.3V to +6V
PGND to GND.....-0.3V to +0.3V
LX Total RMS Current .....±1.6A

Output Short-Circuit Duration.....Continuous
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 10 TDFN	
Package Code	T1032N+1
Outline Number	**21-0429**
Land Pattern Number	**90-0082**
THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 1)	
Junction to Ambient (θ_{JA})	67.3°C/W
Junction to Case (θ_{JC})	18.2°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Note 1: Continuous Power Dissipation (T_A = +70°C) (derate 14.9mW/°C above +70°C) (multilayer board) 1188.7mW

Electrical Characteristics

(V_{IN} = 24V, V_{GND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 1µF, V_{EN} = 1.5V, C_{SS} = 3300pF, V_{FB} = 0.98 x V_{OUT}, COMP = unconnected, LX = unconnected, $\overline{RESET}$ = unconnected. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})							
Input Voltage Range	V_{IN}			4.5		60	V
Input Supply Current	I_{IN-SH}	V_{EN} = 0V, shutdown mode			0.9	3.5	µA
	I_{IN-SW}	Normal switching mode, no load			1.95	2.8	mA
ENABLE/UVLO (EN/UVLO)							
EN Threshold	V_{ENR}	V_{EN} rising		1.183	1.218	1.253	V
	V_{ENF}	V_{EN} falling		1.1	1.135	1.17	
	$V_{EN-TRUESD}$	V_{EN} falling, true shutdown			0.7		
EN Input Leakage Current	I_{EN}	V_{EN} = V_{IN} = 60V, T_A = +25°C			8	200	nA
LDO							
V_{CC} Output Voltage Range	V_{CC}	6V < V_{IN} < 12V, 0mA < I_{VCC} < 10mA, 12V < V_{IN} < 60V, 0mA < I_{VCC} < 2mA		4.65	5	5.35	V
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 12V		15	40	80	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 5mA		4.1			V
V_{CC} UVLO	V_{CC-UVR}	V_{CC} rising		3.85	4	4.15	V
	V_{CC-UVF}	V_{CC} falling		3.55	3.7	3.85	
POWER MOSFETs							
High-Side pMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.5A (sourcing)	T_A = +25°C		0.55	0.85	Ω
			T_A = T_J = +125°C (Note 3)			1.2	
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.5A (sinking)	T_A = +25°C		0.2	0.35	Ω
			T_A = T_J = +125°C (Note 3)			0.47	
LX Leakage Current	I_{LX_LKG}	V_{EN} = 0V, T_A = +25°C, V_{LX} = (V_{PGND} + 1V) to (V_{IN} – 1V)				1	µA
SOFT-START (SS)							
Charging Current	I_{SS}	V_{SS} = 0.5V		4.7	5	5.3	µA
FEEDBACK (FB)							
FB Regulation Voltage	V_{FB_REG}			0.884	0.9	0.916	V
FB Input Bias Current	I_{FB}	T_A = +25°C				100	nA
TRANSCONDUCTANCE AMPLIFIER (COMP)							
Transconductance	GM	I_{COMP} = ±2.5µA		510	590	650	µS
COMP Source Current	I_{COMP_SRC}			19	32	55	µA
COMP Sink Current	I_{COMP_SINK}			19	32	55	µA
Current Sense Transresistance	R_{CS}			0.45	0.5	0.55	V/A

Electrical Characteristics (continued)

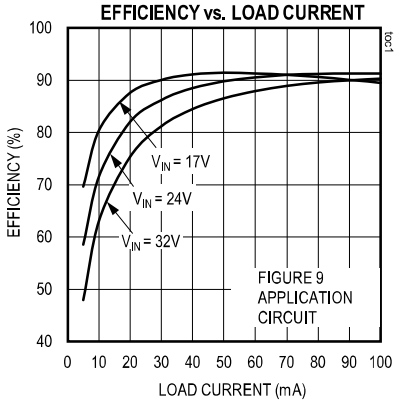
(V_{IN} = 24V, V_{GND} = V_{PGND} = 0V, C_{VIN} = 2.2µF, C_{VCC} = 1µF, V_{EN} = 1.5V, C_{SS} = 3300pF, V_{FB} = 0.98 x V_{OUT}, COMP = unconnected, LX = unconnected, $\overline{RESET}$ = unconnected. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

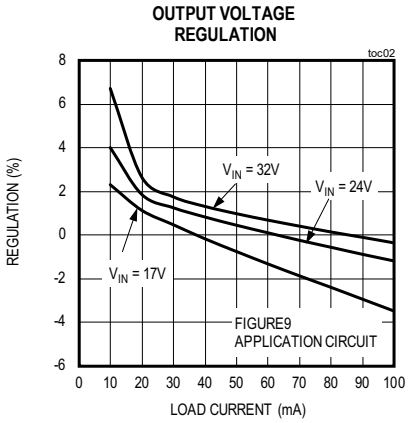
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		1.4	1.65	1.9	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$		1.45	1.7	2	A
Sink Current-Limit Threshold	$I_{SINK-LIMIT}$		1.05	1.25	1.45	A
TIMINGS						
Switching Frequency	f_{SW}		186	200	213	kHz
Events to Hiccup After Crossing Runaway Current Limit				1		
V_{OUT} Undervoltage Trip Level to Cause Hiccup	$V_{OUT-HICF}$	V_{SS} > 0.95V (soft-start is done)	67.86	70.5	73.14	%
Hiccup Timeout				32768		Cycles
Minimum On-Time	t_{ON_MIN}		200	300	415	ns
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.98 x V_{FB-REG}	96.5	97.5	98.5	%
LX Dead Time				12		ns
$\overline{RESET}$						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 1mA			0.02	V
$\overline{RESET}$ Output Leakage Current High		V_{FB} = 1.01 x V_{FB-REG}, T_A= 25°C			0.45	µA
FB Threshold for $\overline{RESET}$ Falling	V_{FB-OKF}	V_{FB} falling	90.5	92.5	94.5	%
FB Threshold for $\overline{RESET}$ Rising	V_{FB-OKR}	V_{FB} rising	93.5	95.5	97.5	%
$\overline{RESET}$ Delay After FB Reaches 95% Regulation		V_{FB} rising		1024		Cycles
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising		165		°C
Thermal Shutdown Hysteresis				10		°C

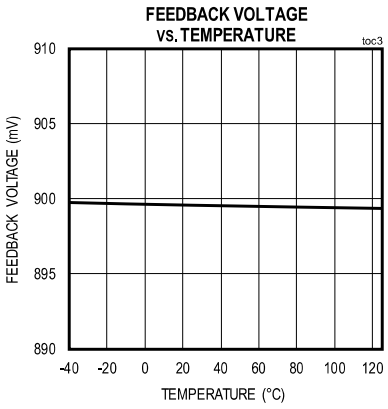
Note 2: All limits are 100% tested at +25°C. Limits over temperature are guaranteed by design.
Note 3: Guaranteed by design, not production tested.

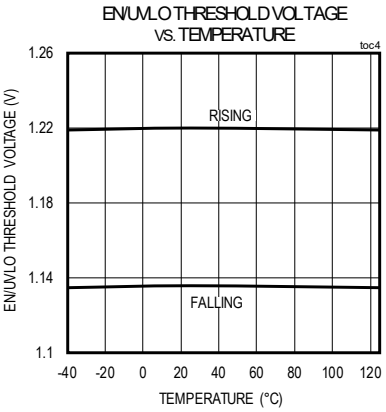
Typical Operating Characteristics

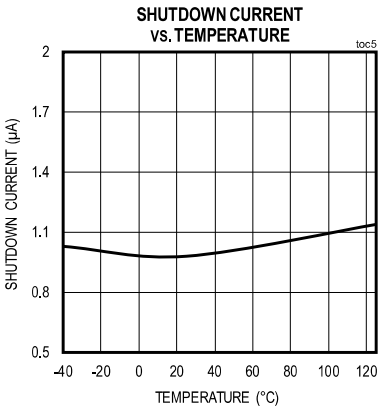
(V_{IN} = 24V, V_{GND} = V_{PGND} = 0V, C_{VIN} = 1µF, C_{VCC} = 1µF, V_{EN} = 1.5V, C_{SS} = 33nF, T_A = +25°C, unless otherwise noted.)

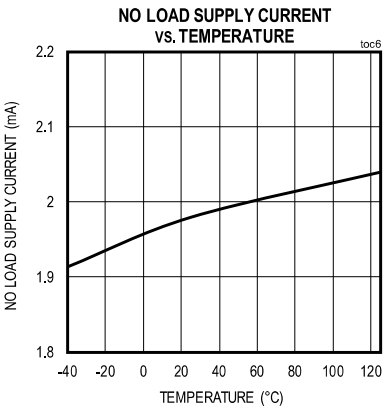


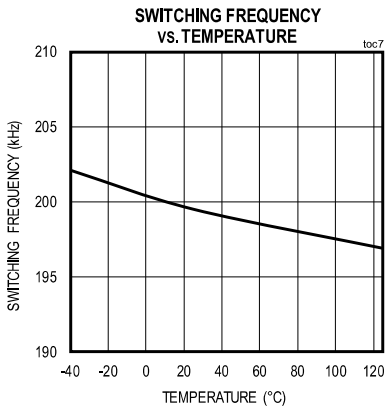


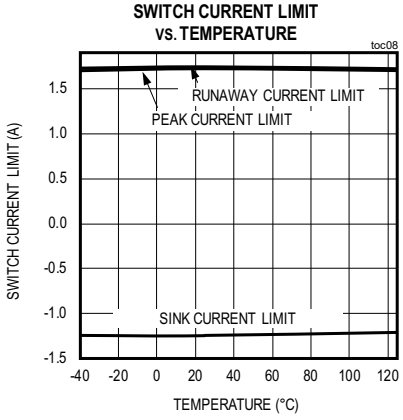








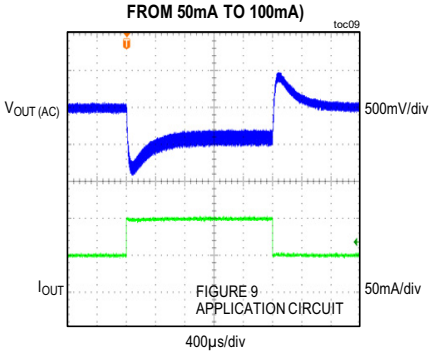




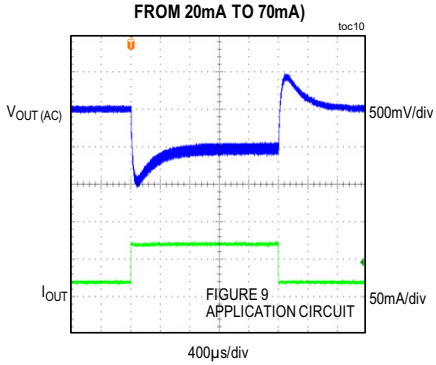
Typical Operating Characteristics (continued)

(V_{IN} = 24V, V_{GND} = V_{PGND} = 0V, C_{VIN} = 1µF, C_{VCC} = 1µF, V_{EN} = 1.5V, C_{SS} = 33nF, T_A = +25°C, unless otherwise noted.)

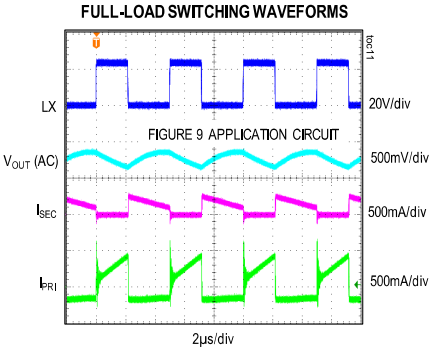
LOAD TRANSIENT RESPONSE
(LOAD CURRENT STEPPED
FROM 50mA TO 100mA)



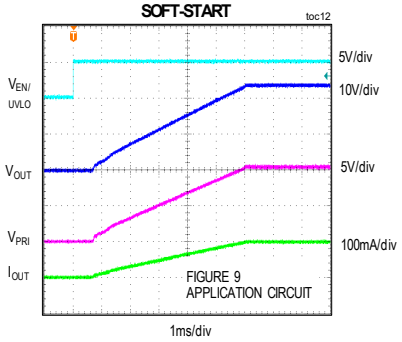
LOAD TRANSIENT RESPONSE
(LOAD CURRENT STEPPED
FROM 20mA TO 70mA)



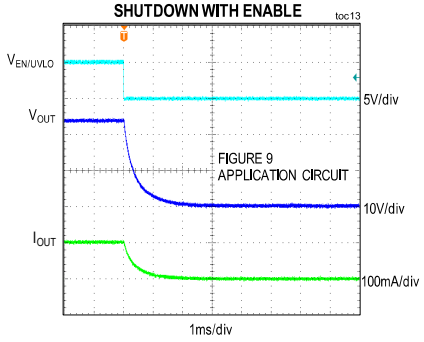
FULL-LOAD SWITCHING WAVEFORMS



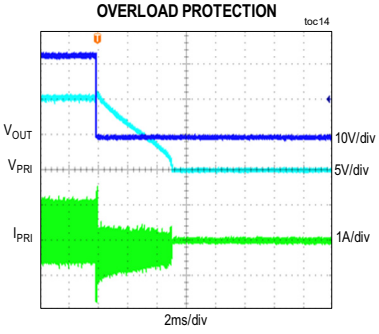
SOFT-START



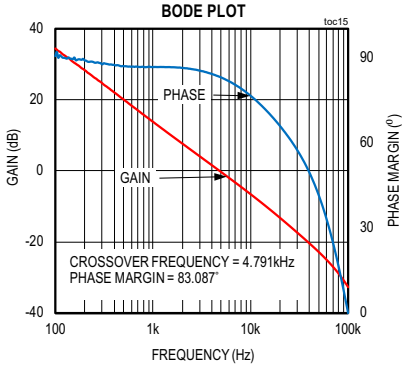
SHUTDOWN WITH ENABLE



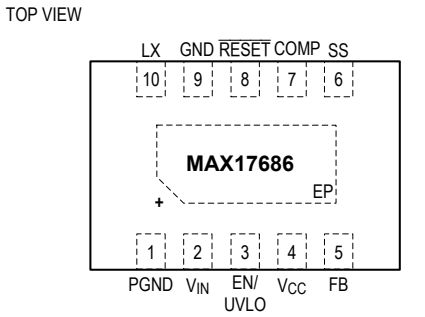
OVERLOAD PROTECTION



BODE PLOT



Pin Configuration



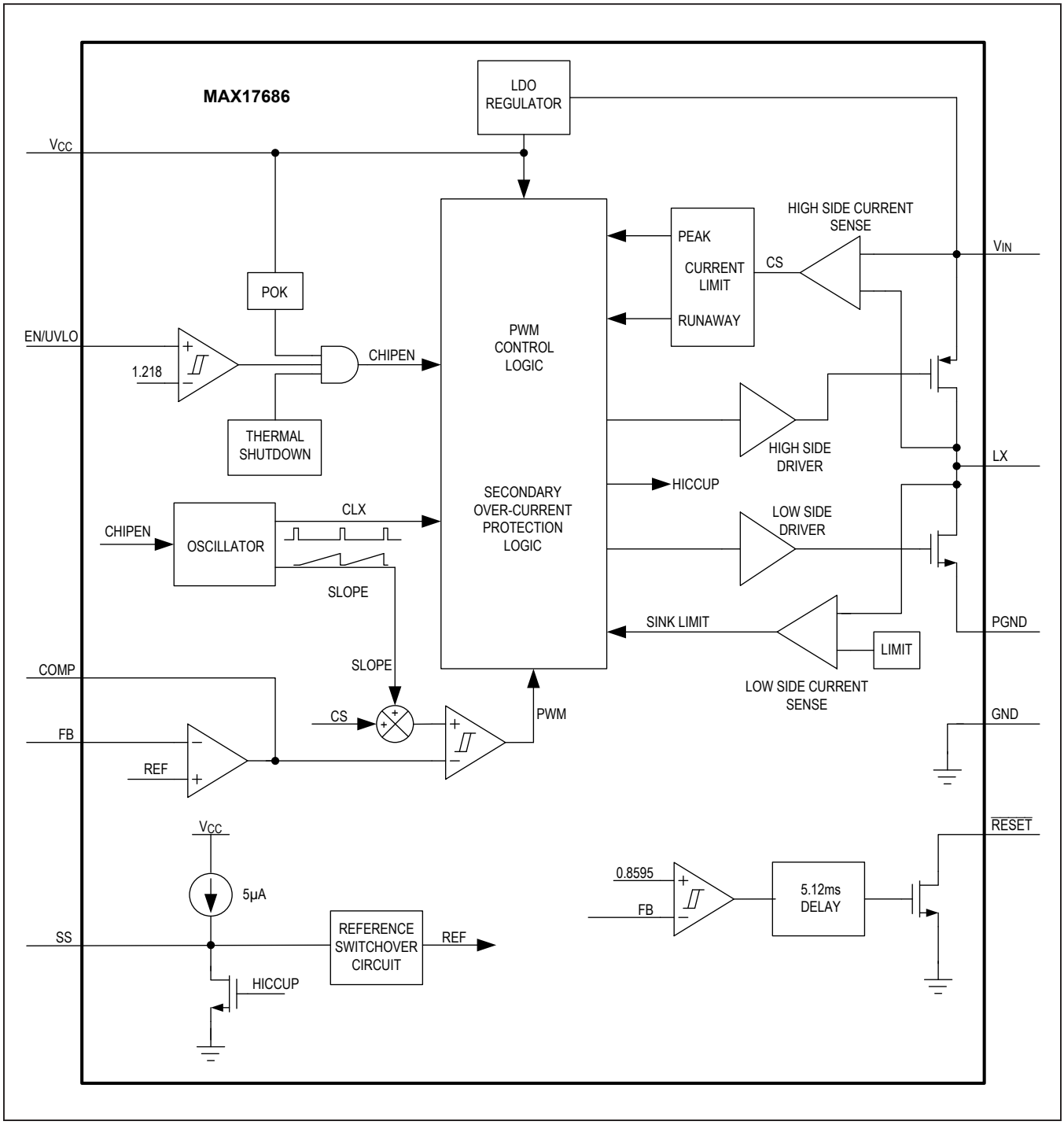
TDFN
3mm x 2mm

*EP = EXPOSED PAD, CONNECTED TO GND

Pin Description

PIN	NAME	FUNCTION
1	PGND	Power Ground. Connect PGND externally to the power ground plane. Connect GND and PGND pins together at the ground return path of the V_{CC} bypass capacitor.
2	V_{IN}	Switching Regulator Input. Connect a X7R ceramic capacitor from V_{IN} to PGND for bypassing.
3	EN/UVLO	Active-High, Enable/Undervoltage-Detection Input. Pull EN/UVLO to GND to disable the regulator output. Connect EN/UVLO to V_{IN} for always-on operation. Connect a resistor-divider between V_{IN}, EN/UVLO, and GND to program the input voltage at which the device is enabled and turns on.
4	V_{CC}	Internal LDO Output. Bypass V_{CC} to GND with a minimum 1µF capacitor.
5	FB	Output Feedback Connection. Connect FB to a resistor-divider between V_{PRI} and GND to set the output voltage. See the *Adjusting the Primary Output Voltage* section for details.
6	SS	Soft-Start Input. Connect a ceramic capacitor from SS to GND to set the soft-start time.
7	COMP	Compensation Input. Connect an RC network from COMP to GND. See the *External Loop Compensation* section.
8	$\overline{RESET}$	Open-Drain Reset Output. Pull up $\overline{RESET}$ to an external power supply with an external resistor. $\overline{RESET}$ pulls low if FB voltage drops below 92.5% of its set value. $\overline{RESET}$ goes high impedance 1024 clock cycles after FB voltage rises above 95.5% of its set value.
9	GND	Signal Ground.
10	LX	Switching Node. Connect LX to the switching side of the transformer. LX is high impedance when the device is in shutdown mode.
—	EP	Exposed Pad. Connect to the GND pin of the IC. Connect to a large copper plane below the IC to improve heat dissipation capability.

Block Diagram



Detailed Description

The MAX17686 is a high-voltage, high-efficiency, iso-buck DC-DC converter designed to provide isolated power up to 5W. The device operates over a wide 4.5V to 60V input and uses primary side feedback to regulate the output voltage.

The MAX17686 uses peak-current-mode control. The low-resistance, on-chip MOSFETs ensure high efficiency at full load while simplifying the PCB layout.

The programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input-voltage level. An open-drain $\overline{RESET}$ pin provides a delayed power-good signal to the system upon achieving successful regulation of the primary output voltage.

The device operates over the -40°C to +125°C industrial temperature range and is available in a compact 10-pin (3mm x 2mm) TDFN package.

Linear Regulator (V_{CC})

An internal linear regulator (V_{CC}) provides a 5V nominal supply to power the internal blocks and the low-side MOSFET driver. The output of the V_{CC} linear regulator should be bypassed with a 1µF ceramic capacitor to GND. The device employs an undervoltage-lockout circuit that disables the internal linear regulator when V_{CC} falls below 3.7V (typ). The internal V_{CC} linear regulator can source up to 40mA (typ) to supply the device and to power the low-side gate driver.

Enable Input (EN/UVLO) and Soft-Start (SS)

When the EN/UVLO voltage increases above 1.218V (typ), the device initiates a soft-start sequence with the duration of the soft-start being dependent on the value of the capacitor connected from SS to GND. A 5µA current source charges the capacitor and ramps up the SS pin voltage. The SS pin voltage is used as reference for the internal error amplifier. The reference ramp-up allows the output voltage to increase monotonically from zero to the target value.

The EN/UVLO can be used as an input-voltage UVLO-adjustment input. An external voltage-divider between V_{IN} and EN/UVLO to GND adjusts the input voltage at which the device turns on or turns off. See the *Setting the Input Undervoltage Lockout Level* section for details. If input UVLO programming is not desired, connect the EN/UVLO to V_{IN} (see the *Electrical Characteristics* table for the EN/UVLO rising and falling-threshold voltages). Driving the EN/UVLO low disables both power MOSFETs as well as other internal circuitry and reduces V_{IN} quiescent current to 0.9µA (typ). The SS capacitor is discharged with an internal pulldown resistor when the EN/UVLO is low. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the signal source output and the EN/UVLO pin to reduce voltage ringing on the line.

Overcurrent Protection/HICCUP Mode

The MAX17686 are provided with an overcurrent-protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the switch current exceeds the internal limit of 1.65A (typ). Additionally, the sink current limit turns off the low-side switch when the low side MOSFET negative current exceeds 1.25A (typ). A runaway current limit on the high-side MOSFET current at 1.7A (typ) protects the devices under high input voltage, short-circuit conditions.

The MAX17686 provides the robust secondary overcurrent protection, and smooth output voltage recovery after removal of overcurrent, by entering into hiccup mode after detecting 16 consecutive negative current limit events. This is supported by implementing a scheme where the primary capacitor voltage is actively discharged during the hiccup timeout period, and soft-starting both primary and secondary-side outputs.

The MAX17686 enters hiccup mode, either on one occurrence of the runaway current limit, when the primary output voltage drops to 71.14% (typ) of its nominal value after the soft-start is completed, or when 16 consecutive negative current limit events occur. When hiccup is triggered, the converter enters a hiccup timeout period of 32,768 clock cycles. During this period, the high side switch is kept off and the low side switch is turned on each cycle until the low side MOSFET negative current reaches 0.6A limit. This mode of operation effectively produces a negative current in the primary capacitor and discharges it towards zero. Once the hiccup timeout period expires, the MAX17686 smoothly soft starts both primary and secondary output voltages.

If the output capacitance is such that it is discharged to zero within one hiccup timeout period, the MAX17686 executes a normal soft-start operation upon exit from the hiccup timeout period. For cases, where the capacitor is sized such that it does not discharge to zero in one hiccup timeout period, during the next soft-start attempt the converter may re-enter the hiccup time period due to one of the event which triggers hiccup mode. Eventually the primary capacitor is completely discharged and the smooth output voltage recovery is ensured.

In summary the MAX17686 provides both primary and secondary side overcurrent protection.

$\overline{\text{RESET}}$ Output

The device includes a $\overline{\text{RESET}}$ comparator to monitor the primary output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ can sink 2mA of current while low. $\overline{\text{RESET}}$ goes high (high-impedance) 1024 switching cycles after the primary output increases above 95.5% of the nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the primary output voltage drops to below 92.5% of the nominal regulated voltage. In MAX17686, when the secondary output is shorted, the primary output voltage is discharged as well during the hiccup period. So, in this case, even for a fault on the isolated output, the $\overline{\text{RESET}}$ can be used as an indicator. $\overline{\text{RESET}}$ also goes low during thermal shutdown. $\overline{\text{RESET}}$ is valid when the device is enabled and V_{IN} is above 4.5V.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal-overload protection in normal operation.

Applications Information

Operation of the Iso-Buck Converter

The iso-buck is a synchronous-buck-converter-based topology, useful for generating isolated outputs at low power level without using an optocoupler. Figure 1 shows the basic circuit of an iso-buck converter, consists of a half-bridge transformer driver and secondary side filter.

Figure 2 shows the equivalent circuit when the high-side switch (QHS) is ON. During this time, the primary current ramps up and stores energy in the transformer magnetizing inductance L_{PRI} and the primary capacitor C_{PRI}. The secondary side diode is reverse-biased and the load current is supplied by the secondary-side filter capacitor C_{OUT}.

Figure 3 shows the equivalent circuit when the low-side switch (QLS) is on. During this time, the secondary diode gets forward-biased. The primary current ramps down and releases stored energy in the transformer magnetizing inductance and the primary capacitor to the load. Operating waveforms of the converter are shown in Figure 4. Neglecting diode drop V_D, transformer resistances, and leakage inductance, the output voltage V_{OUT} is proportional to the primary output voltage V_{PRI} and is regulated by the MAX17686 control loop.

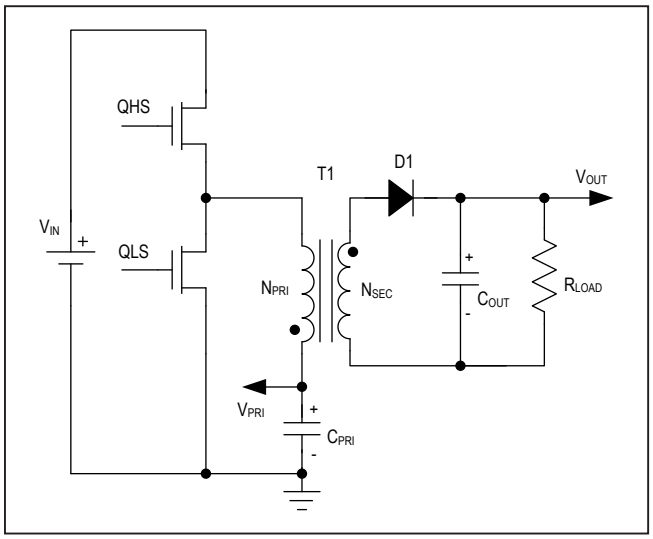


Figure 1. Iso-Buck Topology

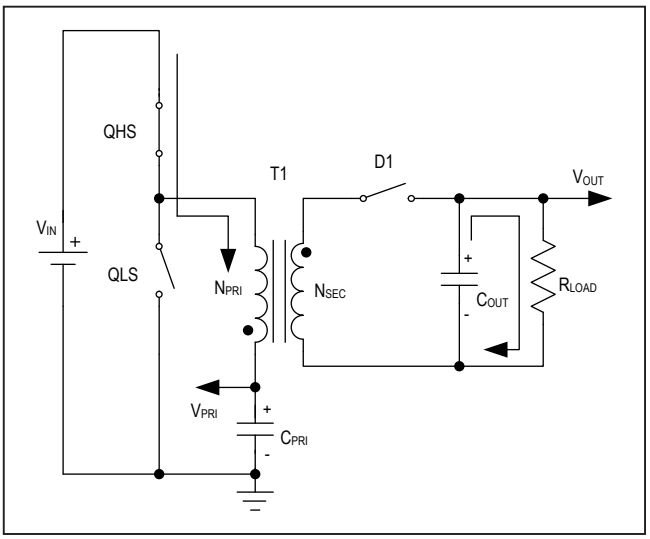


Figure 2. On-Period Equivalent Circuit

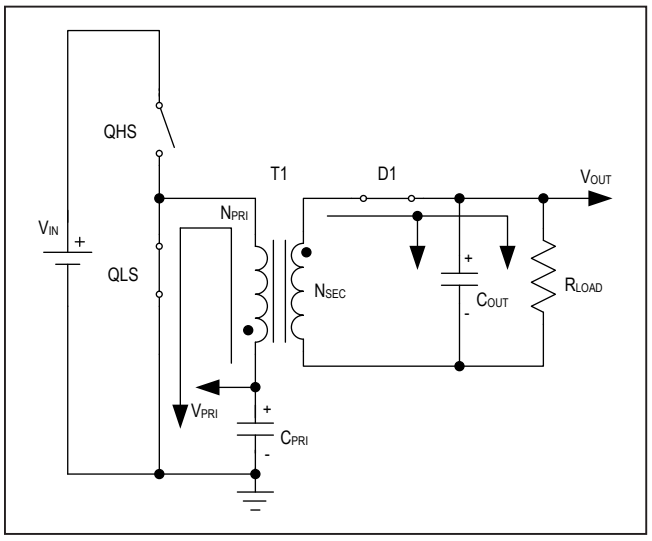


Figure 3. Off-Period Equivalent Circuit

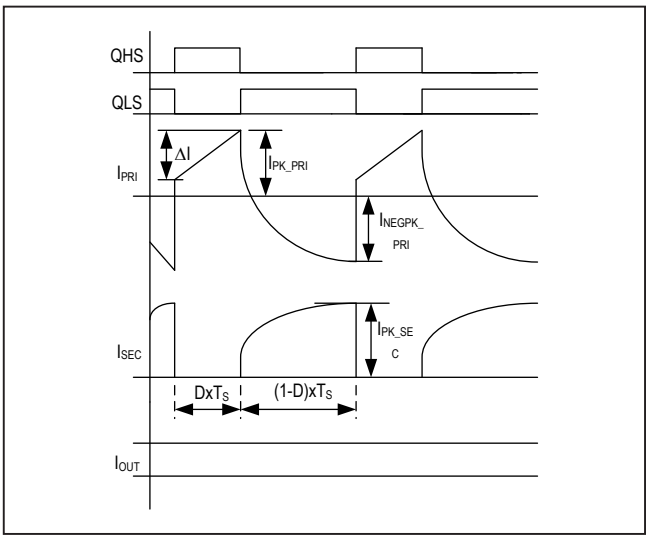


Figure 4. Iso-Buck Operating Waveforms

Primary Output Voltage Selection

Primary output voltage is regulated by the MAX17686 control loop. The primary output voltage can be calculated by using the equation:

$$V_{PRI} = D_{MAX} \times V_{IN\_MIN}$$

where D_{MAX} is the maximum duty cycle of the converter and V_{IN_MIN} is the minimum input voltage. Maximum duty cycle should be in the range of 0.4 to 0.6 for ideal iso-buck operation.

Adjusting the Primary Output Voltage

The primary output voltage is set with a resistor-divider from primary output to FB to GND (see Figure 5). Choose R2 in the range of 10k to 49.9k and calculate R1 using the equation:

$$R1 = R2 \times \left(\frac{V_{PRI}}{0.9} - 1 \right)$$

Turns Ratio Selection

Neglecting parasitic resistances, and leakage inductance, the iso-buck output voltage V_{OUT} is proportional to the primary output voltage V_{PRI}. The turns ratio (K) is given by the equation:

$$\frac{N_{SEC}}{N_{PRI}} = \frac{V_{OUT} + V_D}{V_{PRI}}$$

$$K = \frac{N_{SEC}}{N_{PRI}}$$

Turns ratio can be adjusted to match with the readily available off-the-shelf transformer turns ratio by adjusting the primary output voltage.

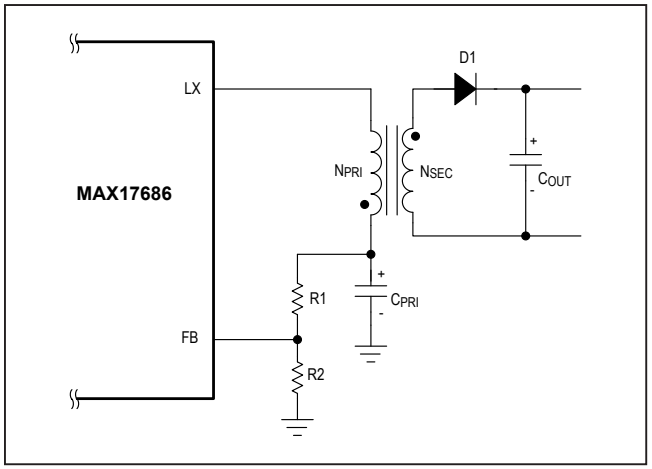


Figure 5. Adjusting the Primary Output Voltage

Primary Inductance Selection

Primary inductance value determines the ripple current in the transformer. The required primary inductance is given by the equation:

$$L_{PRI} = 7 \times V_{PRI}$$

where L_{PRI} is the primary inductance in µH and V_{PRI} is the primary output voltage.

The primary ripple current can be calculated using the equation:

$$\Delta I = \frac{V_{PRI} \times \left(1 - \frac{V_{PRI}}{V_{IN}} \right)}{f_{SW} \times L_{PRI}}$$

where L_{PRI} is the primary inductance in H, f_{SW} is the switching frequency in Hz, V_{PRI} is the primary output voltage, V_{IN} is the input voltage.

Winding Peak and RMS Currents

Windings peak and RMS current ratings should be specified for selecting the iso-buck transformer.

Primary and secondary winding peak currents are given by the equations:

$$I_{HS\_AVG} = I_{PRI} + \left(\sum_{i=1}^{n} I_{OUT_i} \times K_i \right)$$

$$I_{PK\_PRI} = I_{HS\_AVG} + \frac{\Delta I}{2}$$

$$I_{PK\_SEC_i} \cong \frac{I_{OUT_i}}{(1 - D)}$$

$$D = \frac{V_{PRI}}{V_{IN}}$$

where n is the total number of isolated outputs, i is the individual isolated output, I_{PRI} is the primary load current, I_{OUTi} is the individual secondary load current, K_i is the individual secondary turns ratio, D is the duty cycle, and ΔI is the primary ripple current.

Primary RMS current is the sum of the high-side and low-side switch RMS currents.

High-side switch RMS current:

$$I_{HS\_RMS} = \sqrt{D \times \left(I_{HS\_AVG}^2 + \frac{\Delta I^2}{12} \right)}$$

Low-side switch RMS current:

$$I_{LS\_RMS} = \sqrt{(1-D) \times \left(\left(I_{PK\_PRI} - \left(\frac{1}{(1-D)} \times \sum_{i=1}^{n} (I_{OUT_i} \times K_i) \right) \right) - \frac{\Delta I}{2})^2 + \frac{\Delta I^2}{12} \right)}$$

Primary winding RMS current:

$$I_{PRI\_RMS} = \sqrt{I_{HS\_RMS}^2 + I_{LS\_RMS}^2}$$

Secondary winding RMS current is given by the equation:

$$I_{SEC\_RMS_i} = \frac{I_{OUT_i}}{\sqrt{(1-D)}}$$

Leakage Inductance

Transformer leakage inductance (L_{LEAK}) plays a key role in determining the output voltage regulation. For better output voltage regulation, leakage inductance should be reduced to less than 1% of the primary inductance value. Higher leakage inductance also limits the amount of power delivered to the output.

Primary Negative Peak Current

The primary current can go negative when the low side switch is turned on. Steady-state primary negative peak current should be verified not to exceed -1A. The primary negative peak current can be calculated using the equation:

$$I_{NEGPK\_PRI} = I_{PK\_PRI} - \left(\frac{1}{(1-D)} \times \sum_{i=1}^{n} (I_{OUT_i} \times K_i) \right) - \Delta I$$

Specifying the Iso-Buck Transformer

An off-the-shelf transformer or coupled inductor can be used as an Iso-buck transformer. If readily not available, use the table below to specify the Iso-buck transformer parameters to transformer vendors.

Primary Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The minimum required output capacitance is given by the equation:

$$C_{PRI} = \frac{I_{HS\_AVG} \times D_{MAX}}{f_{SW} \times 0.01 \times V_{PRI}}$$

$$D_{MAX} = \frac{V_{PRI}}{V_{IN\_MIN}}$$

Where I_{OUT} is the load current, K is the turns ratio, f_{SW} is the switching frequency, V_{PRI} is the primary output voltage, V_{IN_MIN} is the minimum input voltage.

Secondary Output Capacitor Selection

A secondary side capacitor supplies load current when the high-side switch is on. The required output capacitance to support 1% steady state ripple is given by the equation:

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times 0.01 \times V_{OUT}}$$

It should be noted that dielectric materials used in ceramic capacitors exhibit capacitance loss due to DC bias levels and should be appropriately derated to ensure the required output capacitance is obtained in the application.

Table 1. Specifying Iso-Buck Transformer

PARAMETER	SYMBOL
Primary Inductance	L_{PRI}
Leakage Inductance	L_{LEAK}
Primary Ripple Current	ΔI
Primary Peak Current	I_{PK_PRI}
Primary RMS Current	I_{PRI_RMS}
Secondary Peak Current	I_{PK_SEC}
Secondary RMS Current	I_{SEC_RMS}
Working Voltage	VAC, VDC
Insulation Level	VAC, VDC

Input Capacitor Selection

Ceramic input capacitors are recommended for the IC. The input capacitor reduces peak current drawn from the power source and reduces noise and voltage ripple on the input caused by the switching circuitry. In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the input ceramic capacitor to provide necessary damping for potential oscillations caused by the longer input power path and input ceramic capacitor. The required input capacitance can be calculated using the equation:

$$C_{IN} = \frac{I_{HS\_AVG} \times D_{MAX} \times (1 - D_{MAX})}{f_{SW} \times \Delta V_{IN}}$$

$$D_{MAX} = \frac{V_{PRI}}{V_{IN\_MIN}}$$

ΔV_{IN} is the input voltage ripple, normally 2% of the minimum input voltage, D_{MAX} is the maximum duty cycle, and f_{SW} is the switching frequency of operation.

Secondary Diode Selection

A secondary rectifier diode should be rated to carry peak secondary current and to withstand reverse voltage when the high-side switch is on. A Schottky diode with less forward-voltage drop is preferred for better output voltage regulation.

The peak current rating of the diode is given by:

$$I_{PK\_DIODE_i} = \frac{I_{OUT_i}}{(1 - D)}$$

The peak reverse voltage rating of the diode is given by:

$$V_{DIODE} = 2 \times \left(\left(V_{IN\_MAX} - V_{PRI} \right) \times K + V_{OUT} \right)$$

Power dissipated in the diode can be calculated using the equation:

$$P_{DIODE} = V_D \times I_{OUT}$$

Minimum Load Requirements

Under light-load conditions, the iso-buck converter output voltage increases excessively due to the transformer leakage inductance and parasitic capacitance. Normally, a minimum load of 10% to 20% of the full load is sufficient to keep the converter output voltage regulation within ±5%. The output voltage regulation should be verified after testing prototype.

A resistor connected in series with a Zener diode (See R4, Z1 in Figure 9) can be used as an overvoltage protection circuit to limit the overvoltage under absolute no load conditions.

Soft-Start Capacitor Selection

The MAX17686 implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to GND programs the soft-start period.

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$C_{SS} = 5.55 \times t_{SS}$$

where t_{SS} is in milliseconds and C_{SS} is in nanofarads.

Setting the Input Undervoltage Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to GND (see Figure 6). Connect the center node of the divider to EN/UVLO.

Choose R1 to be 3.3MΩ max and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.218}{(V_{INU} - 1.218)}$$

where V_{INU} is the voltage at which the device is required to turn on.

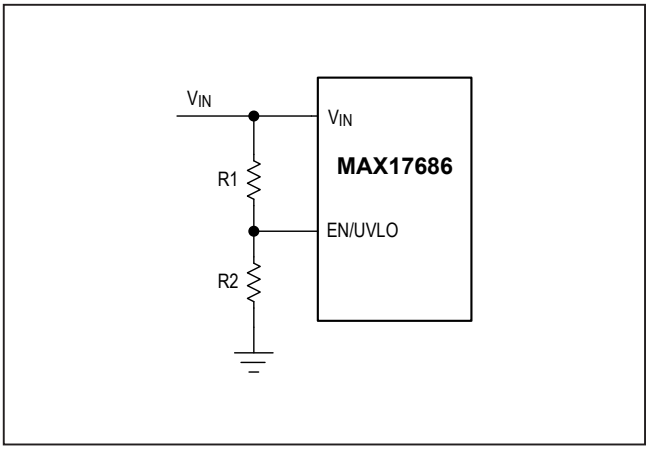


Figure 6. Adjustable EN/UVLO Network

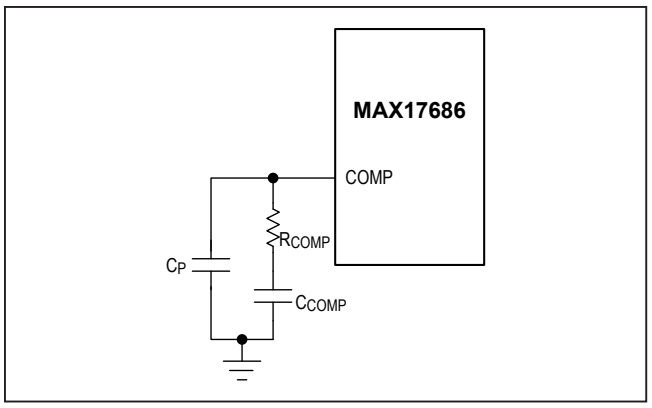


Figure 7. External Compensation Network

External Loop Compensation

The MAX17686 uses peak current-mode control scheme and needs only a simple RC network to have a stable control loop. The compensation network is shown in Figure 7. The following equations can be used for calculating the compensation components:

$$R_{COMP} = 6000 \times f_C \times \left(\begin{matrix} C_{OUT} \times (1-D) \\ \times K^2 + C_{PRI} \end{matrix} \right) \times V_{PRI}$$

where R_{COMP} is in Ω, and the maximum limit for R_{COMP} is 12kΩ. f_C is bandwidth of the converter in Hz. Choose f_C in the range of 2kHz to 10kHz.

$$C_{COMP} = \frac{5}{\pi \times f_C \times R_{COMP}}$$

$$C_P = \frac{1}{2\pi \times 50000 \times R_{COMP}}$$

Power Dissipation

Ensure that the junction temperature of the device does not exceed +125°C under the operating conditions specified for the power supply. At a particular operating condition, the power losses that lead to temperature rise of the device can be estimated as follows:

$$P_{LOSS} = P_{OUT} \times \left(\frac{1}{\eta} - 1 \right) - \left(I_{PRI\_RMS}^2 \times R_{PRI} \right) - \left(I_{SEC\_RMS}^2 \times R_{SEC} \right) - \left(V_D \times I_{OUT} \right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where P_{OUT} is the output power, η is the efficiency of power conversion, R_{PRI} is the primary resistance of the transformer, R_{SEC} is the secondary resistance of the transformer and V_D is the diode drop.

The junction temperature (T_J) of the device can be estimated at any ambient temperature (T_A) from the following equation:

$$T_J = T_A + (\theta_{JA} \times P_{LOSS})$$

where θ_{JA} is the junction-to-ambient thermal impedance of the package.

PCB Layout Guidelines

Careful PCB layout is critical to achieve clean and stable operation. For a sample layout that ensures first-pass success, refer to the MAX17686 evaluation kit layouts available at **www.maximintegrated.com**. Follow these guidelines for good PCB layout:

1) All connections carrying pulsed currents must be very short and as wide as possible. The loop area of these connections must be made very small to reduce stray inductance and radiated EMI.
2) A ceramic input filter capacitor should be placed close to the V_{IN} pin of the device. The bypass capacitor for the V_{CC} pin should also be placed close to the V_{CC} pin. External compensation components should be placed close to the IC and far from the LX node. The feedback trace should be routed as far as possible from the LX node.
3) Signal and power grounds must be kept separate. They should be connected together at a point where switching noise is minimum, typically the return terminal of the V_{CC} bypass capacitor. The ground plane should be kept continuous as much as possible.
4) Multiple thermal vias that connect to a large ground plane should be provided under the exposed pad of the device, for efficient heat dissipation.

Figure 8 show the recommended component placement for the MAX17686 iso-buck converter.

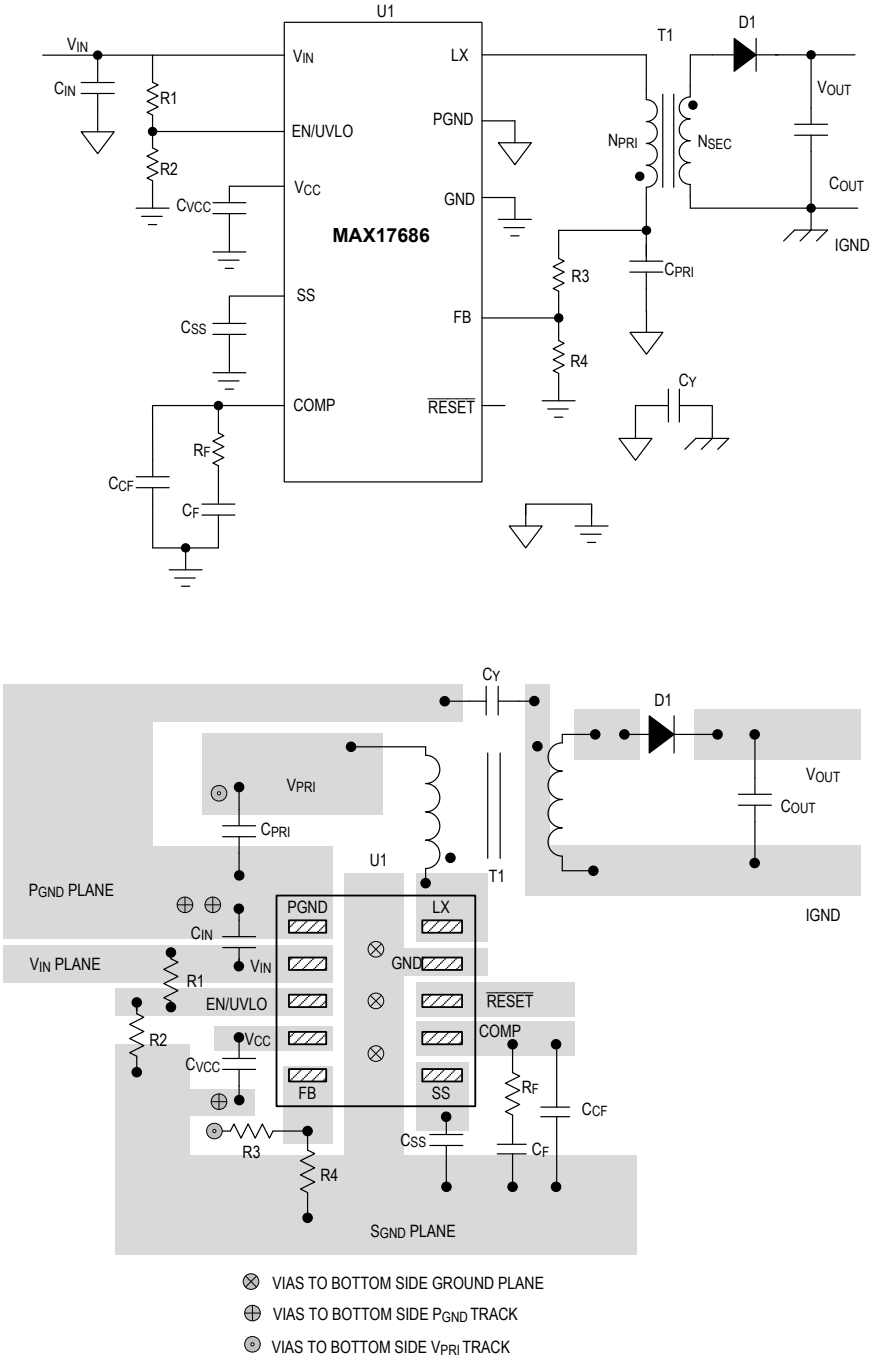


Figure 8. Recommended Component Placement

Typical Application Circuits

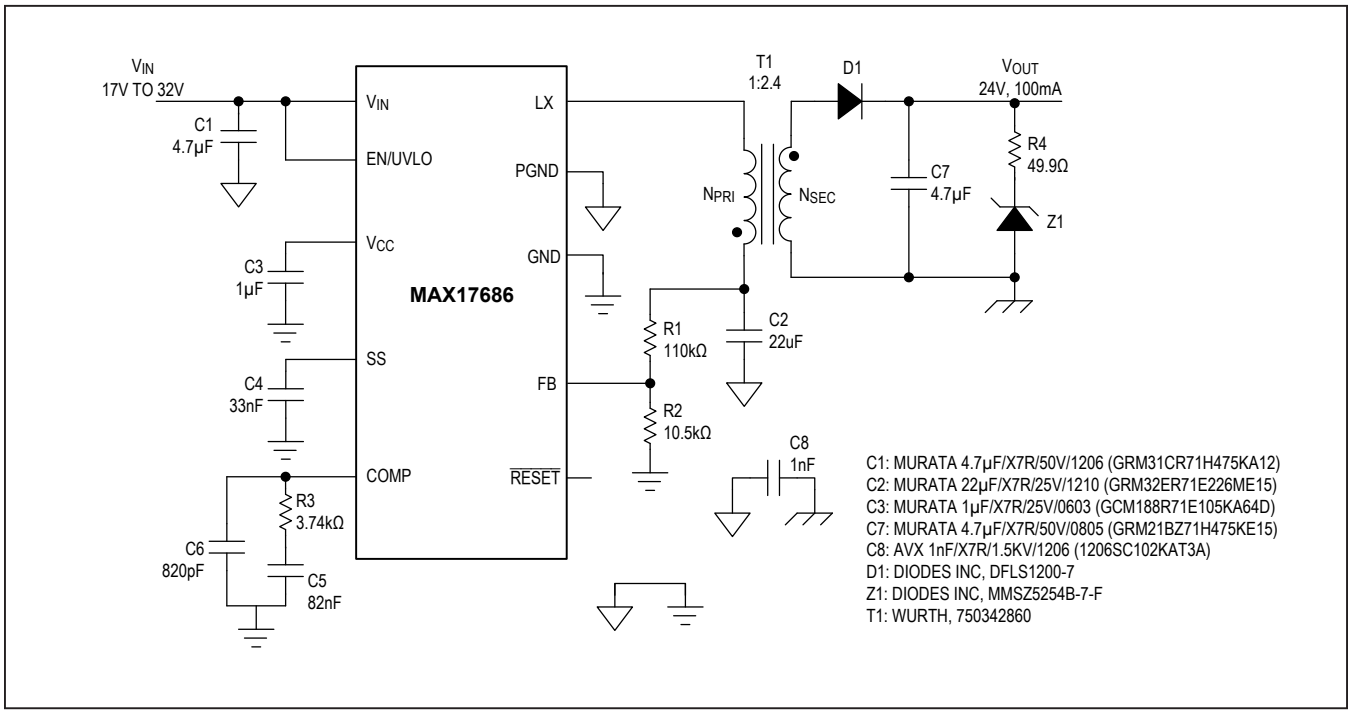


Figure 9. Low-Profile 24V to 24V, 100mA Isolated Output Application Circuit

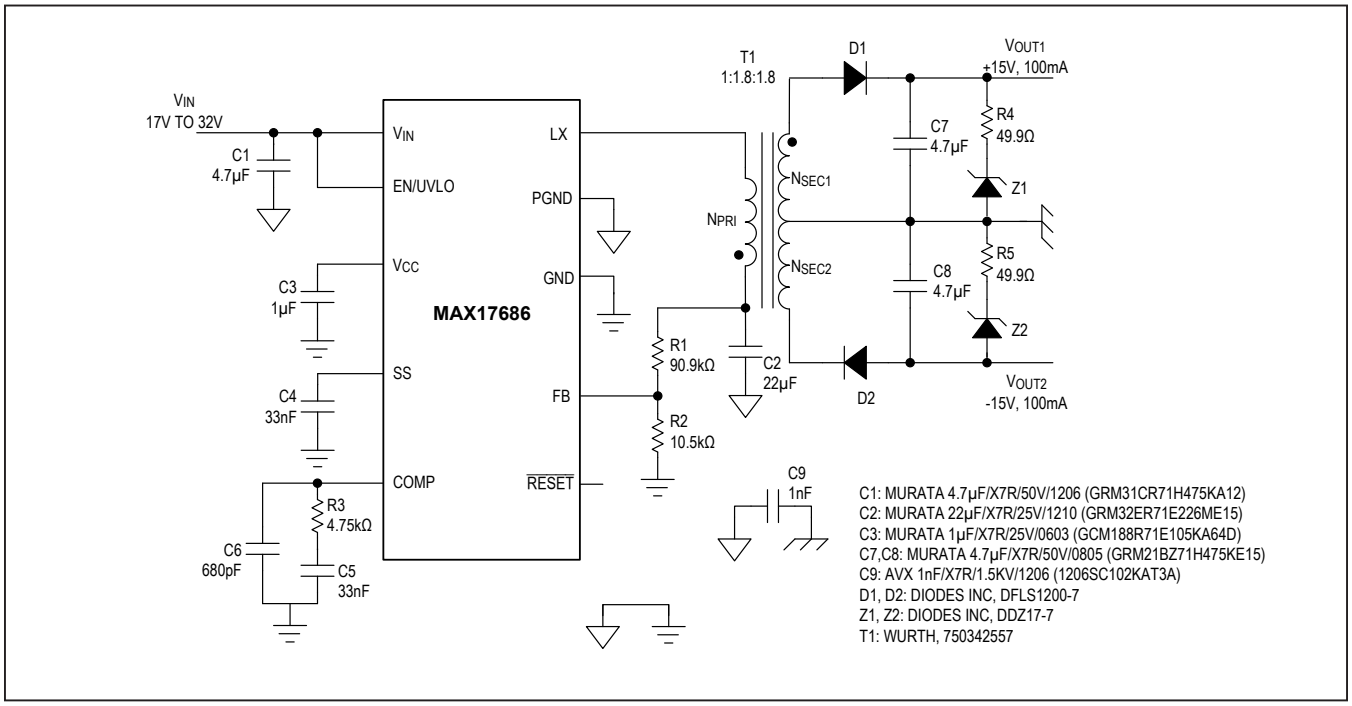


Figure 10. 24V to ±15V, 75mA Isolated Output Application Circuit

Typical Application Circuits (continued)

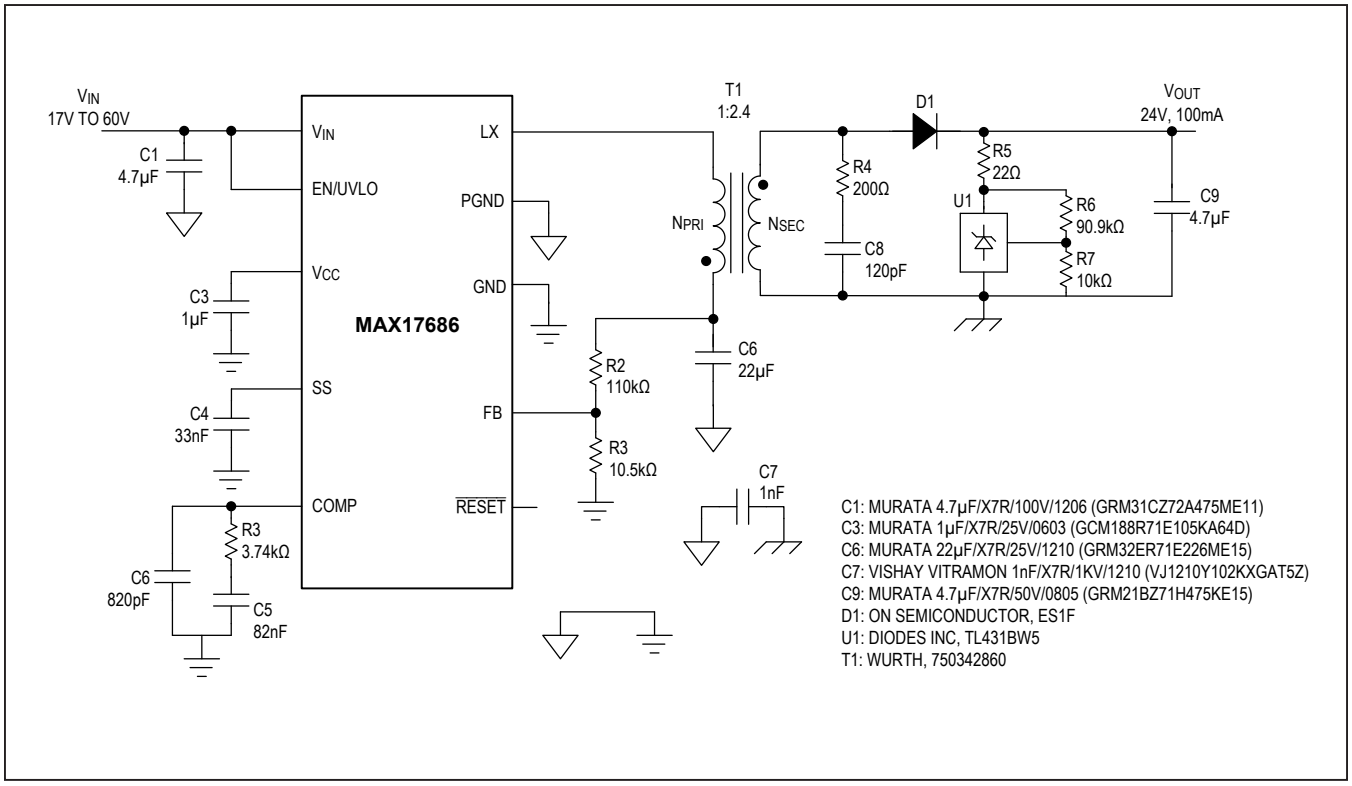


Figure 11. 24V to 3.3V/80mA Non-Isolated and ±16V,65mA Isolated Output Application circuit

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17686ATB+	-40°C to +125°C	10L TDFN-EP*

+Denotes a lead (Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/19	Initial release	—

