



## Product Change Notification / SYST-16VVUZ402

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### Date:

17-Aug-2023

### Product Category:

8-bit Microcontrollers

### PCN Type:

Document Change

### Notification Subject:

ERRATA - PIC16F18114/15/24/25/44/45 Silicon Errata and Datasheet Clarifications

### Affected CPNs:

[SYST-16VVUZ402\\_Affected\\_CPN\\_08172023.pdf](#)

[SYST-16VVUZ402\\_Affected\\_CPN\\_08172023.csv](#)

### Notification Text:

SYST-16VVUZ402

Microchip has released a new Errata for the PIC16F18114/15/24/25/44/45 Silicon Errata and Datasheet Clarifications of devices. If you are using one of these devices please read the document located at [PIC16F18114/15/24/25/44/45 Silicon Errata and Datasheet Clarifications](#).

**Notification Status:** Final

**Description of Change:**

Added new silicon revision B3; updated datasheet revision letter to 'C'; added silicon issues 1.1.2, 1.5.1 and 1.6.1.

**Impacts to Data Sheet:** None

**Change Implementation Status:** Complete

**Estimated First Ship Date:** 08 Sep 2023

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices::N/A

## Attachments:

[PIC16F18114/15/24/25/44/45 Silicon Errata and Datasheet Clarifications](#)

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Affected Catalog Part Numbers (CPN)

PIC16F18144-I/6N  
PIC16F18145-I/6N  
PIC16F18124-I/7N  
PIC16F18125-I/7N  
PIC16F18114-I/SN  
PIC16F18115-I/SN  
PIC16F18114-I/P  
PIC16F18115-I/P  
PIC16F18124-I/P  
PIC16F18125-I/P  
PIC16F18124-I/SL  
PIC16F18125-I/SL  
PIC16F18124-I/ST  
PIC16F18125-I/ST  
PIC16F18144-I/SS  
PIC16F18145-I/SS  
PIC16F18144-I/SO  
PIC16F18145-I/SO  
PIC16F18144-I/P  
PIC16F18145-I/P  
PIC16F18114-I/MD  
PIC16F18115-I/MD  
PIC16F18144T-I/6N  
PIC16F18145T-I/6N  
PIC16F18124T-I/7N  
PIC16F18125T-I/7N  
PIC16F18114T-I/SN  
PIC16F18115T-I/SN  
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PIC16F18144T-I/SS  
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PIC16F18145T-I/SO  
PIC16F18114T-I/MD  
PIC16F18115T-I/MD

# PIC16F18114/15/24/25/44/45 Silicon Errata and Datasheet Clarifications

## PIC16F18114/15/24/25/44/45



The PIC16F18114/15/24/25/44/45 devices that you have received conform functionally to the current device data sheet (DS40002404C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC16F18114/15/24/25/44/45 silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

**Table 1.** Silicon Device Identification

Part Number	Device ID	Revision ID		
		B0	B2	B3
PIC16F18114	0x3107	0xA040	0xA042	0xA043
PIC16F18115	0x310C	0xA040	0xA042	0xA043
PIC16F18124	0x3108	0xA040	0xA042	0xA043
PIC16F18125	0x310D	0xA040	0xA042	0xA043
PIC16F18144	0x3109	0xA040	0xA042	0xA043
PIC16F18145	0x310E	0xA040	0xA042	0xA043



**Important:** Refer to the **Device/Revision ID** section in the device data sheet for more detailed information on Device Identification and Revision IDs for your specific device.

## Silicon Issue Summary

**Table 2.** Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions		
				B0	B2	B3
Analog-to-Digital Converter with Computation (ADCC)	Double Sample Conversions	1.1.1	An unexpected acquisition time is added between the first and second conversions.	X		
Analog-to-Digital Converter with Computation (ADCC)	Acquisition Time	1.1.2	Acquisition time cannot be changed through either the ADACQ or ADPRE registers.	X	X	
Comparator (CMP)	Comparator 2	1.2.1	Comparator 2 is not available on 8-pin devices.	X		
Host Synchronous Serial Port (MSSP)	I <sup>2</sup> C Start and Stop Interrupt Function	1.3.1	A race condition can cause the Start and/or Stop flags to be set when I <sup>2</sup> C is enabled.	X		
Configuration Words (CONFIG)	Sleep	1.4.1	Waking from Sleep may cause unexpected behavior.	X		
Digital-to-Analog Converter (DAC)	DAC Auto Enable	1.5.1	Mid-band voltage spike at code 128 may occur when $\overline{\text{DACAUTOEN}}$ is enabled and the application is incrementing the DACxDATL register from 127 to 129.	X	X	
Fixed Voltage Reference (FVR)	ADC Buffer	1.6.1	Power-down current ( $I_{\text{PD}}$ ) for the ADC FVR Buffer may be higher than the current data sheet limits.			X

**Note:** Only those issues indicated in the last column apply to the current silicon revision.

# 1. Silicon Errata Issues

**CAUTION**

**Notice:** This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

## 1.1 Module: Analog-to-Digital Converter with Computation (ADCC)

### 1.1.1 Double Sample Conversions

When enabling a Double Sample Conversion ( $DSEN = 1$ ) with no Precharge time ( $ADPRE = 0$ ) and no Acquisition time ( $ADACQ = 0$ ), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

#### Work around

##### Method 1:

Disable Double Sample Conversion ( $DSEN = 0$ ) and perform two single conversions back to back.

##### Method 2:

If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

#### Affected Silicon Revisions

B0	B2	B3					
X							

### 1.1.2 Acquisition Time Cannot Be Changed through Either the ADACQ or the ADPRE Registers

ADC acquisition (sample) time cannot be modified by writing to either the ADPRE or ADACQ registers. Writes to the ADPRE or ADACQ registers will correctly delay the next conversion but will have no affect on increasing the actual sample time of the current conversion. For example, if the ADCRC is used as the clock source, the sample time will be nominally  $3.33 \mu s$ , regardless of the values in either of the ADACQ or ADPRE registers.

#### Work around

There is essentially no work around for increasing the sample times via the ADPRE or ADACQ registers; however, there are various work arounds and/or techniques that can be implemented to acquire a more accurate ADC measurement.

- If the ADC is using the  $F_{OSC}$ , reducing the clock speed at the time of measurement will increase the overall sampling time
  - Use the NOSCON/NDIV bits of OSCCON1 to reduce the oscillator speed
  - Adjust the ADCLK divider value to reduce the oscillator speed
  - Switch the ADC clock to the ADCRC
- The source input impedance ( $R_S$ ) directly effects the amount of time it takes to charge the  $C_{HOLD}$  capacitor. Reducing the input impedance to a minimum will help reduce the sample time needed for the ADC measurement.

#### Affected Silicon Revisions

B0	B2	B3					

X	X						
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## 1.2 Module: Comparator (CMP)

### 1.2.1 Comparator 2 Is Not Available

Comparator 2 is not available on 8-pin devices.

#### Work around

None.

#### Affected Silicon Revisions

B0	B2	B3				
X						

## 1.3 Module: MSSP

### 1.3.1 The I<sup>2</sup>C Start and/or Stop Flags May Be Set When I<sup>2</sup>C Is Enabled

When I<sup>2</sup>C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I<sup>2</sup>C interrupts if enabled.

#### Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I<sup>2</sup>C module.
3. Wait 250 ns + six instructions cycles ( $F_{OSC}/4$ ).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions if used.

```

SSPxCON3bits.SCIE = 0;           // Disable Start condition interrupt
SSPxCON3bits.PCIE = 0;         // Disable Stop condition interrupt
SSPxCON1bits.SSPEN = 1;        // Enable I2C
Delay();                        // Wait for 250 ns + 6 instruction cycles (Fosc/4)
PIRxbits.SSPxIF = 0;          // Clear the MSSP interrupt flag
SSPxCON3bits.SCIE = 1;         // Enable Start condition interrupt if used
SSPxCON3bits.PCIE = 1;         // Enable Stop condition interrupt if used

```

#### Affected Silicon Revisions

B0	B2	B3				
X						

## 1.4 Module: Configuration Words (CONFIG)

### 1.4.1 Waking from Sleep May Cause Unexpected Behavior

Waking from Sleep may cause unexpected behavior.

#### Work around

Do not use the SLEEP instruction. If clock switching is available and there is a need for reduced current consumption, switch to the slowest system clock.

#### Affected Silicon Revisions

B0	B2	B3				
X						

## 1.5 Module: Digital-to-Analog Converter (DAC)

### 1.5.1 Mid-band Voltage Spike at Code 128 May Occur when DACAUTOEN Is Enabled and the Application Is Incrementing the DACxDATL Register from 127 to 129

When the DACAUTOEN bit is enabled, a voltage glitch on the DACxOUT pin may occur at code 128 when the application is incrementing the DACxDATL register from 127 to 129 and the alternate DACxOUT pin is either tied to GND or  $V_{DD}$ . If the alternate pin is tied to  $V_{DD}$ , the glitch will be positive; if the pin is tied to GND, the glitch will be negative.

#### Work around

None.

#### Affected Silicon Revisions

B0	B2	B3					
X	X						

## 1.6 Module: Fixed Voltage Reference (FVR)

### 1.6.1 Power-down Current ( $I_{PD}$ ) for the ADC FVR Buffer May Be Higher than the Current Data Sheet Limits

When using the ADC FVR Buffer as an ADC reference, the  $I_{PD}$  current may be higher than the current data sheet limits. The parameters for **B3** silicon are as follows:

Param. No.	Sym.	Device Characteristics	Min.	Typ.†	Max. +85°C	Max. +125°C	Units	Conditions	
								$V_{DD}$	Note
D204	$I_{PD\_FVR\_BUF1}$	FVR Buffer 1 (ADC)	—	171	420	485	$\mu A$	3.0V	

#### Work around

None.

#### Affected Silicon Revisions

B0	B2	B3					
		X					



## 2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002404C):

**Note:**

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

### 2.1 None

There are no known data sheet clarifications as of this publication date.

### 3. Appendix A: Revision History

Doc Rev.	Date	Comments
C	08/2023	Added new silicon revision B3; updated datasheet revision letter to 'C'; added silicon issues 1.1.2, 1.5.1, and 1.6.1.
B	9/2022	Added new silicon revision B2; updated datasheet revision letter to 'B'; adding silicon issue 1.4.1.
A	3/2022	Initial release of this document.

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