



Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



4-Mbit (256K words × 16-bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
 - $t_{AA} = 10 \text{ ns}/15 \text{ ns}$
- Embedded ECC for single-bit error correction^[1, 2]
- Low active and standby currents
 - Active current: $I_{CC} = 38 \text{ mA}$ typical
 - Standby current: $I_{SB2} = 6 \text{ mA}$ typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Pb-free 44-pin SOJ, 44-pin TSOP II, and 48-ball VFBGA packages

Functional Description

CY7C1041G and CY7C1041GE are high-performance CMOS fast static RAM devices with embedded ECC. Both devices are offered in single chip-enable option and in multiple pin configurations. The CY7C1041GE device includes an ERR pin that signals an error-detection and correction event during a read cycle.

Data writes are performed by asserting the Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW, while providing the data on I/O₀ through I/O₁₅ and address on A₀ through A₁₇ pins. The Byte High Enable (\overline{BHE}) and Byte Low Enable (\overline{BLE}) inputs control write operations to the upper and lower bytes of the specified memory location. \overline{BHE} controls I/O₈ through I/O₁₅ and \overline{BLE} controls I/O₀ through I/O₇.

Data reads are performed by asserting the Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) inputs LOW and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O₀ through I/O₁₅). Byte accesses can be performed by asserting the required byte enable signal (\overline{BHE} or \overline{BLE}) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O₀ through I/O₁₅) are placed in a high-impedance state during the following events:

- The device is deselected (\overline{CE} HIGH)
- The control signals (\overline{OE} , \overline{BLE} , \overline{BHE}) are de-asserted

On the CY7C1041GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = HIGH)^[1]. See the [Truth Table on page 14](#) for a complete description of read and write modes.

The logic block diagram is on page 2.

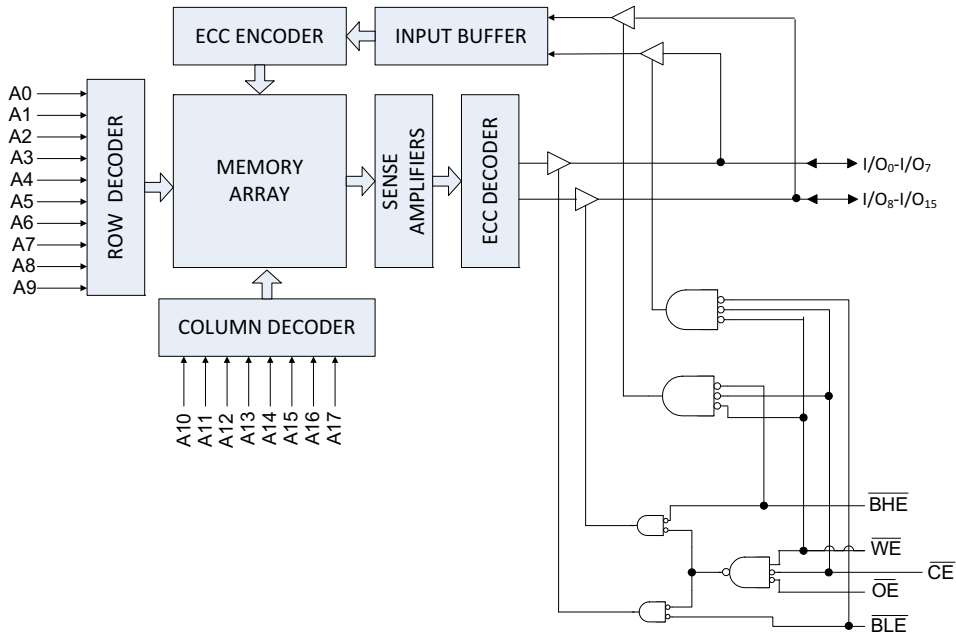
Product Portfolio

Product ^[3]	Features and Options (see Pin Configurations on page 4)	Range	V _{CC} Range (V)	Speed (ns) 10/15	Power Dissipation			
					Operating I _{CC} , (mA)		Standby, I _{SB2} (mA)	
					f = f _{max}			
					Typ ^[4]	Max	Typ ^[4]	Max
CY7C1041G(E)18	Single Chip Enable	Industrial	1.65 V–2.2 V	15	–	40	6	8
CY7C1041G(E)30	Optional ERR pins		2.2 V–3.6 V	10	38	45		
CY7C1041G(E)			4.5 V–5.5 V	10	38	45		

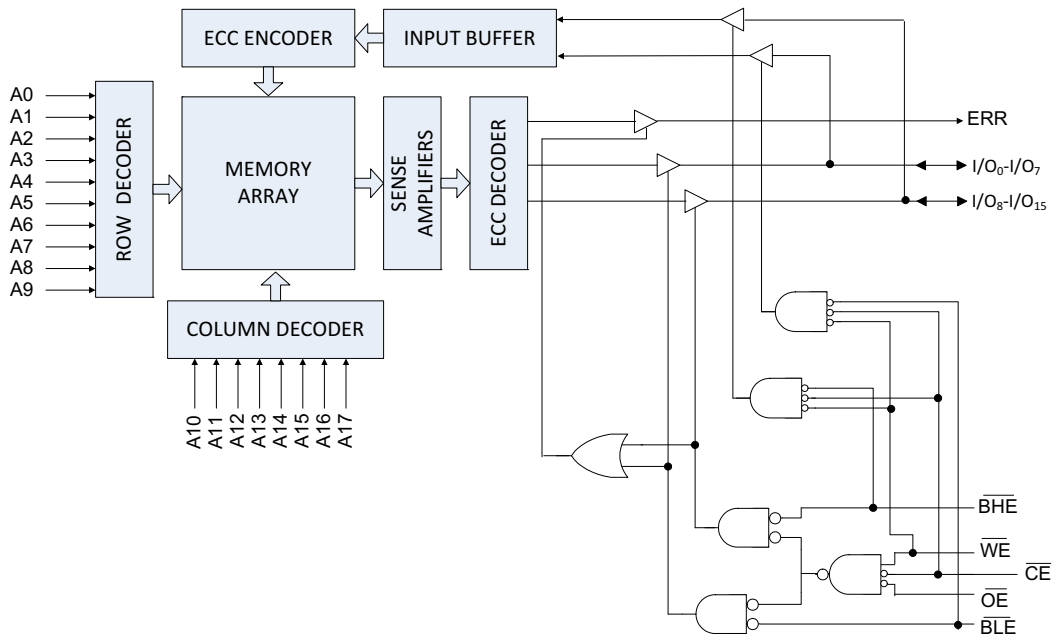
Notes

1. This device does not support automatic write-back on error detection.
2. SER FIT Rate <0.1 FIT/Mb. Refer [AN88889](#) for details.
3. The ERR pin is available only for devices which have ERR option "E" in the ordering code. Refer [Ordering Information on page 15](#) for details.
4. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY7C1041G



Logic Block Diagram – CY7C1041GE



Contents

Pin Configurations	4	Ordering Information	15
Maximum Ratings	6	Ordering Code Definitions	16
Operating Range	6	Package Diagrams	17
DC Electrical Characteristics	6	Acronyms	19
Capacitance	7	Document Conventions	19
Thermal Resistance	7	Units of Measure	19
AC Test Loads and Waveforms	7	Document History Page	20
Data Retention Characteristics	8	Sales, Solutions, and Legal Information	21
Data Retention Waveform	8	Worldwide Sales and Design Support	21
AC Switching Characteristics	9	Products	21
Switching Waveforms	10	PSoC® Solutions	21
Truth Table	14	Cypress Developer Community	21
ERR Output – CY7C1041GE	14	Technical Support	21

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable without ERR, CY7C1041G ^[5], Package/Grade ID: BVXI ^[7]

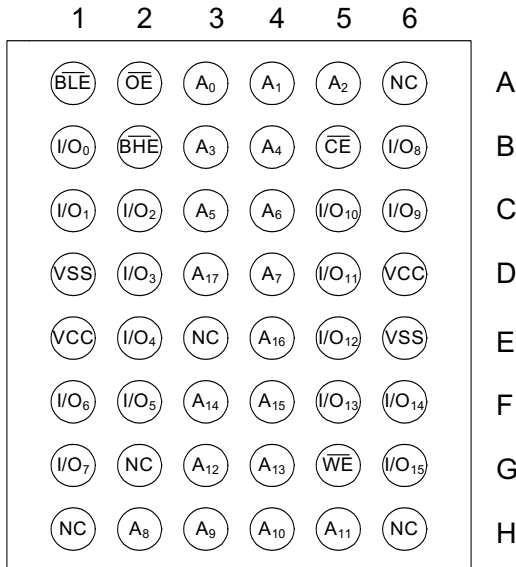


Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable with ERR, CY7C1041GE ^[5, 6], Package/Grade ID: BVXI ^[7]

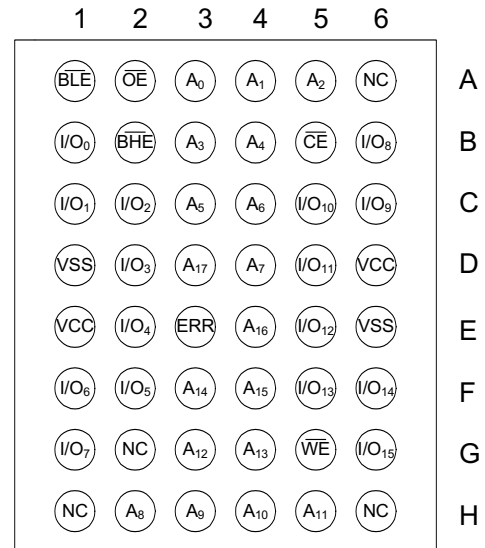


Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable without ERR, CY7C1041G ^[5], Package/Grade ID: BVJXI ^[7]

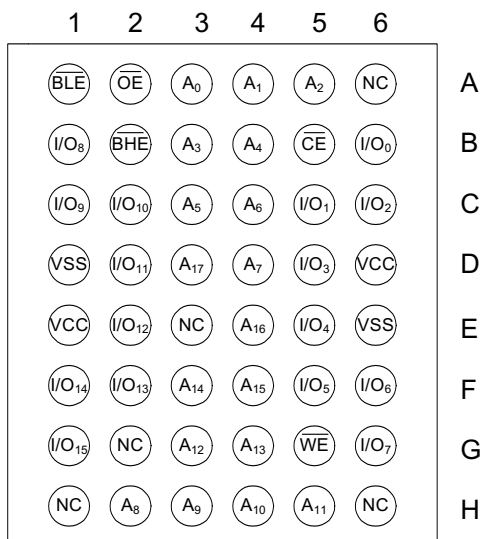
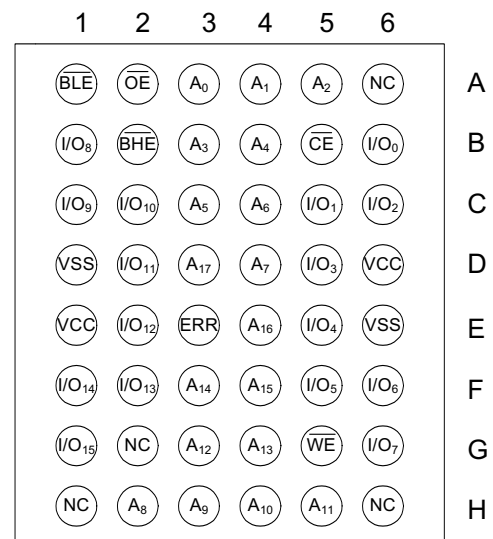


Figure 4. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable with ERR, CY7C1041GE ^[5, 6], Package/Grade ID: BVJXI ^[7]



Notes

- NC pins are not connected internally to the die.
- ERR is an output pin.
- Package type BVJXI is JEDEC compliant compared to package type BVXI. The difference between the two is that the higher and lower byte I/Os (I/O_[7:0] and I/O_[15:8] balls are swapped).

Pin Configurations (continued)

Figure 5. 44-pin TSOP II/44-pin SOJ Single Chip Enable with ERR, CY7C1041GE [8, 9]

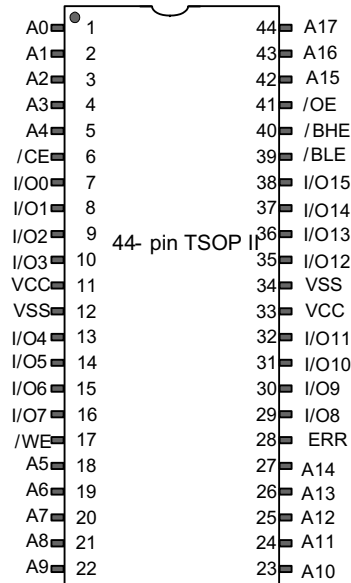
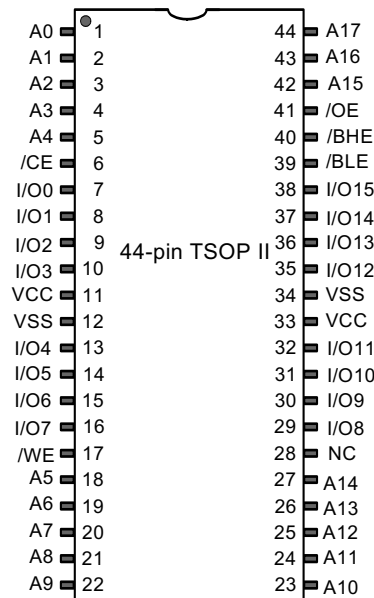


Figure 6. 44-pin TSOP II/44-pin SOJ Single Chip Enable without ERR, CY7C1041G [8]



Notes

- 8. NC pins are not connected internally to the die.
- 9. ERR is an output pin.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C
 Ambient temperature
 with power applied -55 °C to +125 °C
 Supply voltage
 on V_{CC} relative to GND ^[10] -0.5 V to $V_{CC} + 0.5$ V
 DC voltage applied to outputs
 in HI-Z State ^[10] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[10] -0.5 V to $V_{CC} + 0.5$ V
 Current into outputs (in LOW state) 20 mA
 Static discharge voltage
 (MIL-STD-883, Method 3015) > 2001 V
 Latch-up current > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

Parameter	Description	Test Conditions	10 ns/15 ns			Unit	
			Min	Typ ^[11]	Max		
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	$V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	1.4	-	-	V
		2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2	-	-	
		2.7 V to 3.0 V	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.2	-	-	
		3.0 V to 3.6 V	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	-	
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	-	
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	$V_{CC} - 0.5$ ^[12]	-	-	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	$V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$	-	-	0.2	V
		2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OL} = 2 \text{ mA}$	-	-	0.4	
		2.7 V to 3.6 V	$V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	-	-	0.4	
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	-	-	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V	-	1.4	-	$V_{CC} + 0.2$ ^[10]	V
		2.2 V to 2.7 V	-	2	-	$V_{CC} + 0.3$ ^[10]	
		2.7 V to 3.6 V	-	2	-	$V_{CC} + 0.3$ ^[10]	
		4.5 V to 5.5 V	-	2	-	$V_{CC} + 0.5$ ^[10]	
V_{IL}	Input LOW voltage	1.65 V to 2.2 V	-	-0.2 ^[10]	-	0.4	V
		2.2 V to 2.7 V	-	-0.3 ^[10]	-	0.6	
		2.7 V to 3.6 V	-	-0.3 ^[10]	-	0.8	
		4.5 V to 5.5 V	-	-0.5 ^[10]	-	0.8	
I_{IX}	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1	-	+1	μA	
I_{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, Output disabled	-1	-	+1	μA	
I_{CC}	Operating supply current	Max V_{CC} , $I_{OUT} = 0 \text{ mA}$, CMOS levels	f = 100 MHz	-	38	45	mA
			f = 66.7 MHz	-	-	40	
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	-	-	15	mA	
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, f = 0	-	6	8	mA	

Notes

10. $V_{L(\text{min})} = -2.0 \text{ V}$ and $V_{H(\text{max})} = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8 \text{ V}$ (for V_{CC} range of 1.65 V – 2.2 V), $V_{CC} = 3 \text{ V}$ (for V_{CC} range of 2.2 V – 3.6 V), and $V_{CC} = 5 \text{ V}$ (for V_{CC} range of 4.5 V – 5.5 V), $T_A = 25 \text{ }^\circ\text{C}$.

12. This parameter is guaranteed by design and not tested.

Capacitance

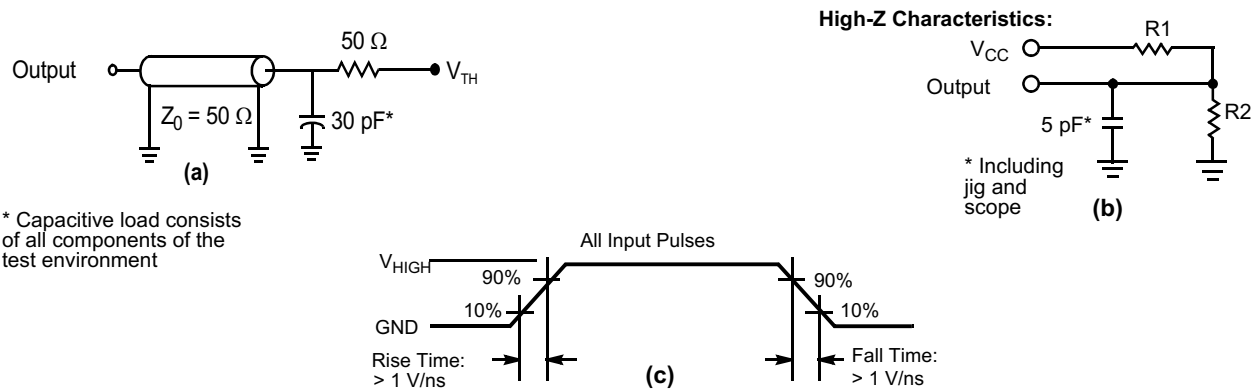
Parameter ^[13]	Description	Test Conditions	48-ball VFBGA	44-pin SOJ	44-pin TSOP II	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	10	10	pF
C _{OUT}	I/O capacitance		10	10	10	pF

Thermal Resistance

Parameter ^[13]	Description	Test Conditions	48-ball VFBGA	44-pin SOJ	44-pin TSOP II	Unit
θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.35	55.37	68.85	°C/W
θ _{JC}	Thermal resistance (junction to case)		14.74	30.41	15.97	°C/W

AC Test Loads and Waveforms

Figure 7. AC Test Loads and Waveforms ^[14]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V _{TH}	0.9	1.5	1.5	V
V _{HIGH}	1.8	3	3	V

Notes

13. Tested initially and after any design or process changes that may affect these parameters.

14. Full-device AC operation assumes a 100-μs ramp time from 0 to V_{CC(min)} and a 100-μs wait time after V_{CC} stabilization.

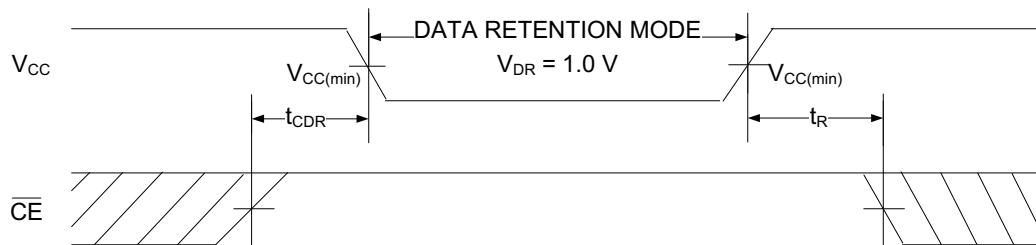
Data Retention Characteristics

Over the operating range of $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	V
I_{CCDR}	Data retention current	$V_{CC} = 1.2\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ ^[15] , $V_{IN} \geq V_{CC} - 0.2\text{ V}$, or $V_{IN} \leq 0.2\text{ V}$	–	8	mA
t_{CDR} ^[16]	Chip deselect to data retention time		0	–	ns
t_R ^[15, 16]	Operation recovery time	$V_{CC} \geq 2.2\text{ V}$	10	–	ns
		$V_{CC} < 2.2\text{ V}$	15	–	ns

Data Retention Waveform

Figure 8. Data Retention Waveform ^[15]



Notes

15. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ $\geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)}$ $\geq 100\text{ }\mu\text{s}$.
16. These parameters are guaranteed by design.

AC Switching Characteristics

Over the operating range of $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$

Parameter ^[17]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	10	–	15	–	ns
t_{AA}	Address to data / ERR valid	–	10	–	15	ns
t_{OHA}	Data / ERR hold from address change	3	–	3	–	ns
t_{ACE}	\overline{CE} LOW to data / ERR valid	–	10	–	15	ns
t_{DOE}	\overline{OE} LOW to data / ERR valid	–	4.5	–	8	ns
t_{LZOE}	\overline{OE} LOW to low impedance ^[18]	0	–	0	–	ns
t_{HZOE}	\overline{OE} HIGH to HI-Z ^[18, 19]	–	5	–	8	ns
t_{LZCE}	\overline{CE} LOW to low impedance ^[18]	3	–	3	–	ns
t_{HZCE}	\overline{CE} HIGH to HI-Z ^[18, 19]	–	5	–	8	ns
t_{PU}	\overline{CE} LOW to power-up ^[19, 18]	0	–	0	–	ns
t_{PD}	\overline{CE} HIGH to power-down ^[19, 18]	–	10	–	15	ns
t_{DBE}	Byte enable to data valid	–	4.5	–	8	ns
t_{LZBE}	Byte enable to low impedance ^[18]	0	–	0	–	ns
t_{HZBE}	Byte disable to HI-Z ^[19]	–	6	–	8	ns
Write Cycle ^[20, 21]						
t_{WC}	Write cycle time	10	–	15	–	ns
t_{SCE}	\overline{CE} LOW to write end	7	–	12	–	ns
t_{AW}	Address setup to write end	7	–	12	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	\overline{WE} pulse width	7	–	12	–	ns
t_{SD}	Data setup to write end	5	–	8	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	\overline{WE} HIGH to low impedance ^[18]	3	–	3	–	ns
t_{HZWE}	\overline{WE} LOW to HI-Z ^[19]	–	5	–	8	ns
t_{BW}	Byte Enable to write end	7	–	12	–	ns

Notes

17. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3\text{ V}$) and $V_{CC}/2$ (for $V_{CC} < 3\text{ V}$), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3\text{ V}$) and 0 to V_{CC} (for $V_{CC} < 3\text{ V}$). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 7 on page 7, unless specified otherwise.
18. t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{HZBE} , t_{LZOE} , t_{LZCE} , t_{LZWE} , and t_{LZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 7 on page 7. Transition is measured $\pm 200\text{ mV}$ from steady state voltage.
19. These parameters are guaranteed by design and are not tested.
20. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and \overline{BHE} or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
21. The minimum write cycle pulse width in Write Cycle No 2 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to sum of t_{sd} and t_{HZWE} .

Switching Waveforms

Figure 9. Read Cycle No. 1 of CY7C1041G (Address Transition Controlled) [22, 23]

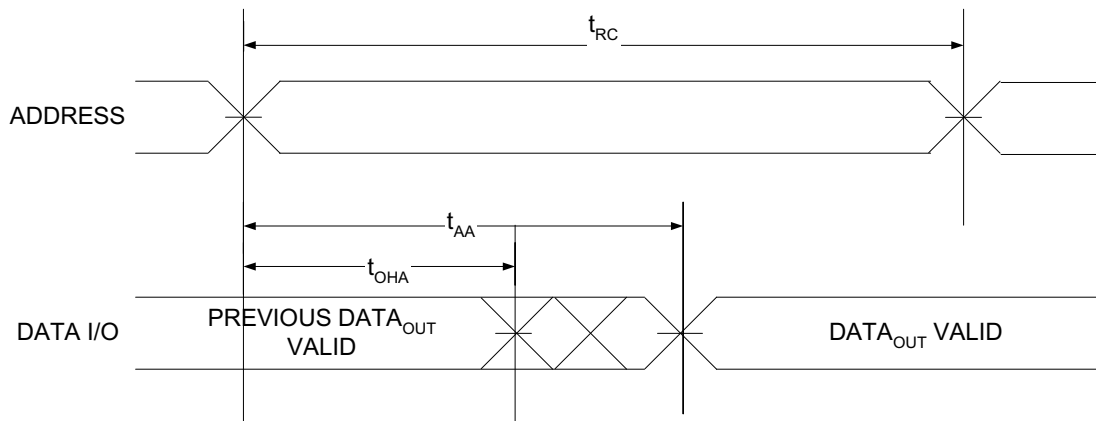
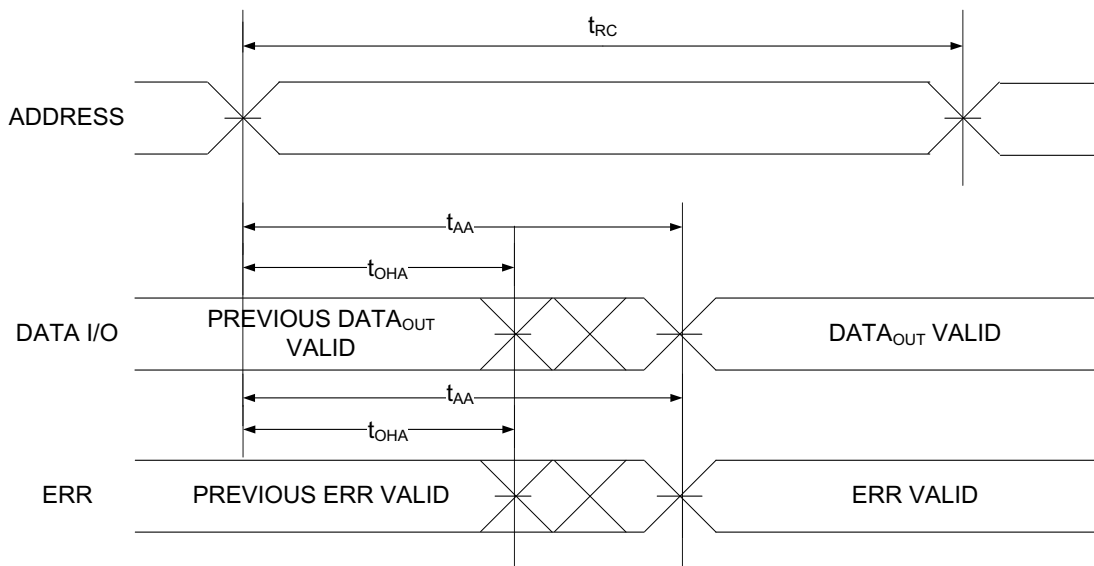


Figure 10. Read Cycle No. 1 of CY7C1041GE (Address Transition Controlled) [22, 23]

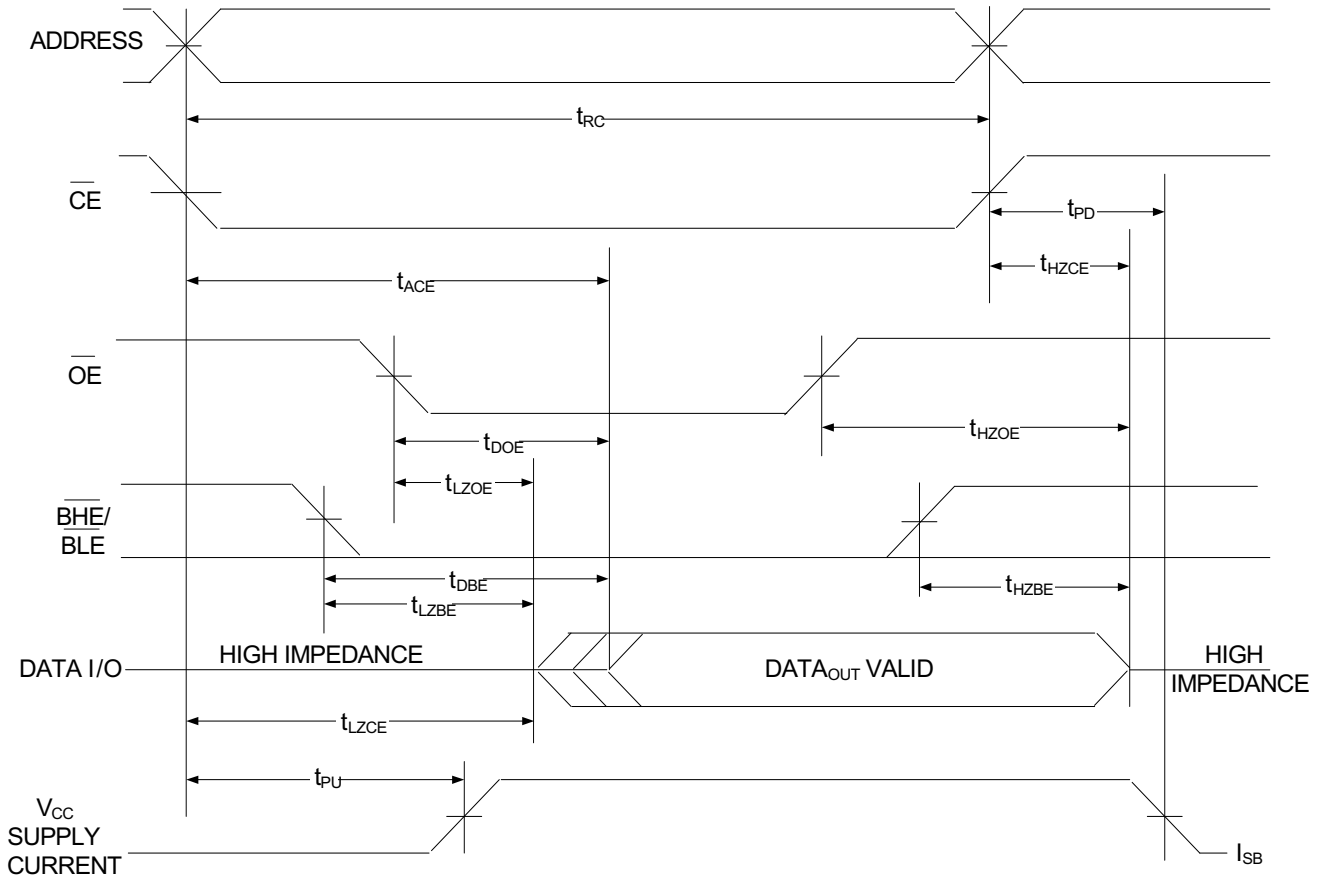


Notes

22. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} .
23. \overline{WE} is HIGH for the read cycle.

Switching Waveforms (continued)

Figure 11. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [24, 25]



Notes

- 24. $\overline{\text{WE}}$ is HIGH for the read cycle.
- 25. Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.

Switching Waveforms (continued)

Figure 12. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [26, 27]

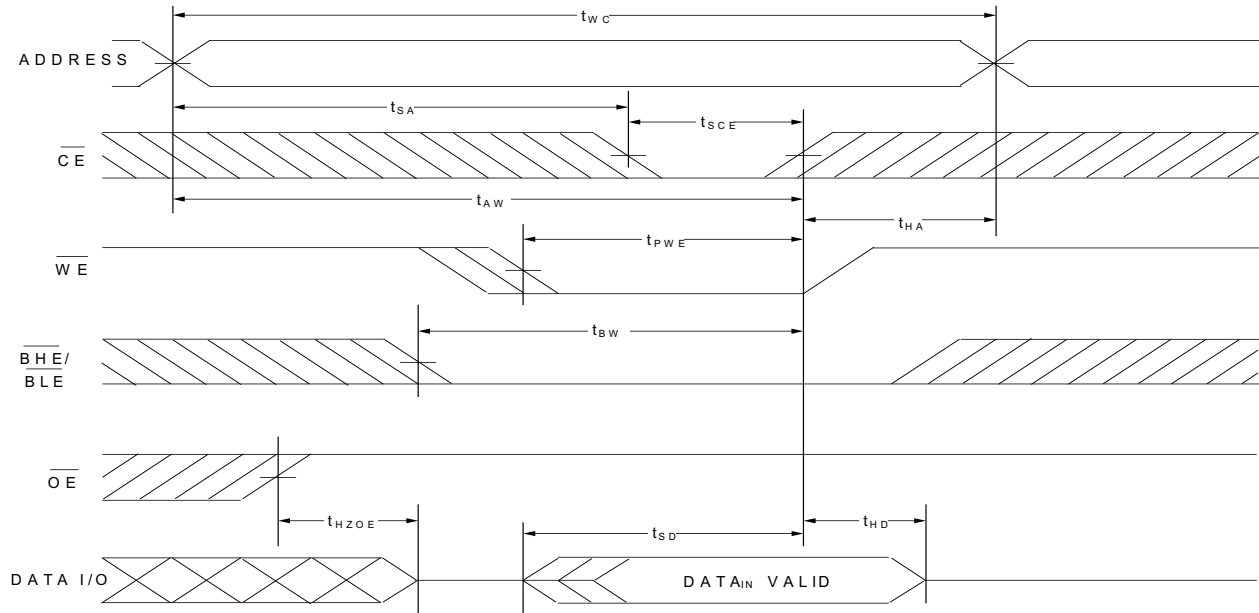
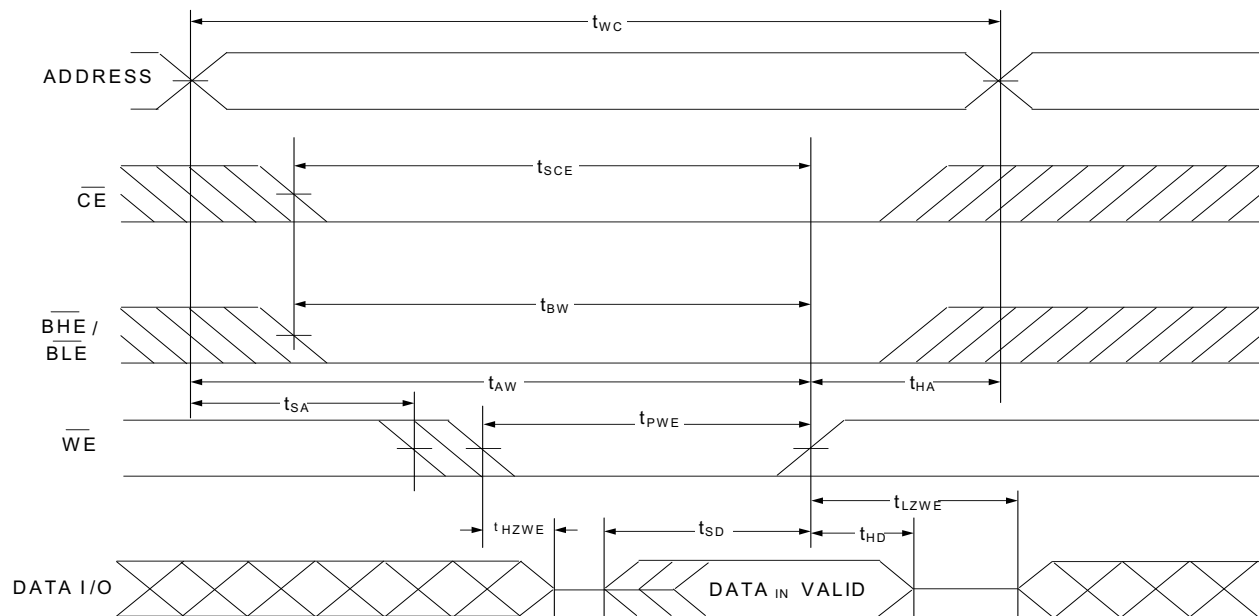


Figure 13. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [26, 27, 28]



Notes

26. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$, and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{\text{IL}}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

27. Data I/O is in HI-Z state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$, or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.

28. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE} .

Switching Waveforms (continued)

Figure 14. Write Cycle No. 3 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled) [29, 30]

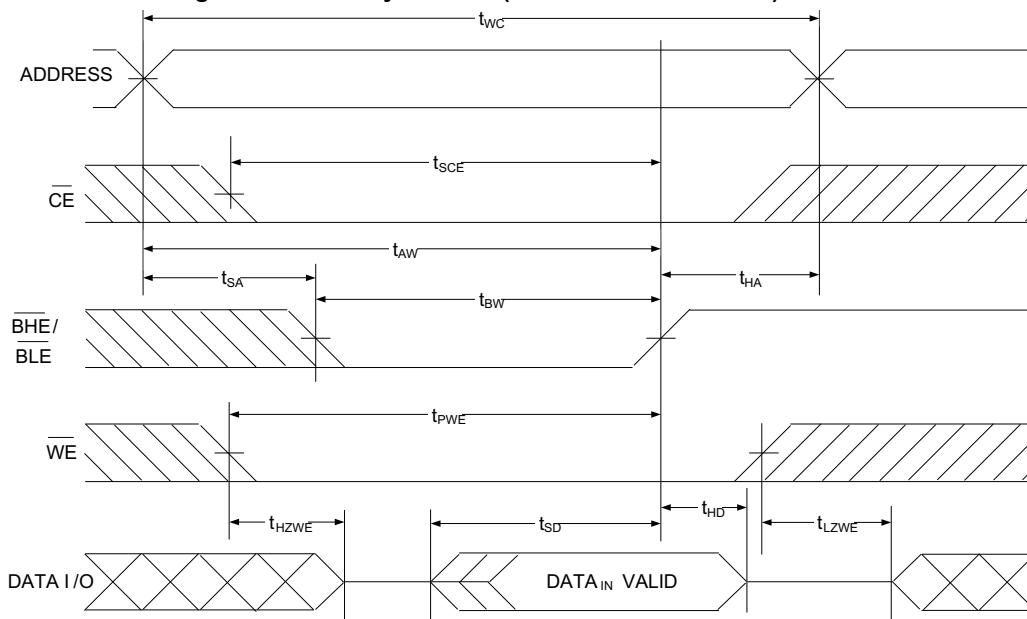
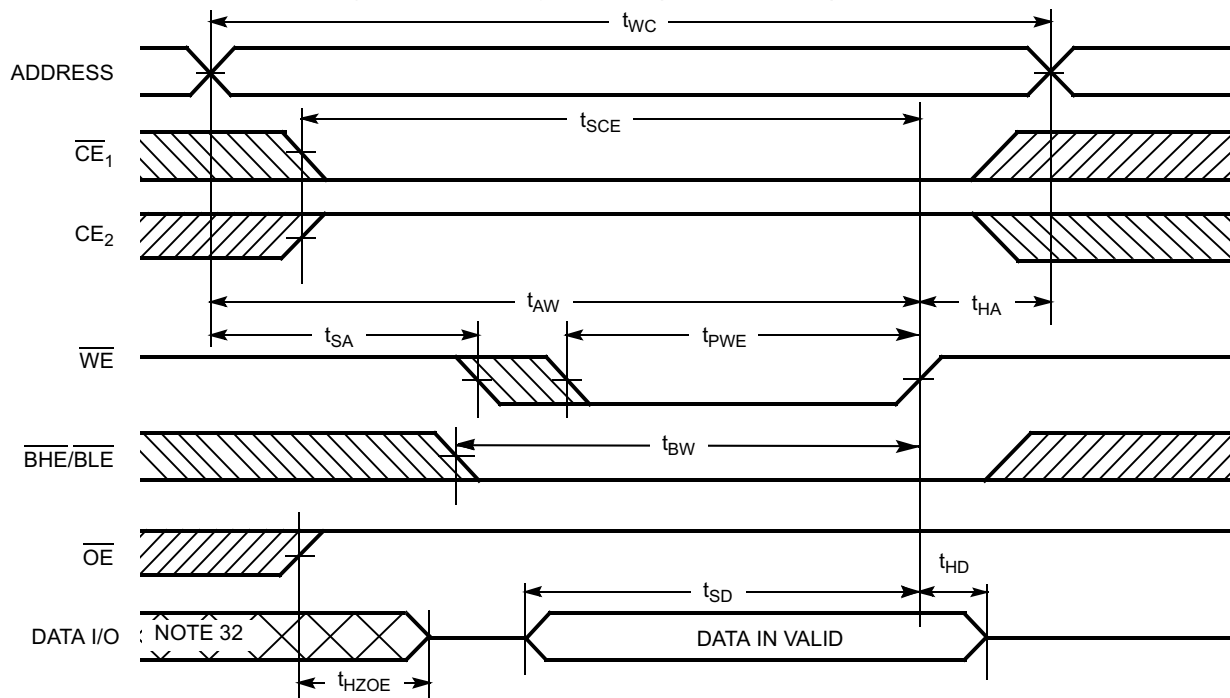


Figure 15. Write Cycle No. 4 ($\overline{\text{WE}}$ Controlled) [29, 30, 31]



Notes

- 29. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$, and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 30. Data I/O is in HI-Z state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$, or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{IH}$.
- 31. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
- 32. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X ^[33]	X ^[33]	X ^[33]	X ^[33]	HI-Z	HI-Z	Power down	Standby (I _{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I _{CC})
L	L	H	L	H	Data out	HI-Z	Read lower bits only	Active (I _{CC})
L	L	H	H	L	HI-Z	Data out	Read upper bits only	Active (I _{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I _{CC})
L	X	L	L	H	Data in	HI-Z	Write lower bits only	Active (I _{CC})
L	X	L	H	L	HI-Z	Data in	Write upper bits only	Active (I _{CC})
L	H	H	X	X	HI-Z	HI-Z	Selected, outputs disabled	Active (I _{CC})
L	X	X	H	H	HI-Z	HI-Z	Selected, outputs disabled	Active (I _{CC})

ERR Output – CY7C1041GE

Output ^[34]	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
HI-Z	Device deselected or outputs disabled or Write operation

Notes

33. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

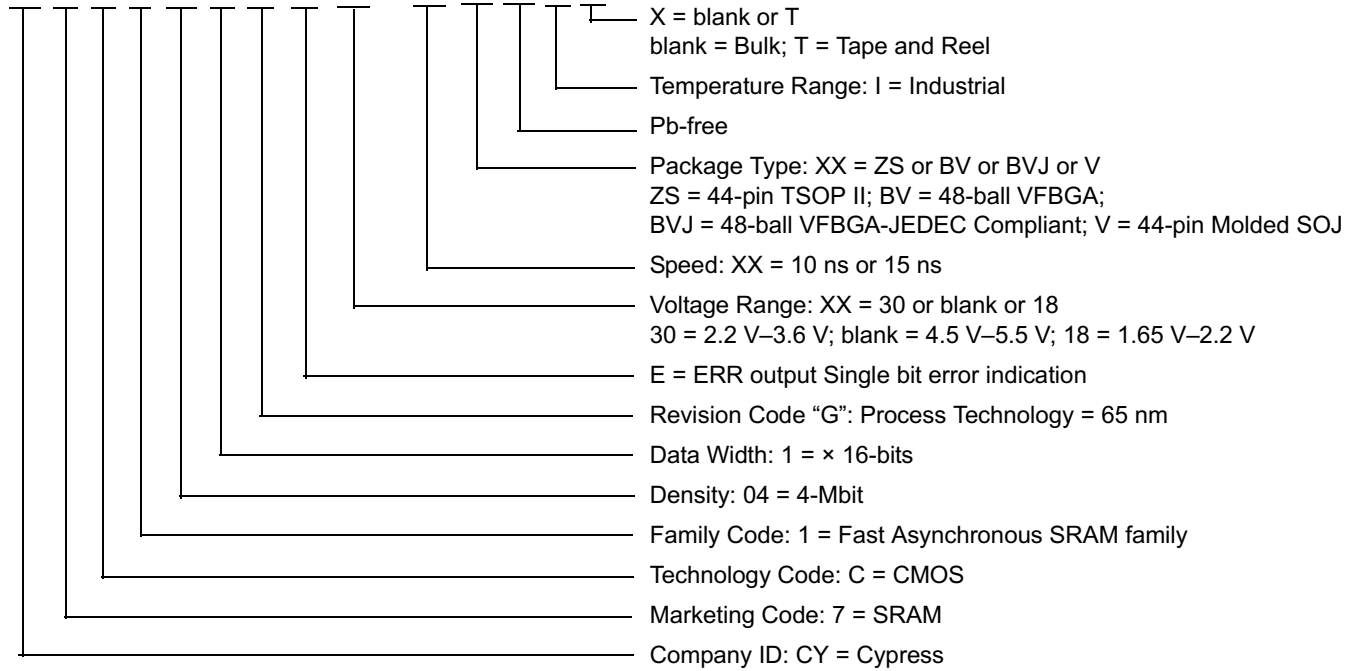
34. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7C1041GE30-10ZSXI	51-85087	44-pin TSOP II, ERR output	Industrial
		CY7C1041GE30-10ZSXIT	51-85087	44-pin TSOP II, ERR output, Tape and Reel	
		CY7C1041G30-10ZSXI	51-85087	44-pin TSOP II	
		CY7C1041G30-10ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	
		CY7C1041GE30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), ERR output	
		CY7C1041GE30-10BVXIT	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), ERR output, Tape and Reel	
		CY7C1041G30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm)	
		CY7C1041G30-10BVXIT	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), Tape and Reel	
		CY7C1041G30-10BVJXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), JEDEC	
		CY7C1041G30-10BVJXIT	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), JEDEC, Tape and Reel	
		CY7C1041G30-10VXI	51-85082	44-pin SOJ (400 Mils)	
		CY7C1041G30-10VXIT	51-85082	44-pin SOJ (400 Mils), Tape and Reel	
		CY7C1041GE30-10VXI	51-85082	44-pin SOJ (400 Mils), ERR output	
		CY7C1041GE30-10VXIT	51-85082	44-pin SOJ (400 Mils), ERR output, Tape and Reel	
	4.5 V–5.5 V	CY7C1041G-10ZSXI	51-85087	44-pin TSOP II	
		CY7C1041G-10ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	
		CY7C1041GE-10ZSXI	51-85087	44-pin TSOP II, ERR output	
		CY7C1041GE-10ZSXIT	51-85087	44-pin TSOP II, ERR output, Tape and Reel	
CY7C1041GE-10VXI		51-85082	44-pin SOJ (400 Mils), ERR output		
CY7C1041GE-10VXIT		51-85082	44-pin SOJ (400 Mils), ERR output, Tape and Reel		
CY7C1041G-10VXI		51-85082	44-pin SOJ (400 Mils)		
CY7C1041G-10VXIT		51-85082	44-pin SOJ (400 Mils), Tape and Reel		
15	1.65 V–2.2 V	CY7C1041G18-15ZSXI	51-85087	44-pin TSOP II	
		CY7C1041G18-15ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	
		CY7C1041G18-15VXI	51-85082	44-pin SOJ (400 Mils)	
		CY7C1041G18-15VXIT	51-85082	44-pin SOJ (400 Mils), Tape and Reel	
		CY7C1041G18-15BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm)	
		CY7C1041G18-15BVXT	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), Tape and Reel	

Ordering Code Definitions

CY 7 C 1 04 1 G E XX - XX XX X I X



Package Diagrams

Figure 16. 44-pin TSOP II (Z44) Package Outline, 51-85087

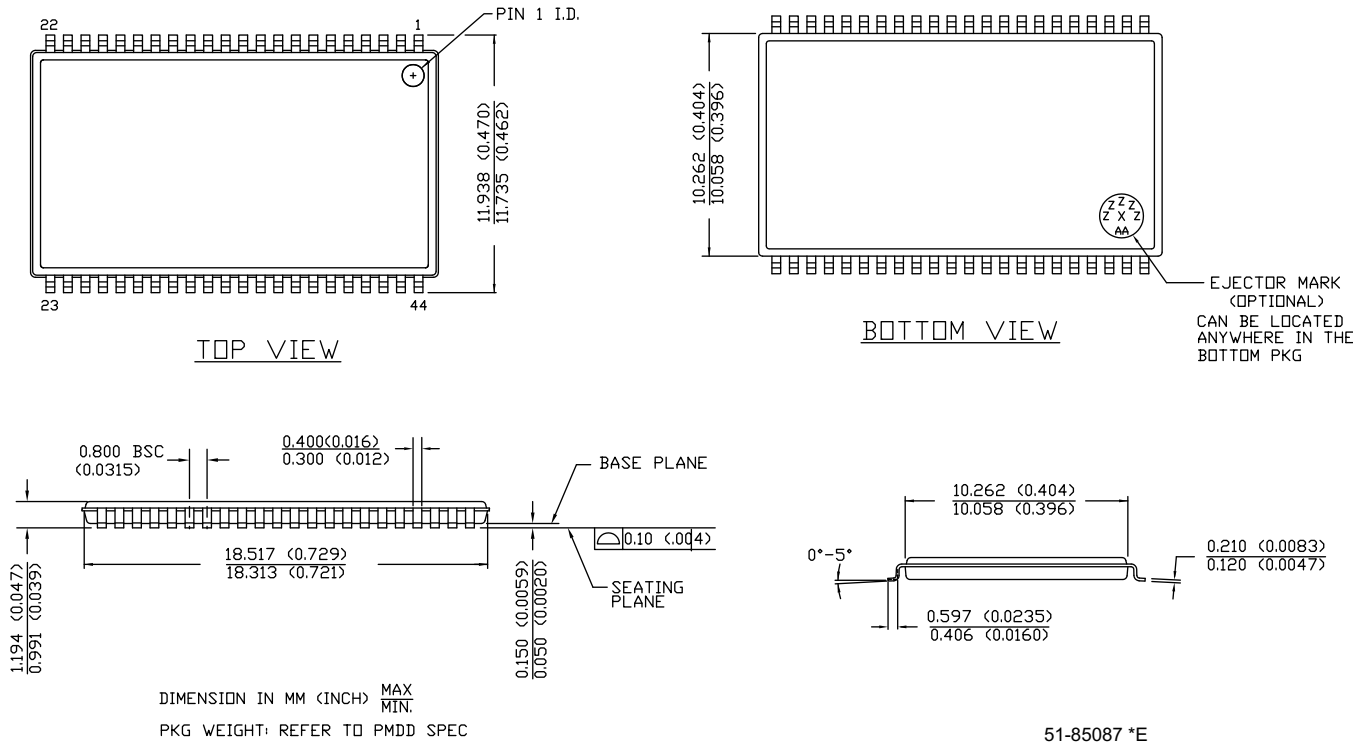
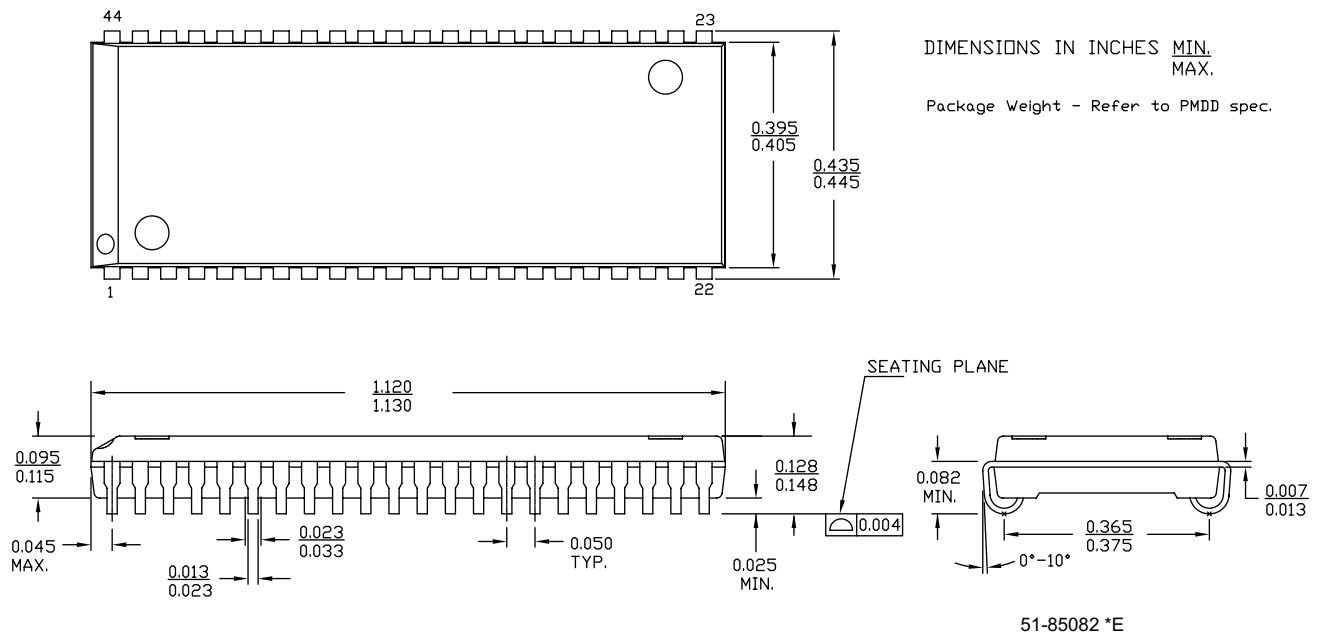
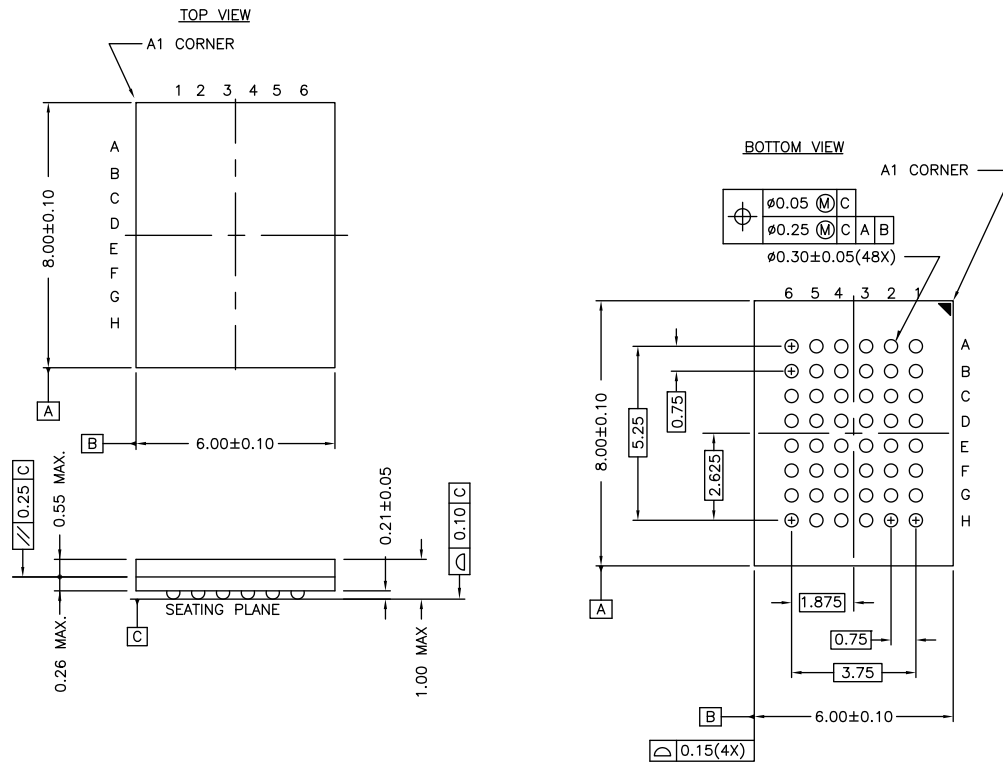


Figure 17. 44-pin SOJ (400 Mils) Package Outline, 51-85082



Package Diagrams (continued)

Figure 18. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{\text{BHE}}$	byte high enable
$\overline{\text{BLE}}$	byte low enable
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
$^{\circ}\text{C}$	Degrees Celsius
MHz	megahertz
μA	microamperes
μs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY7C1041G/CY7C1041GE, 4-Mbit (256K words × 16-bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-91368				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*F	4867081	NILE	07/31/2015	Changed status from Preliminary to Final.
*G	4876251	NILE	08/07/2015	Updated Ordering Information : Updated part numbers.
*H	4968879	NILE	10/16/2015	Fixed typo in bookmarks.
*I	5019226	VINI	11/18/2015	Updated Ordering Information : Updated part numbers.
*J	5122043	NILE	02/02/2016	Updated Truth Table .
*K	5223335	NILE	08/30/2016	Updated DC Electrical Characteristics : Removed values of V _{OH} parameter corresponding to “2.7 V to 3.6 V” range. Added values of V _{OH} parameter corresponding to “2.7 V to 3.0 V” and “3.0 V to 3.6 V” ranges. Updated Note 10 (Replaced “2 ns” with “20 ns”). Updated Ordering Information : Updated part numbers. Updated to new template.
*L	5655218	NILE	03/09/2017	Updated Logic Block Diagram – CY7C1041G (Updated diagram to change the devices from Dual Chip enabled to Single Chip enabled). Updated Logic Block Diagram – CY7C1041GE (Updated diagram to change the devices from Dual Chip enabled to Single Chip enabled). Updated to new template.
*M	5731242	GNKK	05/09/2017	Updated logo and copyright. Completing Sunset Review.
*N	6245720	NILE	07/13/2018	Updated Features : Added Note 2 and referred the same note in “Embedded ECC for single-bit error correction”. Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2014–2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.