ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE74LS280
Integrated Circuit
TTL – 9–Bit Odd/Even Parity Generator/Checker

Description:

The NTE74LS280 is a universal, monolithic, nine–bit parity generator/checker in a 14–Lead plastic DIP type package that utilizes Schottky–clamped TTL high–performance circuitry and features odd/even outputs to facilitate operation of either odd or even parity applications. The word–length capability is easily expanded by cascading.

This parity generator/checker offers the designer a trade–off between reduced power consumption and high performance and can be used to upgrade the performance of most systems utilizing the ’180 parity generator/checker. Although the NTE74LS280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at Pin4 and the absence of any internal connection at Pin3. This permits the NTE74LS280 to be substituted for the ’180 in existing designs to produce an identical function even if the ’LS280’s are mixed with the existing ’180’s.

Features:

- Generate Either Odd or Even Parity fo Nine Data Lines
- Cascadable for n–Bits
- Can Be Used to Upgrade Existing Systems using MSI Parity Circuits
- Data–to–Output Delay: 33ns (Typ)

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
Input Voltage, V_{IN} 7V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Voltage values are with respect to network ground terminal.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Input Voltage	V_{IH}	2	–	–	V
Low–Level Input Voltage	V_{IL}	–	–	0.8	V
High–Level Output Current	I_{OH}	–	–	–0.4	mA
Low–Level Output Current	I_{OL}	–	–	8	mA
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA		–	–	−1.5	V
High−Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = −0.4mA		2.7	3.4	–	V
Low−Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	–	0.25	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 7V		–	–	0.1	mA
High−Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V		–	–	20	μA
Low−Level Input Current	I_{IL}	V_{CC} = MAX, V_{IL} = 0.4V		–	–	−0.4	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4		−20	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5		–	16	27	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time, and the duration of the short−circuit should not exceed one second.

Note 5. I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From Data Input to Σ Even Output)	t_{PLH}	C_L = 15pF, R_L = 2kΩ, Inputs not under test at 0V	–	33	50	ns
	t_{PHL}		–	29	45	ns
Propagation Delay Time (From Data Input to Σ Odd Output)	t_{PLH}		–	23	35	ns
	t_{PHL}		–	31	50	ns

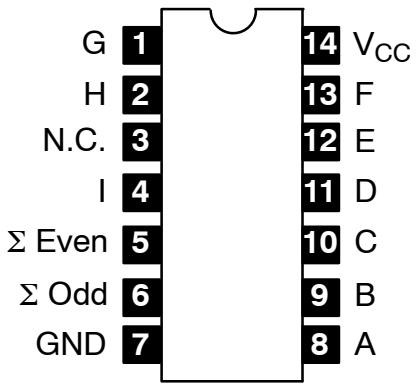
Function Table:

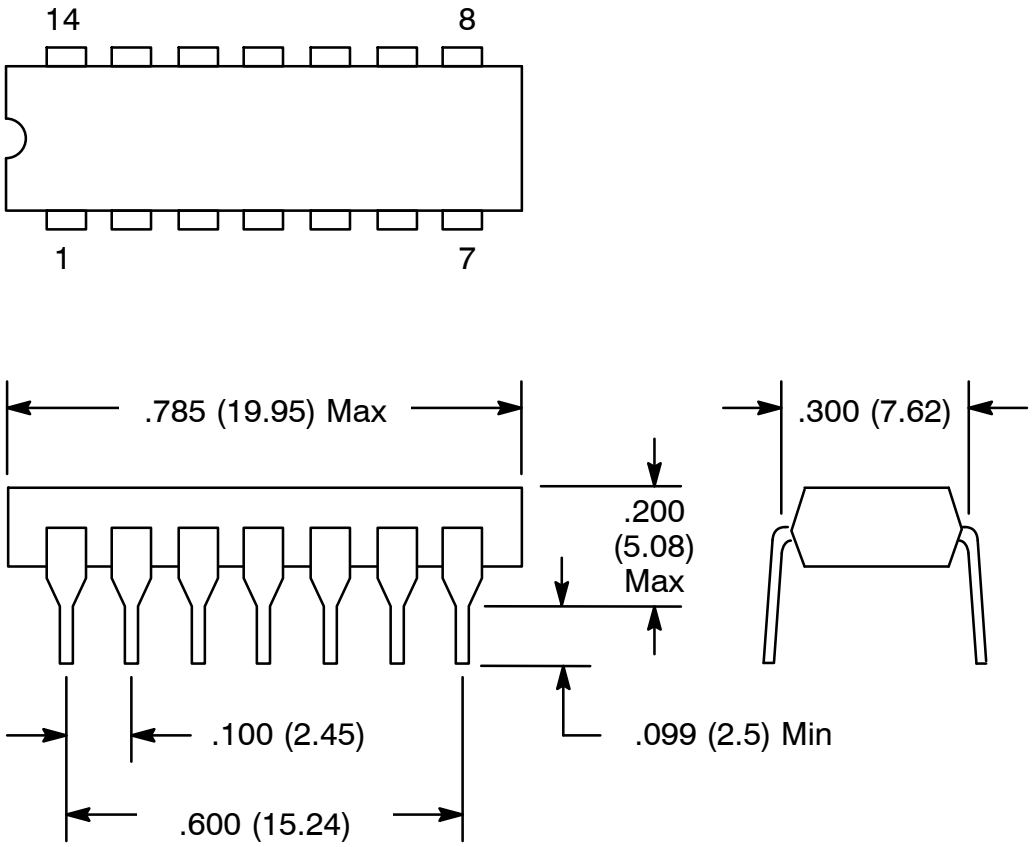
Number of Inputs A thru I That Are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = High Level

L = Low Level

Pin Connection Diagram




14
8
1
7
.785 (19.95) Max
.300 (7.62)
.200
(5.08)
Max
.100 (2.45)
.099 (2.5) Min
.600 (15.24)