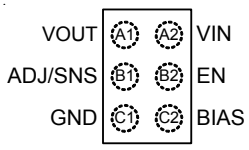
1A, 5.5V, Ultra Low Dropout Linear Regulator

General Description

The RT9085A is a high performance positive voltage regulator with separated bias voltage (V_{BIAS}), designed for applications requiring low input voltage and ultra low dropout voltage, output current up to 1A. The feature of ultra low dropout voltage is ideal for applications where output voltage is very close to input voltage. The input voltage can be as low as 0.8V and the output voltage is adjustable by an external resistive divider. The RT9085A features very low quiescent current consumption for portable applications. The device is available in the WL-CSP-6B 0.8x1.2 (BSC) package.

Pin Configuration

(TOP VIEW)



WL-CSP-6B 0.8x1.2 (BSC)

Features

- **Input Voltage Range : 0.8V to 5.5V**
- **Bias Voltage Range : 3V to 5.5V**
- **Adjustable Output Voltage Version, Output Voltage Range : 0.5V to 3V**
- **Ultra Low Dropout Voltage : 60mV at 1A**
- **Output Voltage Accuracy**
  - **± 1% Over Operating Ambient Temperature**
  - **± 0.5% @ 25°C**
- **Low Bias Input Current**
  - **Typ 35μA in Operating Mode**
  - **Typ 0.5μA in Disable Mode**
- **Output Active Discharge Function**
- **Enable Control**
- **Stable with a 10μF Output Ceramic Capacitor**
- **RoHS Compliant and Halogen/Pb Free**

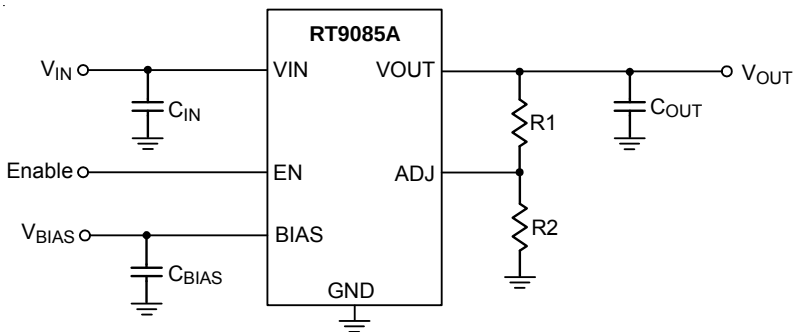
Applications

- Battery Powered Systems
- Portable Electronic Device
- Digital Set Top Boxes

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Simplified Application Circuit



Ordering Information

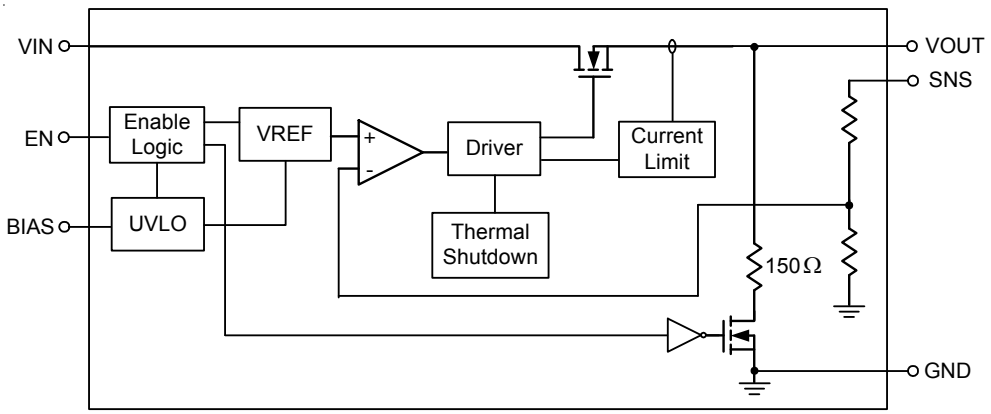
Product No.	Nominal Output Voltage	Package
RT9085A-07WSC	0.70V	WL-CSP-6B 0.8x1.2 (BSC)
RT9085A-0GWSC	0.75V	
RT9085A-08WSC	0.80V	
RT9085A-0HWSC	0.85V	
RT9085A-09WSC	0.90V	
RT9085A-0JWSC	0.95V	
RT9085A-10WSC	1.00V	
RT9085A-1KWSC	1.05V	
RT9085A-11WSC	1.10V	
RT9085A-1AWSC	1.15V	
RT9085A-12WSC	1.20V	
RT9085A-1BWSC	1.25V	
RT9085A-13WSC	1.30V	
RT9085A-15WSC	1.50V	
RT9085A-18WSC	1.80V	
RT9085AWSC	Adjustable	

Functional Pin Description

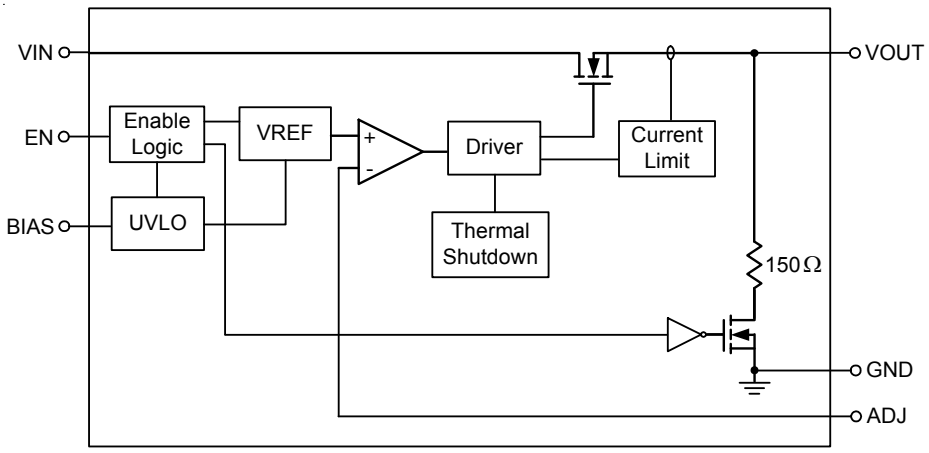
Pin No.	Pin Name	Pin Function
A1	VOUT	Regulated output voltage. A 10μF capacitor should be placed directly at this pin.
A2	VIN	Power input for the LDO.
B1	ADJ (ADJ devices)	Adjustable output voltage feedback input.
	SNS (Fix Vlot devices)	Output voltage sensing input, connect to the output terminal on the PCB.
B2	EN	Chip enable (Active-High). Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. This pin must not be left unconnected, connect to BIAS if not being used.
C1	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
C2	BIAS	Supply V_{BIAS} ripple should be less than 30mV (5mV/μs) to secure safe stabilization of internal control circuitry. Apply RC filter consists of (500 to 1k) Ω + 1μF at the pin input.

Functional Block Diagram

V_{OUT} Fixed Version



V_{OUT} Adjustable Version



Operation

The RT9085A is using N-MOSFET pass transistor for output voltage regulation from VIN voltage. The separated bias voltage (V_{BIAS}) power the low current internal control circuit for applications requiring low input voltage and ultra low dropout voltage.

In steady-state operation, the feedback voltage is regulated to the reference voltage by the internal regulator. When the feedback voltage signal is less than the reference, the output current passes through the power MOSFET will be increased. The extra amount of the current is sent to the output until the voltage level of ADJ pin returns to the reference. On the other hand, if the feedback voltage is higher than the reference, the power MOSFET current is decreased. The excess charge at the output can be released by the loading current.

Over-Temperature Protection (OTP)

The RT9085A has an over-temperature protection. When the device triggers the OTP, the device shuts down until the temperature back to normal state.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 6V
- All Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-6B 0.8x1.2 (BSC) ---------- 0.67W
- Package Thermal Resistance (Note 2)
  WL-CSP-6B 0.8x1.2 (BSC), θ_{JA} ---------- 148°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 0.8V to 5.5V
- Supply Input Voltage, BIAS ---------- 3V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{BIAS} = 3V, or (V_{OUT} + 1.6V), whichever is greater, V_{IN} = $V_{OUT(Normal)}$ + 0.3V, I_{OUT} = 1mA, V_{EN} = 1V, C_{IN} = 10µF, C_{OUT} = 10µF, C_{BIAS} = 1µF, T_A = 25°C, unless otherwise specified). (Note 6)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Input Voltage Range	V_{IN}		V_{OUT} + V_{DROP}	--	5.5	V
Operating Bias Voltage Range	V_{BIAS}		(V_{OUT} + 1.2) ≥ 3	--	5.5	V
Under-Voltage Lockout	V_{UVLO}	V_{BIAS} rising	--	1.6	--	V
		Hysteresis	--	0.2	--	V
Reference Voltage (Adj devices only)	V_{REF}		0.49	0.5	0.51	V
Output Voltage Accuracy	V_{OUT}	(Note 5)	–0.5	--	0.5	%
Output Voltage Accuracy (Note 5)	V_{OUT}	$V_{OUT(Normal)}$ + 0.3V ≤ V_{IN} ≤ $V_{OUT(Normal)}$ + 1V, 3V or ($V_{OUT(Normal)}$ + 1.2V), whichever is greater < V_{BIAS} < 5.5V, 1mA < I_{OUT} < 1A	–1	--	1	%
V_{IN} Line Regulation	ΔV_{LINE_VIN}	$V_{OUT(NOM)}$ + 0.3V ≤ V_{IN} ≤ 5V	--	0.01	--	%/V
V_{BIAS} Line Regulation	ΔV_{BIAS_VIN}	3V or ($V_{OUT(Normal)}$ + 1.2V), whichever is greater < V_{BIAS} < 5.5V	--	0.01	--	%/V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Load Regulation		ΔV_{LOAD}	I_{OUT} = 1mA to 1A	--	2	--	mV
V_{IN} Dropout Voltage		V_{DROP_VIN}	I_{OUT} = 1A (Note 9)	--	60	75	mV
V_{BIAS} Dropout Voltage		V_{DROP_BIAS}	I_{OUT} = 1A, V_{IN} = V_{BIAS} (Note 7, Note 8)	--	1.05	1.5V	V
Output Current Limit		I_{LIM}	V_{OUT} = 90% $V_{OUT(Normal)}$	--	2000	--	mA
ADJ Pin Operating Current (ADJ devices only)		I_{ADJ}		--	0.1	0.5	μA
Bias Pin Quiescent Current		I_{BIAS}	V_{BIAS} = 3V	--	35	50	μA
Bias Pin Shutdown Current		$I_{BIAS(DIS)}$	$V_{EN} \leq$ 0.4 V	--	0.5	1	μA
V_{IN} Pin Shutdown Current		$I_{VIN(DIS)}$	$V_{EN} \leq$ 0.4 V	--	0.5	1	μA
EN Input Voltage	Logic_High	V_{IH}		0.9	--	--	V
	Logic_Low	V_{IL}		--	--	0.4	
EN Pull Down Current		I_{EN}	V_{EN} = 5.5V, V_{BIAS} = 5.5V	--	0.3	--	μA
Turn-On Time		t_{ON}	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$. $V_{OUT(NOM)}$ = 1V	--	150	--	μs
Power Supply Rejection Ratio (Note 10)		PSRR_V_{IN}	V_{IN} to V_{OUT}, f = 1kHz, I_{OUT} = 150mA, VIN $\geq$ V_{OUT} + 0.5V	--	70	--	dB
		PSRR_V_{BIAS}	V_{BIAS} to V_{OUT}, f = 1kHz, I_{OUT} = 150mA, $V_{IN} \geq V_{OUT}$ + 0.5V	--	70	--	dB
Output Noise Voltage (Fixed Volt.) (Note 10)		e_{NO_FIXED}	V_{IN} = V_{OUT} +0.5 V, $V_{OUT(NOM)}$ = 1V, f = 10Hz to 100kHz	--	60	--	μV_{RMS}
Output Noise Voltage (Adj devices) (Note 10)		e_{NO_ADJ}	V_{IN} = V_{OUT} + 0.5V, f = 10Hz to 100kHz	--	30 x V_{OUT}/ V_{REF}	--	μV_{RMS}
Thermal Shutdown Threshold		T_{SD}	Shutdown temperature	--	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C
Output Discharge Pull- Down		R_{DISCH}	$V_{EN} \leq$ 0.4V, V_{OUT} = 0.5V	--	150	--	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Adjustable devices tested at 0.5V; external resistor tolerance is not taken into account.

Note 6. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.

Note 7. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(Normal)}$.

Note 8. For output voltages below 0.9V, V_{BIAS} dropout voltage does not apply due to a minimum Bias operating voltage of 3V.

Note 9. For adjustable devices, VIN dropout voltage tested at $V_{OUT(NOM)}$ = 2 x V_{REF}.

Note 10. Guaranteed by design.

Typical Application Circuit

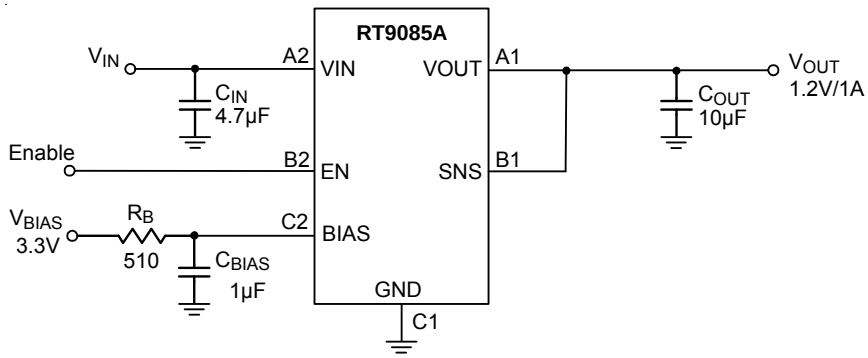


Figure 1. Fixed Voltage Regulator

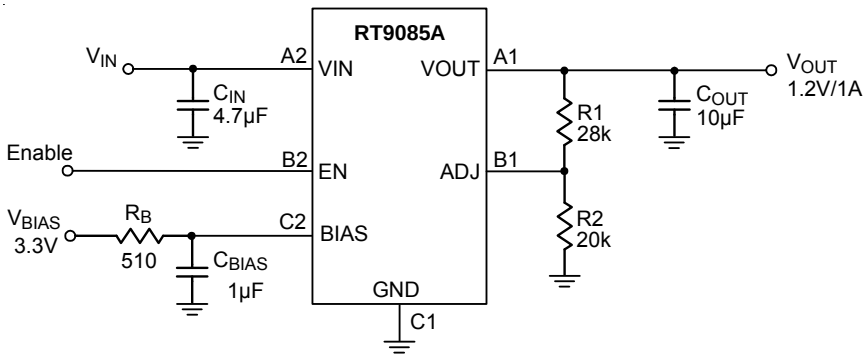
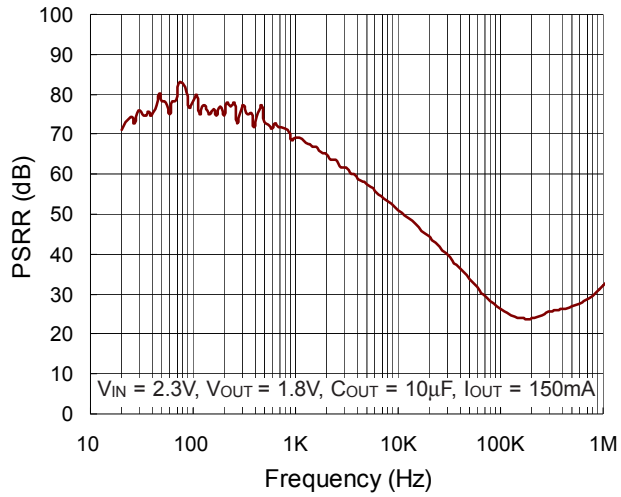


Figure 2. Adjustable Voltage Regulator

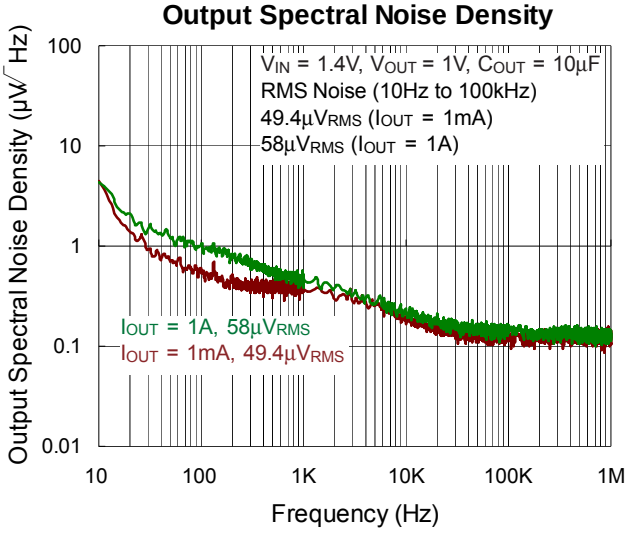
Note : All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC Bias.

Typical Operating Characteristics

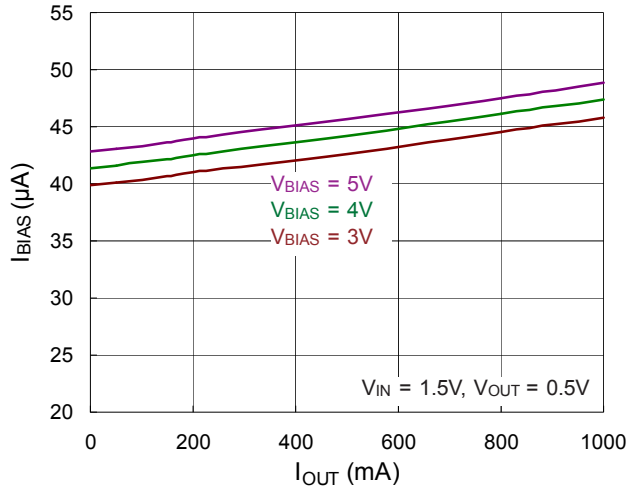
PSRR vs. Frequency



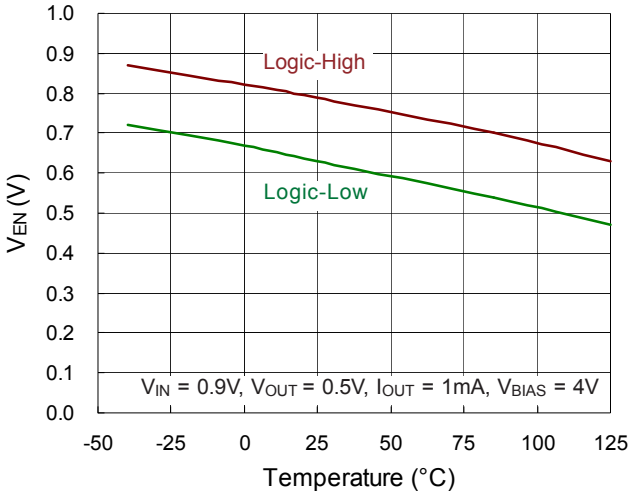
Output Spectral Noise Density



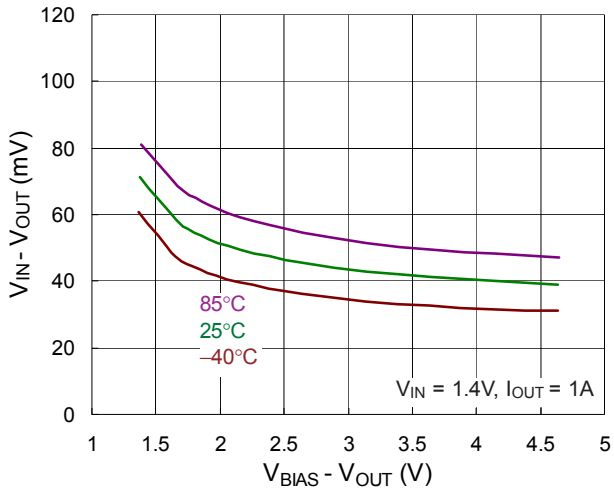
BIAS pin Quiescent Current vs. Output Current



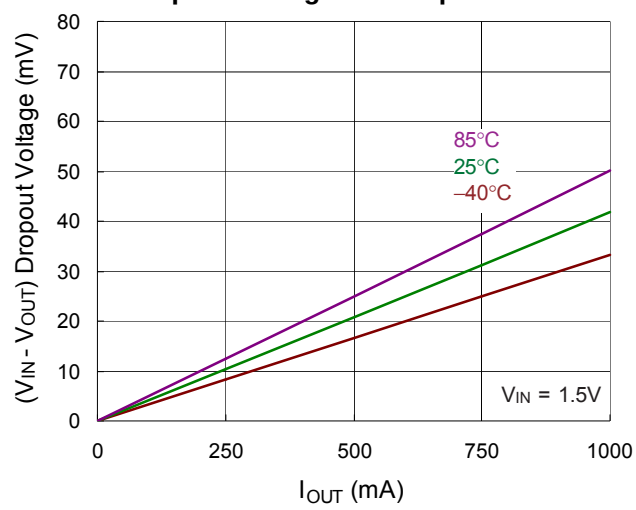
Enable Voltage Threshold vs. Temperature



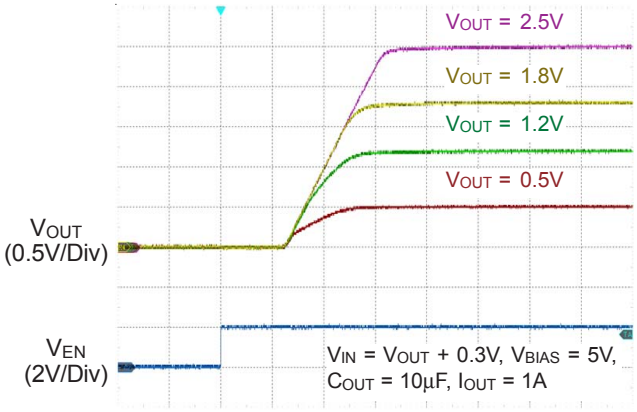
VIN Dropout Voltage vs. (VBIAS - VOUT)



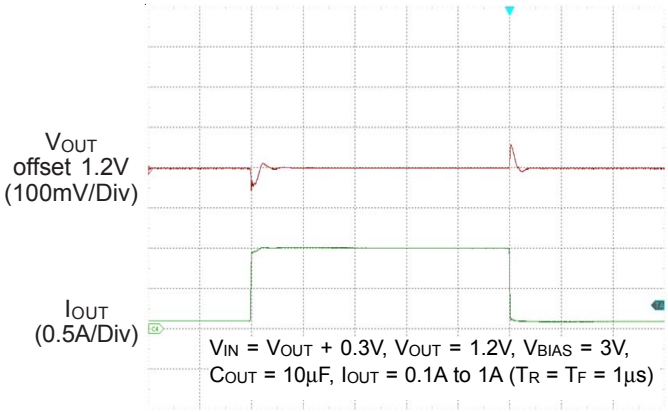
Dropout Voltage vs. Output Current



V_{OUT} Start Up with EN



Load Transient Response



Application Information

The RT9085A is a low voltage, low dropout linear regulator with input voltage V_{IN} from 0.8V to 5.5V, V_{BIAS} from 3V to 5.5V and adjusted output voltage from 0.5V to (V_{IN} – V_{DROP}).

Output Voltage Setting

For the RT9085A, the voltage on the ADJ pin sets the output voltage and is determined by the values of R1 and R2. The values of R1 and R2 can be calculated for any voltage using the formula given in Equation :

$$V_{OUT} = 0.5V \times \left(\frac{R1 + R2}{R2} \right)$$

Using lower values for R1 and R2 is recommended to reduces the noise injected from the ADJ pin. Note that R1 is connected from VOUT pin to ADJ pin, and R2 is connected from ADJ to GND.

Dropout Voltage

There are two power supply inputs V_{IN} and V_{BIAS} and only one output V_{OUT} for the RT9085A, the Dropout voltage with these two different input also have different definition. VIN Dropout voltage is the voltage difference between VIN and VOUT when V_{OUT} starts to decrease while reduce V_{IN} level (for this condition, VBIAS needs high enough as specific value published in Electrical Characteristics table). VBIAS dropout voltage is the voltage difference between V_{BIAS} and V_{OUT} while VIN and BIAS pins are connected together and V_{OUT} starts to decrease.

C_{IN} and C_{OUT} Selection

The RT9085A is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with effective capacitance range from 4.7μF to 22μF on the RT9085A output ensures stability. The input capacitor must be located at a distance of no more than 0.5 inch from the input pin of the chip. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it will provide better PSRR and line transient response. Any good quality ceramic capacitor can be used, C_{IN} = 4.7μF and C_{BIAS} = 0.1μF or greater are recommended.

Chip Enable Operation

The RT9085A goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and band gap are all turned off reducing the supply current to only 1μA (max.).

Consideration should be taken in the power on sequence, it is mandatory to ensure V_{BIAS} > V_{OUT} + 1.6V before both V_{EN} > V_{IH} and V_{IN} > V_{OUT} + 0.1V. The BIAS pin supplies voltage for the LDO control circuit, and powering up V_{BIAS} first will ensure turn on time (t_{ON}) and output voltage accuracy (V_{OUT}) to follow datasheet spec.

Figure 3 also shows the use of an RC-delay circuit that hold off V_{EN} until V_{BIAS} has ramped up to target value. This technique can also be used to drive EN from VIN. An external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.

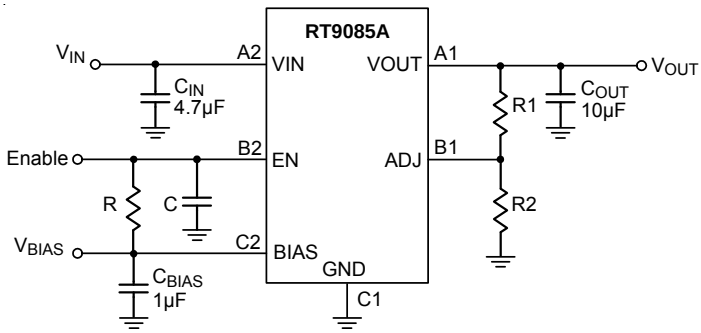


Figure 3. Soft-Start Delay Using an RC Circuit to Enable the Device

Current Limit

The RT9085A continuously monitors the output current to protect the pass transistor against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the pass transistor's gate voltage to limit the output within the predefined range.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC

package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-6B 0.8x1.2 (BSC) package, the thermal resistance, θ_{JA}, is 148°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (148°C/W) = 0.67W for a WL-CSP-6B 0.8x1.2 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

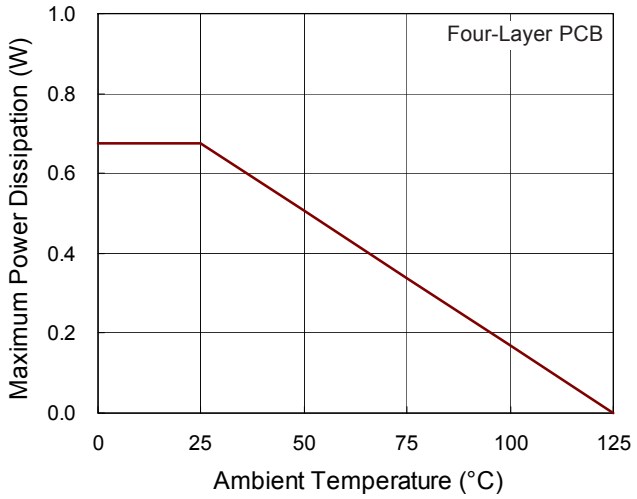
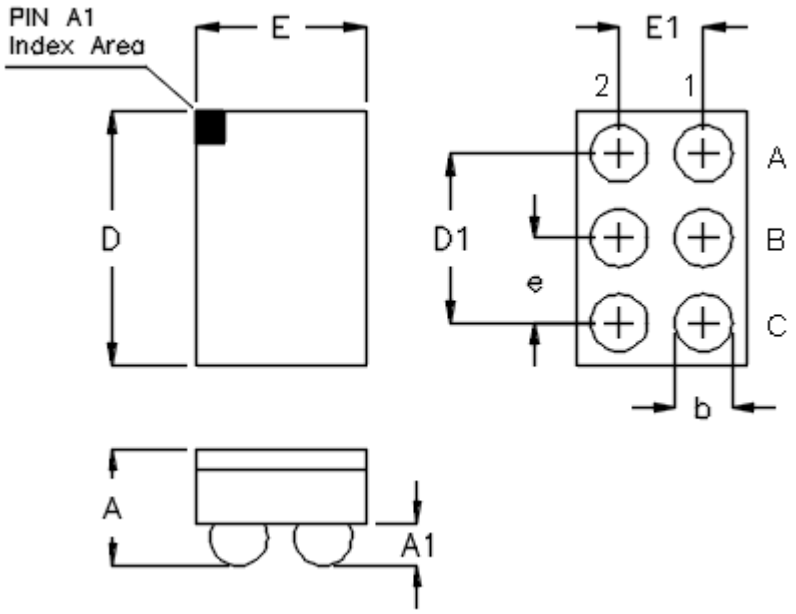


Figure 4. Derating Curve of Maximum Power Dissipation

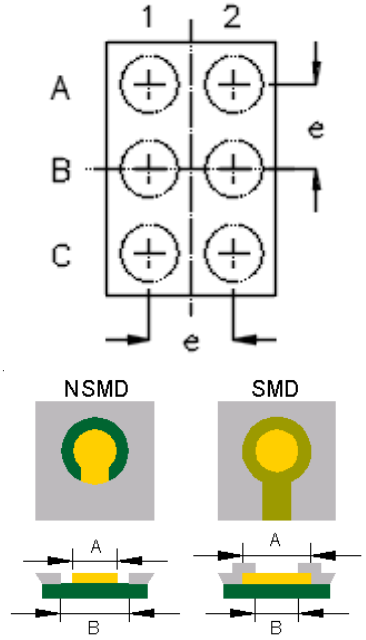
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.160	1.240	0.046	0.049
D1	0.800		0.031	
E	0.760	0.840	0.030	0.033
E1	0.400		0.016	
e	0.400		0.016	

6B WL-CSP 0.8x1.2 Package (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP0.8*1.2-6(BSC)	6	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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