life.augmented

PRODUCT / PROCESS CHANGE NOTIFICATION

ST Shenzhen (China) Assy & Test line upgrade for Industrial plus 105°C EEPROM products in SO8N

105°C EEPROM products in SO8N are widely used in high volume at all customers and in all applications. To maintain high level of service and to support high volume production on the long-term, ST has decided to switch Assembly & Test from High Density (HD) strip test line to **Super High Density (SHD)** strip test line. Both lines are installed in ST Shenzhen (China). SHD strip test line already produces very high-volume of EEPROM SO8N products for industrial market since year 2012.

What is the change?

Assembly & Test of 105°C EEPROM in SO8N package at ST Shenzhen (China) are upgraded from High Density (HD) strip test line to **Super High Density (SHD) strip test line.**

SHD Assembly line runs with higher parallelism and same assembly flow as current HD line. As continuous improvement, a step of plasma cleaning has been introduced between die attach and wire bonding.
A rationalization of the leadframe dimensions has been done.

SHD strip test line runs with higher parallelism and same test flow and test sequence as current HD line. SHD strip test line runs with same test equipment as current HD line.

See appendix B for more details on assembly and test flow.

Why?

The strategy of the STMicroelectronics Memory division is to support our customers on product and service quality on a long-term basis. In line with this commitment, this change will secure long term availability and 105°C SO8N capacity while improving product manufacturing quality.

When?

Shipments will start from **Week 01** / 2023.

Production of 105°C EEPROM SO8N on current HD strip test line will continue until end of June 2023 giving the time to ramp-up gradually the SHD line.

From June 2023, 105°C EEPROM SO8N products will be produced only on SHD line.

How will the change be qualified?

This change has been qualified using the standard STMicroelectronics Corporate Procedures for Quality and Reliability.

Qualification report RERMMY2005 for Assembly is available and included inside this document.
Qualification report TERMMY2005-2 for Test (I2C/SPI) is forecasted for Week 26 / 2022.

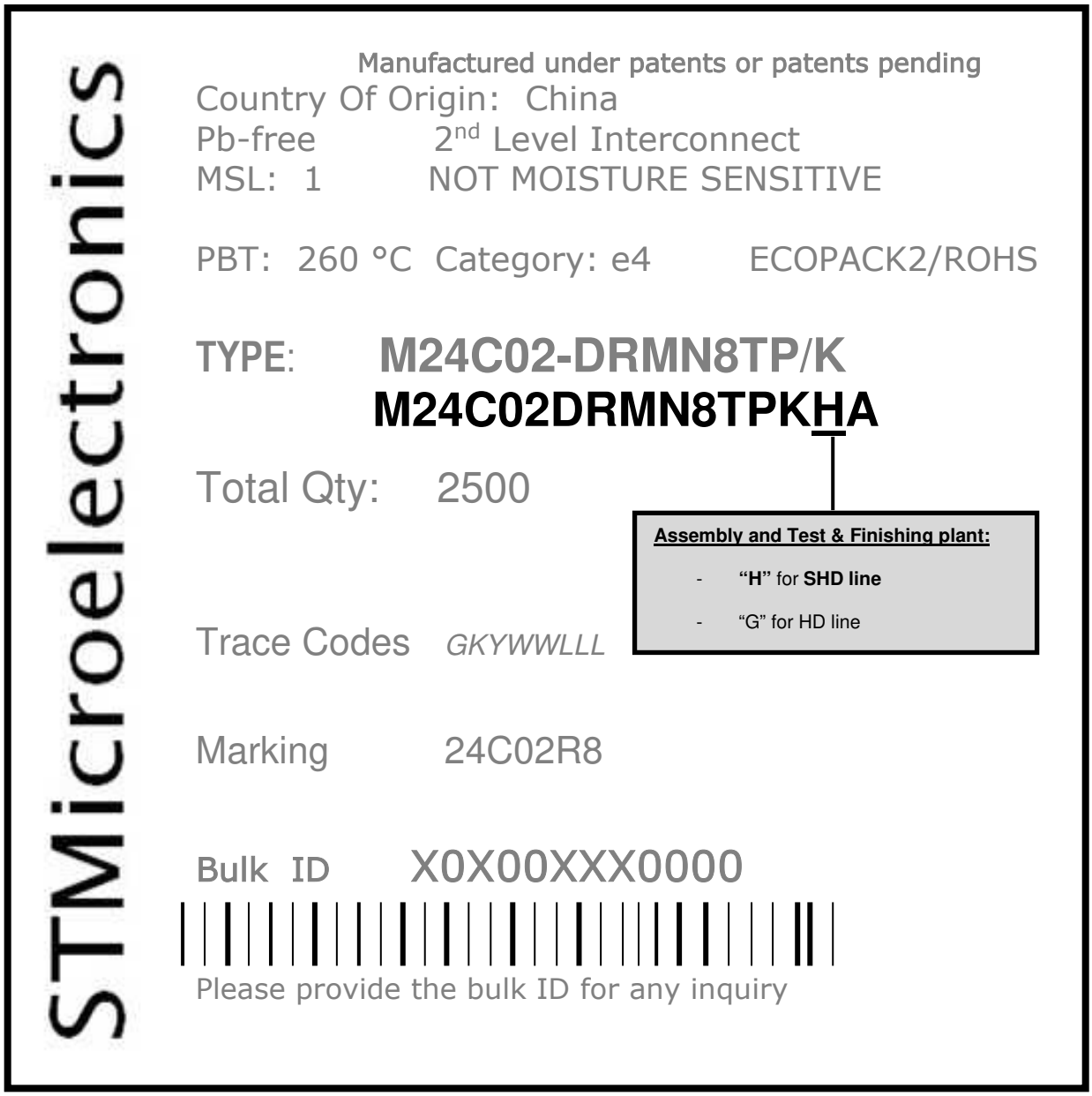
What is the impact of the change?

- **Form:** visual on package top side / backside
- **Fit:** no change
- **Function:** no change

How can the change be seen?

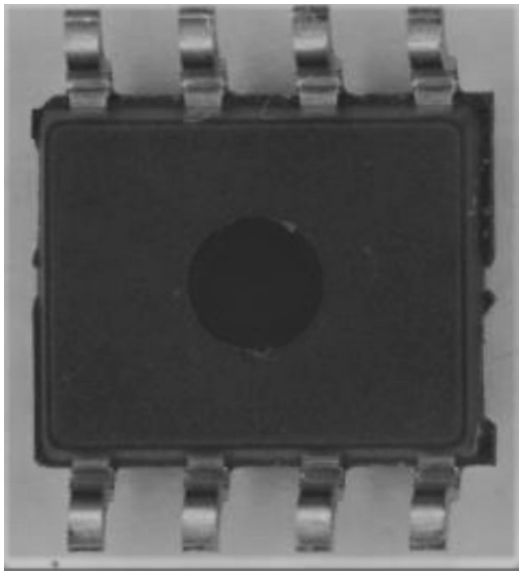
- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number** where the "**Assembly and Test & Finishing plants"** identifier is "**H**" for products **assembled & tested on SHD line**, this digit being "G" for current products assembled & tested on HD line.

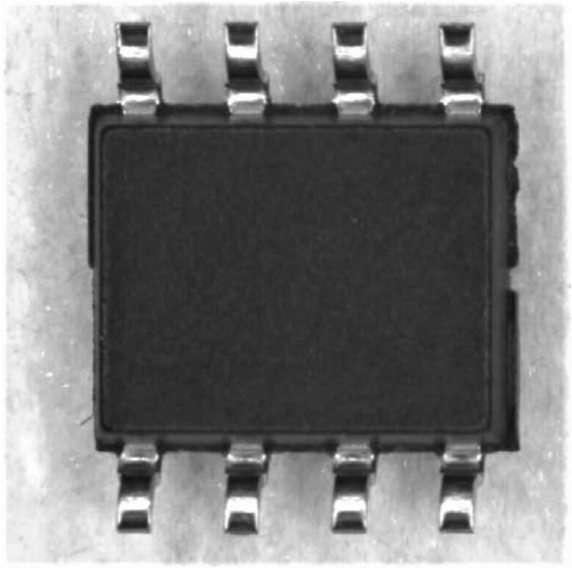


- ***PACKAGE VISUAL***

A visual difference can be observed at bottom side: the **package of the SHD line** is showing a **dot at the center** while no dot at bottom side on the package of the HD line:



Package of SHD line



Package of HD line

Bottom side views

Marking readability improvement:

Package of SHD line

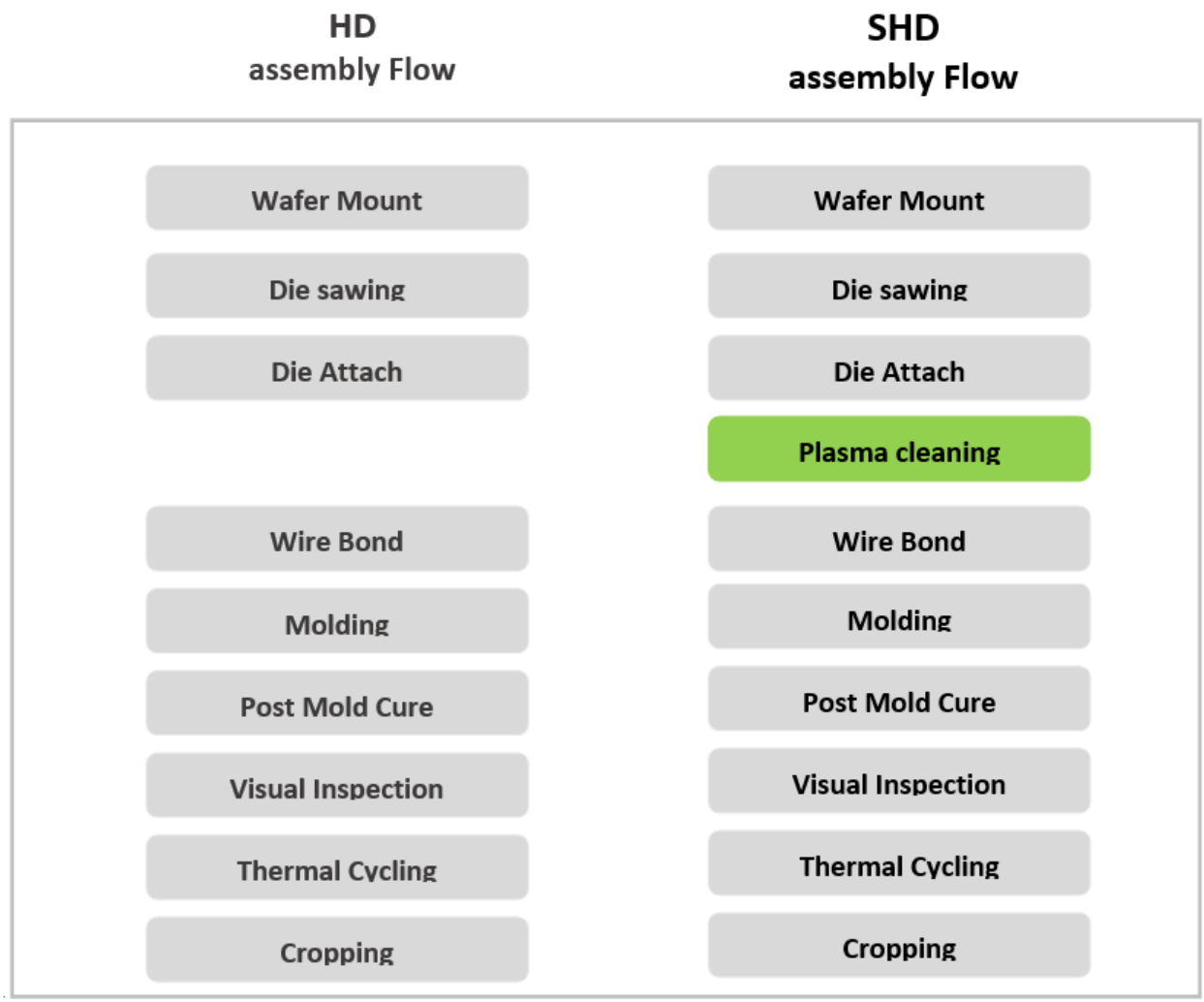
Package of HD line

Top side views

Appendix A- Product Change Information

Product family / Commercial products:	105°C EEPROM products in SO8N
Customer(s):	All
Type of change:	Upgrade Assembly & Test line
Reason for the change:	Upgrade to SHD line
Description of the change:	ST Shenzhen (China) Assembly & Test lines switch from high density (HD) to super high density (SHD).
Forecast date of the change: (Notification to customer)	Week 13 / 2022
Forecast date of Qualification samples availability for customer(s):	Week 26 as per defined in appendix C
Qualification Report availability:	RERMMY2005 for Assembly: Available, see appendix D TERMMY2005-2 for Test: Week 26 / 2022
Marking to identify the changed product:	No change on top marking
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Estimated date of first shipment:	Week 01 / 2023

Appendix B: HD / SHD flows comparison:



Assembly flow comparison

Strip	HD Test line	SHD Test line
Size	32 x 8	**36 x 12**
Unit Qty / strip	256	**432**
Tester	Magnum-sv	Magnum-sv
Handler	MCT-tri-temp MCT SH5000	MCT-tri-temp MCT SH5000
Test parallelism	128	**144**

Test equipement comparison

Appendix C: concerned Commercial Part Numbers:

Commercial product	Samples availability
M24128-DRMN8TP/K	Week 26 / 2022
M24256-DRMN8TP/K	
M24512-DRMN8TP/K	
M24C02-DRMN8TP/K	
M24C04-DRMN8TP/K	
M24C08-DRMN8TP/K	
M24C16-DRMN8TP/K	
M24C32-DRMN8TP/K	
M24C64-DRMN8TP/K	
M93C56-RMN8TP/K	
M95040-DRMN8TP/K	
M95128-DRMN8TP/K	
M95512-DRMN8TP/K	
M95640-DRMN8TP/K	
M95080-DRMN8TP/K	
M95160-DRMN8TP/K	
M95320-DRMN8TP/K	
M95256-DRMN8TP/K	

Appendix D: RERMMY2005:

Reliability Evaluation Report

RERMMY2005

SO8 Narrow SHD Shenzhen assembly line qualification on EEPROM memory products using CMOSF8H technology

Reliability Evaluation Purpose (New product qualification)

General Information	
Commercial Product	See appendix 1
Product Line	Super High Density Line, Automotive
Product Description	EEPROM I²C, SPI, Microwire families, Automotive products
Package	S8On
Silicon Technology	CMOSF8H
Division	MDG / MMY - Memory

Traceability	
Diffusion Plant	ST Rousset, France
Assembly Plant	ST Shenzhen, China

Reliability Assessment	
Pass	☒
Fail	☐

Release	Date	Author	Function
Rev 01	January 24th, 2022	L.BREMOND	Division Back End Quality & Reliability Engineer

DOCUMENT APPROVERS:

Name	Function	Location	Date
R. Pavano	Division Quality & Reliability Manager	Rousset, France	January 24th, 2022

This report is a summary of the reliability trials performed in good faith by STMicroelectronics. This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics General Terms and Conditions of Sale.

RELIABILITY EVALUATION OVERVIEW

- **OBJECTIVE**

This reliability report summarizes the results of the reliability trials that were performed to qualify AEC_Q100 Rev H automotive grade 0, the SO8 Narrow Super High Density (SHD) assembly line at Shenzhen Back End manufacturing plant for EEPROM memory products using CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

- **CONCLUSION**

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

Based on the overall results obtained, the new products list above manufactured in the ST Rousset 8”, France (Diffusion plant) and assembled in ST Shenzhen, China (Assembly plant), has positively passed reliability evaluation performed in agreement to AEC_Q100 Rev H specification Grade 0.

TABLE OF CONTENTS

1. RELIABILITY STRATEGY

Package reliability run on 4 test vehicles, assembled in final SO8n package on SHD Line.
They were defined in order to evaluate the performance of all lead frame dimensions used for the EEPROM familly on SHD Line :

- 60 x 60 mils²
- 75 x 75 mils²
- 95 x 130 mils²
- 98 x 150 mils²

The CMOSF8H technology is also qualified for automotive grade 0 using M95640-A145 as driver product.

Reliability trials performed as part of this reliability evaluation are in agreement with **ST 0061692** specification and **AEC_Q100 Rev H** (cf AEC_Q100 Table 3 “Process Change Qualification Guidelines for the Selection of Tests”, new package change).

2. PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1. Generalities

Details of product test vehicles and associated qualified products are listed in appendix 1.

2.2. Reliability testing information

Table 1

Reliability Testing Information	
Reliability laboratory name / location	RSST-Rousset MDG Reliability Laboratory / Rousset, France SGTP-Asia MDG Reliability Laboratory / Toa Payoh, Singapore STS- Shenzhen Laboratory / Shenzhen, China GRAL-Grenoble Reliability Laboratory / Grenoble, France

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3. TEST RESULTS SUMMARY

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicles used for the die and package qualification are presented in Table 2.

Table 2

Test vehicles	Silicon process technology	Wafer fabrication location	Assembly plant location	Package description	Die paddle dimension (mils²)	Lot ID
M24C02-DRMN3TP/K	CMOSF8H	ST Rousset 8”	ST Shenzhen Back End plant, China	SO8n	60 x 60	Lot 1
M95256-DRMN3TP/K					75 x 75	Lot 2
M95512-DRMN3TP/K					95 x 130	Lot 3
M95M02-DWMN3TP/K					98 x 150	Lot 4

3.1. Test results summary (AEC_Q100 Rev H)

For Automotive ICs, test plan results are summarized in AEC-Q100 rev.H template.
Electrical Testing Temperature and Physical Analysis required by AEC-Q100 (**in bold**) and any additional STM requirements are also reported in tables below in Test Conditions column.
Test method revision reference is the one active at the date of reliability trial execution.

Table 3 – ***TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS***

Test	#	Reference	Test Conditions	Lots Qty	Sample Size / Lot	Total	Results / Lot Fail / Sample Size	Comments (N/A = Not Applicable)
PC	A1	JESD22-A113 J-STD-020	24h bake@125 °C, MSL1 (168h@85 °C / 85% RH) 3x IReflow Peak temperature at 260°C + TC -65 °C / +150 °C, 100 cycles	4	1262	5048	Lot 1 : 0 / 1262 Lot 2 : 0 / 1262 Lot 3 : 0 / 1262 Lot 4 : 0 / 1262	-
				Performed before THB / HAST / HTSL / UHAST / TC / ELFR / HTOL				
THB	A2	JESD22-A101	Ta = 85 °C, 85% RH, bias 5v6 Duration = 2000hrs ☒ **After PC** ☒ **Testing at Room** ☒ **Testing at Hot**	4	77	308	Lot 1 : 0 / 77 Lot 2 : 0 / 77 Lot 3 : 0 / 77 Lot 4 : 0 / 77	
HAST	A2	JESD22-A110	Ta = 130 °C, 85% RH, 230 kPa, bias 5.6 V Duration = 96hrs ☒ **After PC** ☒ **Testing at Room** ☒ **Testing at Hot**	4	77	308	Lot 1 : 0 / 77 Lot 2 : 0 / 77 Lot 3 : 0 / 77 Lot 4 : 0 / 77	
UHAST	A3	JESD22-A118	Ta = 130 °C, 85% RH, 230 kPa, no bias Duration = 96hrs ☒ **After PC** ☒ **Testing at Room**	4	77	308	Lot 1 : 0 / 77 Lot 2 : 0 / 77 Lot 3 : 0 / 77 Lot 4 : 0 / 77	
TC	A4	JESD22 A104	Ta = -65 °C /+150 °C Duration = 2000 cycles ☒ **After PC** ☒ **Testing at Room** ☒ **Testing at Hot** ☒ **WBP after TC**	4	77	308	Lot 1 : 0 / 77 Lot 2 : 0 / 77 Lot 3 : 0 / 77 Lot 4 : 0 / 77	After completion of TC, WBP successfully performed on minimum five devices from one lot
HTSL	A6	JESD22 A103	Ta = 150 ºC Duration = 2000hrs ☒ **After PC** ☒ **Testing at Room** ☒ **Testing at Hot**	4	77	308	Lot 1 : 0 / 77 Lot 2 : 0 / 77 Lot 3 : 0 / 77 Lot 4 : 0 / 77	

Table 4 – ***TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS***

Test	#	Reference	Test Conditions	Lots Qty	Sample Size / Lot	Total	Results / Lot Fail/Sample Size	Comments (N/A = Not Applicable)
HTOL	B1	AEC-Q100-008	HTOL 150 °C, 6V Duration = 2000hrs **☒ After PC** **☒ Testing at Room** **☒ Testing at Cold** **☒ Testing at Hot**	4	77	308	Lot 1 : 0 / 77 Lot 2 : 0 / 77 Lot 3 : 0 / 77 Lot 4 : 0 / 77	
ELFR	B2	AEC-Q100-008	HTOL 150 °C, 6V Duration = 48hrs **☒ After PC** **☒ Testing at Room** **☒ Testing at Hot**	4	800	2400	Lot 1 : 0 / 800 Lot 2 : 0 / 800 Lot 3 : 0 / 800 Lot 4 : 0 / 800	

Table 5 – ***TEST GROUP E – ELECTRICAL VERIFICATION***

Test	#	Reference	Test Conditions	Lots Qty	Sample Size / Lot	Total	Results / Lot Fail/Sample Size	Comments (N/A = Not Applicable)
ESD HBM	E2	AEC-Q100-002	Target HBM = +/- 4kV **☒ Testing at Room** **☒ Testing at Hot**	1	See test method (3 parts / voltage)		Lot 1 : > 4000V Lot 2 : W10 Lot 3 : W10 Lot 4 : W10	Class 3A
ESD CDM	E3	AEC-Q100-011	Target CDM = +/-750V on corner pins; +/- 500V all others Field induced charging method **☒ Testing at Room** **☒ Testing at Hot**	4	See test method (3 parts / voltage)		Lot 1 : > 1500V Lot 2 : > 1500V Lot 3 : > 1500V Lot 4 : > 1500V	Class C3

4. APPENDIX

4.1. APPENDIX 1: Details of product test vehicles and qualified products

Qualified products	Test vehicles	Die paddle dimension (mils²)	Lot ID
M24C02-DRMN3TP/K M24C02-DRMN8TP/K M24C04-DRMN3TP/K M24C04-DRMN8TP/K M24C08-DRMN3TP/K M24C08-DRMN8TP/K M24C16-DRMN3TP/K M24C16-DRMN8TP/K M24C32-DRMN3TP/K M24C32-DRMN8TP/K M24C64-DRMN3TP/K M24C64-DRMN8TP/K M93C46-RMN3TP/K M93C56-RMN3TP/K M93C56-RMN8TP/K M93C66-RMN3TP/K M93C76-RMN3TP/K M93C86-RMN3TP/K M95020-DRMN3TP/K M95040-DRMN3TP/K M95040-DRMN8TP/K M95080DRMN3T/KM3 M95080-DRMN3TP/K M95160DRMN3T/KM3 M95160-DRMN3TP/K M95320DRMN3T/KM3 M95320-DRMN3TP/K M95640DRMN3T/KM3 M95640-DRMN3TP/K M95640-DRMN8TP/K M93C66RMN3TP/KM3 M95080-DRMN8TP/K M95160-DRMN8TP/K M95320-DRMN8TP/K	M24C02-DRMN3TP/K	60 x 60	Lot 1
M24128-DRMN3TP/K M24128-DRMN8TP/K M24256-DRMN3TP/K M24256-DRMN8TP/K M35S128-WMN3TP/K M35S160-WMN3TP/K M95128DRMN3T/KM3 M95128-DRMN3TP/K M95128-DRMN8TP/K M95256DRMN3T/KM3 M95256-DRMN3TP/K M95256-DRMN8TP/K	M95256-DRMN3TP/K	75 x 75	Lot 2
M24512-DRMN3TP/K M24512-DRMN8TP/K M24M01-DWMN3TP/K M95512DRMN3T/KM3 M95512-DRMN3TP/K M95512-DRMN8TP/K M95M01-DWMN3TP/K	M95512-DRMN3TP/K	95 x 130	Lot 3
M24M02-DWMN3TP/K M95M02-DWMN3TP/K	M95M02-DWMN3TP/K	98 x 150	Lot 4

5. APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
AEC-Q100	Failure Mechanism Based Stress Test Qualification for Integrated Circuits in automotive applications
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
DMS 0061692	Reliability Tests and Criteria for Product Qualification
JESD22-A101	Steady state temperature humidity bias life test
JESD22-A103	High temperature storage life
JESD22-A104	Temperature cycling
JESD22-A108	Temperature, bias, and operating life
JESD22-A110	Highly accelerated stress test
JESD22-A113	Preconditioning of nonhermetic surface mount devices prior to reliability testing
JESD22-A115	Electrostatic discharge (ESD) sensitivity testing machine model (MM)
JESD22-A118	Unbiased highly accelerated stress test
JESD22-B100	Physical Dimension
JESD22-B102	Solderability
JESD22-B108	Coplanarity Test for Surface-Mount Semiconductor Devices
J-STD-020	Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

6. GLOSSARY

CDM	Electrostatic Discharge – Charged Device Model
ELFR	Early Life Failure Rate
HAST	Biased HAST (Highly Accelerated Stress Test)
HBM	Electrostatic Discharge - Human Body Model
HTSL	High Temperature Storage Life
HTOL	High Temperature Operating Life
PC	Preconditioning
TC	Temperature Cycling
THB	Temperature Humidity Bias
UHAST	Unbiased HAST (Highly Accelerated Stress Test)

7. REVISION HISTORY

Release	Date	Description
Rev 01	Feb 08th, 2022	Initial release

TERMS OF USE

BY ACCEPTING THIS REPORT, YOU AGREE TO THE FOLLOWING TERMS OF USE:

This Reliability Evaluation Report (the “Report”) and all information contained herein is the property of STMicroelectronics (“ST”) and is provided solely for the purpose of obtaining general information relating to an ST product. Accordingly, you hereby agree to make use of this Report solely for the purpose of obtaining general information relating to the ST product. You further acknowledge and agree that this Report may not be used in or in connection with any legal or administrative proceeding in any court, arbitration, agency, commission or other tribunal or in connection with any action, cause of action, litigation, claim, allegation, demand or dispute of any kind. You further acknowledge and agree that this Report shall not be construed as an admission, acknowledgement or evidence of any kind, including, without limitation, as to the liability, fault or responsibility whatsoever of ST or any of its affiliates, or as to the accuracy or validity of the information contained herein, or concerning any alleged product issue, failure, or defect. ST does not promise that this Report is accurate or error free and specifically disclaims all warranties, express or implied, as to the accuracy of the information contained herein. Accordingly, you agree that in no event will ST or its affiliates be liable to you for any direct, indirect, consequential, exemplary, incidental, punitive, or other damages, including lost profits, arising from or relating to your reliance upon or use of this Report. You further acknowledge and agree that the use of this Report in violation of these Terms of Use would cause immediate and irreparable harm to ST which could not adequately be remedied by damages. You therefore agree that injunctive relief is an appropriate remedy to enforce these Terms of Use.

Disclosure of this document to any non-authorized party must be previously authorized by ST only under the provision of a proper confidentiality contractual arrangement executed between ST and you and must be treated as strictly confidential.

At all times you will comply with the following rules:

- Do not copy or reproduce all or part of this document
- Keep this document locked away
- Further copies can be provided on a "need to know basis", Please contact your local ST Sales Office or document writer

Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement, including, without limitation, the warranty provisions thereunder.

In that respect please note that ST products are not designed for use in some specific applications or environments described in above mentioned terms and conditions.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

Information furnished is believed to be accurate and reliable. However, ST assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license, express or implied, to any intellectual property right is granted by ST herein.

ST and ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously contained in any prior version of this document.

Document Revision History		
Date	Rev.	Description of the Revision
Mar. 14, 2022	1.00	Christian POLI - First draft creation

Source Documents & Reference Documents		
Source document Title	**Rev.:**	**Date:**