

# LMV7235, LMV7239 and LMV7239-Q1 75-ns, Ultra Low Power, Low Voltage, Rail-to-Rail Input Comparator with Open-Drain and Push-Pull Output

## 1 Features

- $V_S = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (Typical Values Unless Otherwise Specified)
- Propagation Delay 75 ns
- Low supply Current 65  $\mu\text{A}$
- Rail-to-Rail Input
- Open Drain and Push-pull Output
- Ideal for 2.7-V and 5-V Single Supply Applications
- Available in Space-saving Packages:
  - 5-pin SOT-23
  - 5-pin SC70
- LMV7239-Q1 is Qualified for Automotive Applications:
  - Device Temperature AEC-Q100 Grade 1:  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  Operating Range
  - Device HBM ESD Classification Level 1C

## 2 Applications

- Portable and Battery Powered Systems
- Set Top Boxes
- High Speed Differential Line Receiver
- Window Comparators
- Zero-crossing Detectors
- High Speed Sampling Circuits

## 3 Description

The LMV7235, LMV7239 and LMV7239-Q1 are ultra low power, low voltage, 75-ns comparators. They are guaranteed to operate over the full supply voltage range of 2.7 V to 5.5 V. These devices achieve a 75 ns propagation delay while consuming only 65  $\mu\text{A}$  of supply current at 5 V.

The LMV7235, LMV7239 and LMV7239-Q1 have a greater than rail-to-rail common mode voltage range. The input common mode voltage range extends 200 mV below ground and 200 mV above supply, allowing both ground and supply sensing.

The LMV7235 features an open drain output. By connecting an external resistor, the output of the comparator can be used as a level shifter.

The LMV7239 and LMV7239-Q1 features a push-pull output stage. This feature allows operation without the need of an external pull-up resistor.

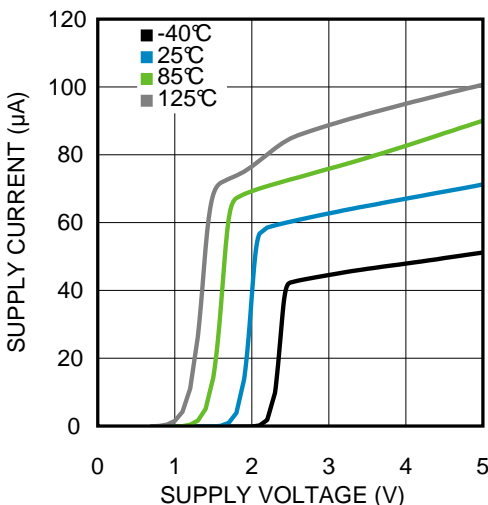
The LMV7235, LMV7239 and LMV7239-Q1 are available in the 5-Pin SC70 and 5-Pin SOT-23 packages, which are ideal for systems where small size and low power is critical.

### Device Information<sup>(1)</sup>

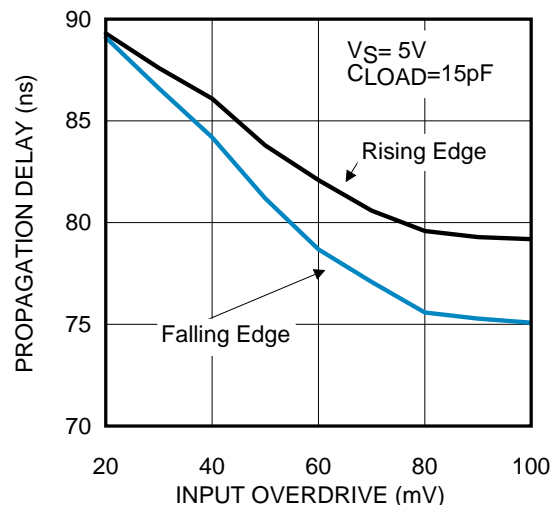
PART NUMBER	PACKAGES	BODY SIZE (NOM)
LMV7235, LMV7239 and LMV7239-Q1	SOT-23 (5)	2.90 mm x 1.60 mm
	SC70 (5)	2.00 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Supply Current vs. Supply Voltage



### Propagation Delay vs. Overdrive



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision M (February 2013) to Revision N

Page

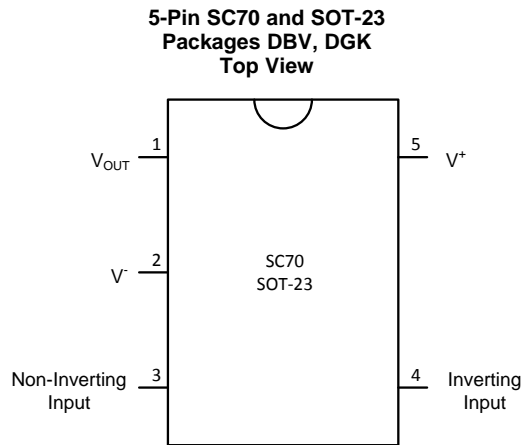
- Added, updated, or renamed the following sections: Device Information Table, *Pin Configuration and Functions*; *Specifications*. *Detailed Description* *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* .....

1

### Changes from Revision L (February 2013) to Revision M

Page

## 5 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V <sub>OUT</sub>	O	Output
2	V <sup>-</sup>	P	Negative Supply
3	IN <sup>+</sup>	I	Non-inverting Input
4	IN <sup>-</sup>	I	Inverting Input
5	V <sup>+</sup>	P	Positive Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Differential Input Voltage		± Supply Voltage	V
Output Short Circuit Duration		See <sup>(2)</sup>	
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )		6	V
<b>SOLDERING INFORMATION</b>			
Infrared or Convection (20 sec)		235	°C
Wave Soldering (10 sec)		260 (lead temp)	°C
Voltage at Input/Output Pins		(V <sup>+</sup> ) +0.3, (V <sup>-</sup> ) -0.3	V
Current at Input Pin <sup>(3)</sup>		±10	mA
Storage Temperature, T <sub>stg</sub>	-65	150	°C
Junction Temperature, T <sub>j</sub>		150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
- (3) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

### 6.2 ESD Ratings, LMV7235 and LMV7239

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
		Machine model (MM)	±100	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

### 6.3 ESD Ratings, LMV7239-Q1

				VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>		±1000	V
		Machine model (MM)		±100	
		Charged-device model (CDM), per AEC Q100-011 <sup>(1)</sup>	DBV package only	±750	

- (1) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 6.4 Recommended Operating Conditions

		MIN	MAX	UNIT
Supply Voltages (V <sup>+</sup> - V <sup>-</sup> )		2.7	5.5	V
Temperature Range <sup>(1)</sup>	LMV7235/LMV7239	-40	85	°C
	LMV7239Q	-40	125	°C

- (1) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC Board.

### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SC70	SOT-23	UNIT
		5 PINS	5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	478	265	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/an/spra953).

## 6.6 Electrical Characteristics, 2.7 V

Unless otherwise specified, all limits guaranteed for  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V^+/2$ ,  $V^+ = 2.7\text{ V}$ ,  $V^- = 0\text{ V}$ .  
 LMV7239 in table below also applies to LMV7239-Q1 unless noted.

		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{OS}$	Input Offset Voltage			0.8	6	mV
		At temp extremes			8	
$I_B$	Input Bias Current			30	400	nA
		At temp extremes			600	
$I_{OS}$	Input Offset Current			5	200	nA
		At temp extremes			400	
CMRR	Common Mode Rejection Ratio	$0\text{ V} < V_{CM} < 2.7\text{ V}^{(3)}$	52	62		dB
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7\text{ V}$ to $5\text{ V}$	65	85		dB
$V_{CM}$	Input Common-Mode Voltage Range	CMRR > 50 dB	$V^- - 0.1$	$-0.2$ to $2.9$	$V^+ + 0.1$	V
		At temp extremes	$V^-$		$V^+$	
$V_O$	Output Swing High (LMV7239 only)	$I_L = 4\text{ mA}$ , $V_{ID} = 500\text{ mV}$	$V^+ - 0.35$	$V^+ - 0.26$		V
		$I_L = 0.4\text{ mA}$ , $V_{ID} = 500\text{ mV}$		$V^+ - 0.02$		V
	Output Swing Low	$I_L = -4\text{ mA}$ , $V_{ID} = -500\text{ mV}$		230	350	mV
		At temp extremes			450	
		$I_L = -0.4\text{ mA}$ , $V_{ID} = -500\text{ mV}$		15		mV
$I_{SC}$	Output Short Circuit Current	Sourcing, $V_O = 0\text{ V}$ (LMV7239 only) <sup>(4)</sup>		15		mA
		Sinking, $V_O = 2.7\text{ V}$ (LMV7235, $R_L = 10\text{ k}$ ) <sup>(4)</sup>		20		mA
$I_S$	Supply Current	No load		52	85	$\mu\text{A}$
		At temp extremes			100	
$t_{PD}$	Propagation Delay	Overdrive = 20 mV $C_{LOAD} = 15\text{ pF}^{(5)}$		96		ns
		Overdrive = 50 mV $C_{LOAD} = 15\text{ pF}^{(5)}$		87		ns
		Overdrive = 100 mV $C_{LOAD} = 15\text{ pF}^{(5)}$		85		ns
$t_{SKEW}$	Propagation Delay Skew (LMV7239 only)	Overdrive = 20 mV <sup>(6)</sup>		2		ns
$t_r$	Output Rise Time	LMV7239/LMV7239Q 10% to 90%		1.7		ns
		LMV7235 10% to 90% <sup>(5)</sup>		112		ns
$t_f$	Output Fall Time	90% to 10%		1.7		ns
$I_{LEAKAGE}$	Output Leakage Current (LMV7235 only)			3		nA

- (1) All limits are guaranteed by testing or statistical analysis.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (3) CMRR is not linear over the common mode range. Limits are guaranteed over the worst case from 0 to  $V_{CC/2}$  or  $V_{CC/2}$  to  $V_{CC}$ .
- (4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of  $150^\circ\text{C}$ . Output currents in excess of  $\pm 30\text{ mA}$  over long term may adversely affect reliability.
- (5) A 10k pull-up resistor was used when measuring the LMV7235. The rise time of the LMV7235 is a function of the R-C time constant.
- (6) Propagation Delay Skew is defined as the absolute value of the difference between  $t_{PDLH}$  and  $t_{PDHL}$ .

## 6.7 Electrical Characteristics, 5 V

Unless otherwise specified, all limits guaranteed for  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V^+/2$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ .  
 LMV7239 in table below also applies to LMV7239-Q1 unless noted.

		TEST CONDITIONS		MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{OS}$	Input Offset Voltage				1	6	mV
		At temp extremes				8	
$I_B$	Input Bias Current				30	400	nA
		At temp extremes				600	
$I_{OS}$	Input Offset Current				5	200	nA
		At temp extremes				400	
CMRR	Common Mode Rejection Ratio	$0\text{V} < V_{CM} < 5\text{V}$		52	67		dB
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7\text{V}$ to $5\text{V}$		65	85		dB
$V_{CM}$	Input Common-Mode Voltage Range	CMRR > 50dB		$V^- - 0.1$	-0.2 to 5.2	$V^+ + 0.1$	V
			At temp extremes	$V^-$		$V^+$	
$V_O$	Output Swing High (LMV7239 only)	$I_L = 4\text{mA}$ , $V_{ID} = 500\text{mV}$		$V^+ - 0.25$	$V^+ - 0.15$		V
		$I_L = 0.4\text{mA}$ , $V_{ID} = 500\text{mV}$			$V^+ - 0.01$		V
	Output Swing Low	$I_L = -4\text{mA}$ , $V_{ID} = -500\text{mV}$			230	350	mV
		At temp extremes				450	mV
$I_{SC}$	Output Short Circuit Current	Sourcing, $V_O = 0\text{V}$ (LMV7239 only) <sup>(3)</sup>		25	55		mA
		At temp extremes		15			
		Sinking, $V_O = 5\text{V}$ (LMV7235, $R_L = 10\text{k}$ ) <sup>(3)</sup>		30	60		mA
		At temp extremes		20			
$I_S$	Supply Current	No load			65	95	$\mu\text{A}$
		At temp extremes				110	
$t_{PD}$	Propagation Delay	Overdrive = 20 mV $C_{LOAD} = 15\text{pF}$ <sup>(4)</sup>			89		ns
		Overdrive = 50 mV $C_{LOAD} = 15\text{pF}$ <sup>(4)</sup>			82		ns
		Overdrive = 100 mV $C_{LOAD} = 15\text{pF}$ <sup>(4)</sup>			75		ns
$t_{SKEW}$	Propagation Delay Skew (LMV7239 only)	Overdrive = 20 mV <sup>(5)</sup>			1		ns
$t_r$	Output Rise Time	LMV7239 10% to 90%			1.2		ns
		LMV7235 10% to 90% <sup>(4)</sup>			100		ns
$t_f$	Output Fall Time	90% to 10%			1.2		ns
$I_{LEAKAGE}$	Output Leakage Current (LMV7235 only)				3		nA

- (1) All limits are guaranteed by testing or statistical analysis.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of  $150^\circ\text{C}$ . Output currents in excess of  $\pm 30\text{mA}$  over long term may adversely affect reliability.
- (4) A 10k pull-up resistor was used when measuring the LMV7235. The rise time of the LMV7235 is a function of the R-C time constant.
- (5) Propagation Delay Skew is defined as the absolute value of the difference between  $t_{PDLH}$  and  $t_{PDHL}$ .

## 7 Typical Performance Characteristics

(Unless otherwise specified,  $V_S = 5V$ ,  $C_L = 10pF$ ,  $T_A = 25^\circ C$ ).

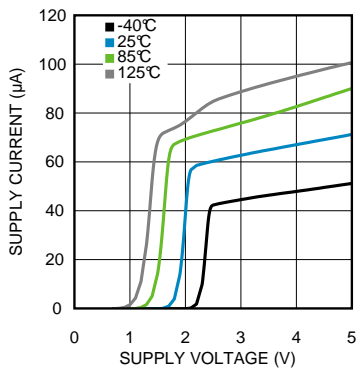


Figure 1. Supply Current vs. Supply Voltage

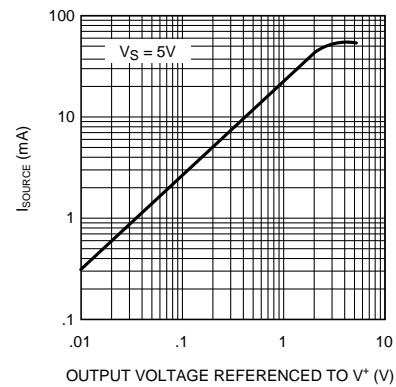


Figure 2. Sourcing Current vs. Output Voltage

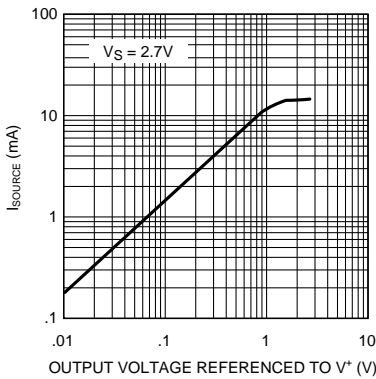


Figure 3. Sourcing Current vs. Output Voltage

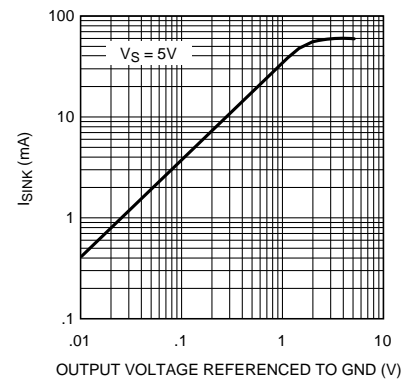


Figure 4. Sinking Current vs. Output Voltage

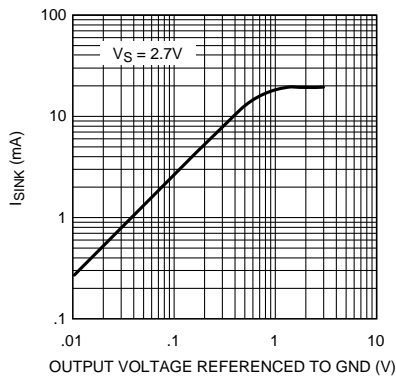


Figure 5. Sinking Current vs. Output Voltage

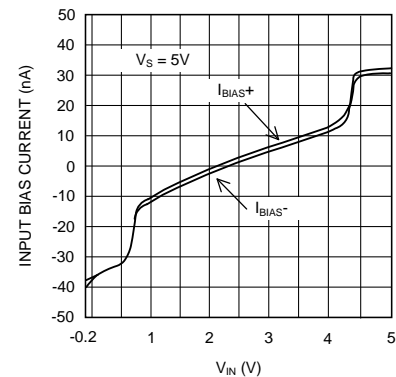


Figure 6. Input Bias Current vs. Input Voltage

### Typical Performance Characteristics (continued)

(Unless otherwise specified,  $V_S = 5V$ ,  $C_L = 10pF$ ,  $T_A = 25^\circ C$ ).

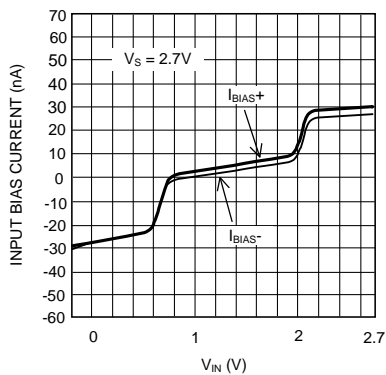


Figure 7. Input Bias Current vs. Input Voltage

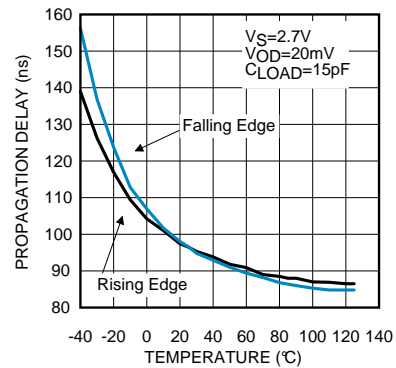


Figure 8. Propagation Delay vs. Temperature

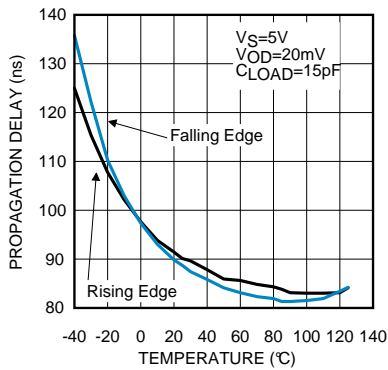


Figure 9. Propagation Delay vs. Temperature

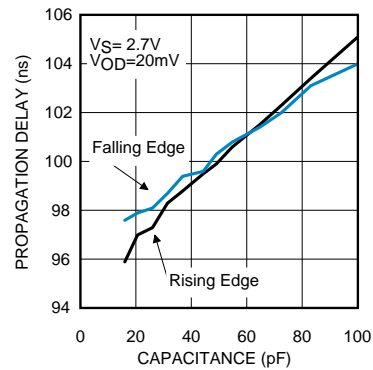


Figure 10. Propagation Delay vs. Capacitive Load

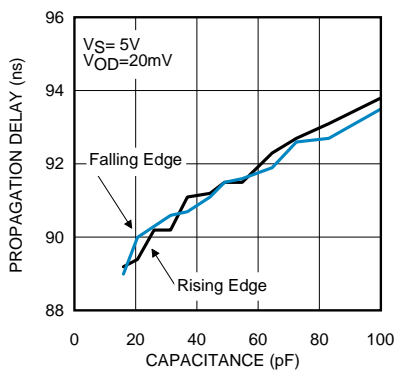


Figure 11. Propagation Delay vs. Capacitive Load

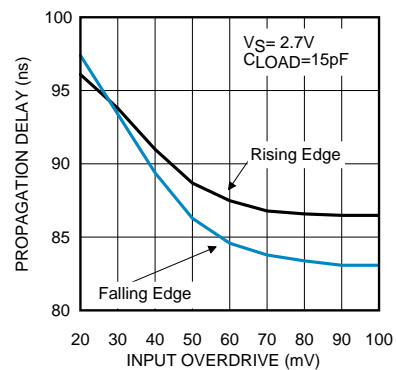
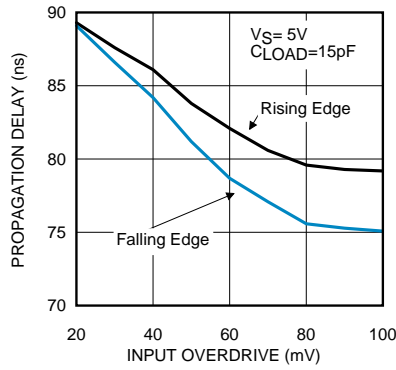


Figure 12. Propagation Delay vs. Input Overdrive

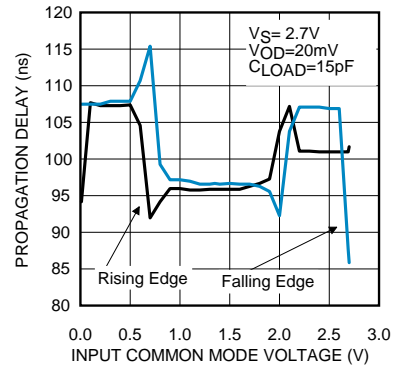


**Typical Performance Characteristics (continued)**

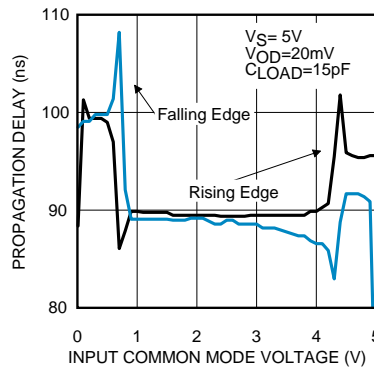
(Unless otherwise specified,  $V_S = 5V$ ,  $C_L = 10pF$ ,  $T_A = 25^\circ C$ ).



**Figure 13. Propagation Delay vs. Input Overdrive**



**Figure 14. Propagation Delay vs. Common Mode Voltage**



**Figure 15. Propagation Delay vs. Common Mode Voltage**

## 8 Detailed Description

### 8.1 Overview

The LMV7235, LMV7239 and LMV7239-Q1 are ultra low power, low voltage, 75-ns comparators. They are guaranteed to operate over the full supply voltage range of 2.7 V to 5.5 V. These devices achieve a 75-ns propagation delay while consuming only 65  $\mu$ A of supply current at 5 V.

The LMV7235, LMV7239 and LMV7239-Q1 have a greater than rail-to-rail common mode voltage range. The input common mode voltage range extends 200 mV below ground and 200 mV above supply, allowing both ground and supply sensing.

### 8.2 Functional Block Diagram



**Simplified Schematic of LMV7239**

### 8.3 Feature Description

#### 8.3.1 Input Stage

The LMV7235, LMV7239 and LMV7239-Q1 are rail-to-rail input and output. The typical input common mode voltage range of  $-0.2$  V below the ground to  $0.2$  V above the supply. The LMV7235, LMV7239 and LMV7239-Q1 use a complimentary PNP and NPN input stage in which the PNP stage senses common mode voltage near  $V_{-}$  and the NPN stage senses common mode voltage near  $V^{+}$ . If either of the input signals falls below the negative common mode limit, the parasitic PN junction formed by the substrate and the base of the PNP will turn on resulting in an increase of input bias current.

If one of the inputs goes above the positive common mode limit, the output will still maintain the correct logic level as long as the other input stays within the common mode range. However, the propagation delay will increase. When both inputs are outside the common mode voltage range, current saturation occurs in the input stage, and the output becomes unpredictable.

The propagation delay does not increase significantly with large differential input voltages. However, large differential voltages greater than the supply voltage should be avoided to prevent damage to the input stage.

#### 8.3.2 Output Stage, LMV7239 and LMV7239-Q1

The LMV7239 has a push-pull output. When the output switches, there is a low resistance path between  $V_{CC}$  and ground, causing high output sinking or sourcing current during the transition.

## Feature Description (continued)

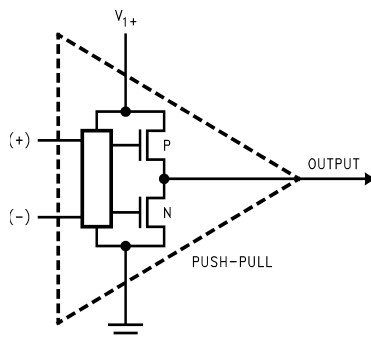


Figure 16. LMV7239 Push-Pull Output Stage

### 8.3.3 Output Stage, LMV7235

The LMV7235 has an open drain that requires a pull-up resistor to a positive supply voltage for the output to switch properly. The internal circuitry is identical to the LMV7239 except that the upper P channel output device M4 is absent in the [Functional Block Diagram](#) above. When the internal output transistor is off, the output voltage will be pulled up to the external positive voltage by the external pull-up resistor. This allows the output to be OR'ed with other open drain outputs on the same bus. The output pull-up resistor can be connected to any voltage level between V- and V+ for level shifting applications.

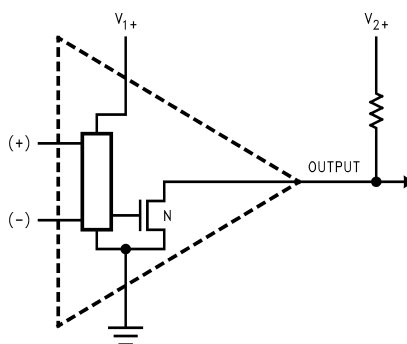


Figure 17. LMV7235 Open Drain Output

## 8.4 Device Functional Modes

### 8.4.1 Capacitive and Resistive Loads

The propagation delay is not affected by capacitive loads at the output of the LPV7239 or LMV7239-Q1. However, resistive loads slightly effect the propagation delay on the falling edge depending on the load resistance value.

The propagation delay on the rising edge of the LMV7235 depends on the load resistance and capacitance values.

### 8.4.2 Noise

Most comparators have rather low gain. This allows the output to spend time between high and low when the input signal changes slowly. The result is the output may oscillate between high and low when the differential input is near zero. The high gain of this comparator eliminates this problem. Less than 1  $\mu\text{V}$  of change on the input will drive the output from one rail to the other rail. If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback. (See [Hysteresis](#).)

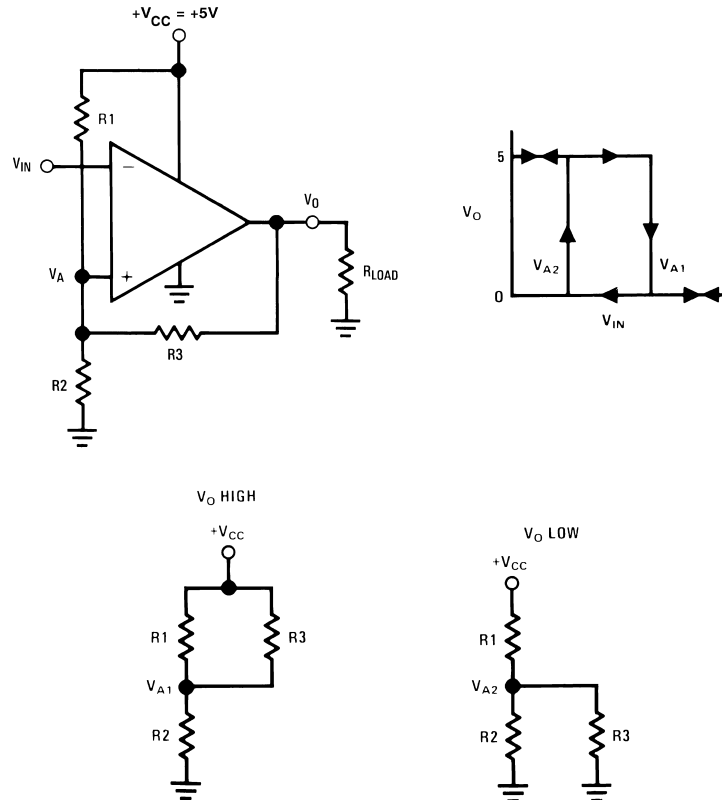
## Device Functional Modes (continued)

### 8.4.3 Hysteresis

In order to improve propagation delay when low overdrive is needed hysteresis can be added.

#### 8.4.3.1 Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage  $V^+$  of the comparator as shown in Figure 18. When  $V_{IN}$  at the inverting input is less than  $V_{A1}$ , the voltage at the non-inverting node of the comparator ( $V_{IN} < V_{A1}$ ), the output voltage is high (for simplicity assume  $V_O$  switches as high as  $V^+$ ). The three network resistors can be represented as  $R_1 // R_3$  in series with  $R_2$ .



**Figure 18. Inverting Comparator with Hysteresis**

The lower input trip voltage  $V_{A1}$  is defined as:

$$V_{A1} = V_{CC} R_2 / [(R_1 // R_3) + R_2]. \quad (1)$$

When  $V_{IN}$  is greater than  $V_{A1}$ , the output voltage is low or very close to ground. In this case the three network resistors can be presented as  $R_2 // R_3$  in series with  $R_1$ .

The upper trip voltage  $V_{A2}$  is defined as:

$$V_{A2} = V_{CC} (R_2 // R_3) / [(R_1) + (R_2 // R_3)] \quad (2)$$

The total hysteresis provided by the network is defined as  $\Delta V_A = V_{A1} - V_{A2}$ .

$$\Delta V_A = \frac{+V_{CC} R_1 R_2}{R_1 R_2 + R_1 R_3 + R_2 R_3} \quad (3)$$

#### 8.4.3.2 Non-Inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference ( $V_{REF}$ ) at the inverting input. When  $V_{IN}$  is low, the output is also low. For the output to switch from low to high,  $V_{IN}$  must rise up to  $V_{IN1}$  where  $V_{IN1}$  is calculated by:

## Device Functional Modes (continued)

$$\Delta V_{IN1} = \frac{V_{REF}(R_1 + R_2)}{R_2} \quad (4)$$

As soon as  $V_O$  switches to  $V_{CC}$ ,  $V_A$  steps to a value greater than  $V_{REF}$  which is given by:

$$V_A = V_{IN} + \frac{(V_{CC} - V_{IN1})R_1}{R_1 + R_2} \quad (5)$$

To make the comparator switch back to its low state,  $V_{IN}$  must equal  $V_{REF}$  before  $V_A$  will again equal  $V_{REF}$ .  $V_{IN2}$  can be calculated by:

$$V_{IN2} = \frac{V_{REF}(R_1 + R_2) - V_{CC}R_1}{R_2} \quad (6)$$

The hysteresis of this circuit is the difference between  $V_{IN1}$  and  $V_{IN2}$ .

$$\Delta V_{IN} = V_{CC}R_1 / R_2 \quad (7)$$

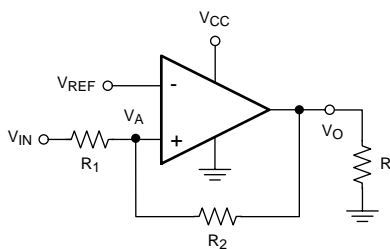


Figure 19. Non-Inverting Comparator with Hysteresis

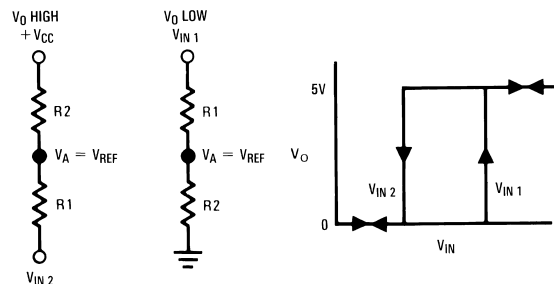


Figure 20. Non-Inverting Comparator Thresholds

### 8.4.4 Zero Crossing Detector

In a zero crossing detector circuit, the inverting input is connected to ground and the non-inverting input is connected to a 100 mV<sub>PP</sub> AC signal. As the signal at the non-inverting input crosses 0V, the comparator's output changes state.

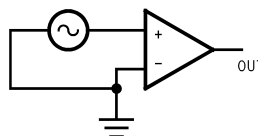


Figure 21. Simple Zero Crossing Detector

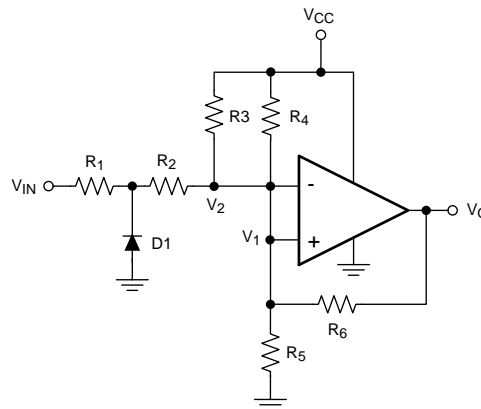
#### 8.4.4.1 Zero Crossing Detector with Hysteresis

To improve switching times and centering the input threshold to ground a small amount of positive feedback is added to the circuit. Voltage divider  $R_4$  and  $R_5$  establishes a reference voltage,  $V_1$ , at the positive input. By making the series resistance,  $R_1$  plus  $R_2$  equal to  $R_5$ , the switching condition,  $V_1 = V_2$ , will be satisfied when  $V_{IN} = 0$ .

## Device Functional Modes (continued)

The positive feedback resistor,  $R_6$ , is made very large with respect to  $R_5 \parallel R_6 = 2000 R_5$ ). The resultant hysteresis established by this network is very small ( $\Delta V_1 < 10 \text{ mV}$ ) but it is sufficient to insure rapid output voltage transitions.

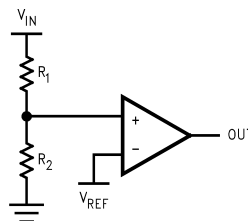
Diode  $D_1$  is used to insure that the inverting input terminal of the comparator never goes below approximately  $-100 \text{ mV}$ . As the input terminal goes negative,  $D_1$  will forward bias, clamping the node between  $R_1$  and  $R_2$  to approximately  $-700 \text{ mV}$ . This sets up a voltage divider with  $R_2$  and  $R_3$  preventing  $V_2$  from going below ground. The maximum negative input overdrive is limited by the current handling ability of  $D_1$ .



**Figure 22. Zero Crossing Detector with Hysteresis**

### 8.4.5 Threshold Detector

Instead of tying the inverting input to  $0\text{V}$ , the inverting input can be tied to a reference voltage. As the input on the non-inverting input passes the  $V_{\text{REF}}$  threshold, the comparator's output changes state. It is important to use a stable reference voltage to ensure a consistent switching point.



**Figure 23. Threshold Detector**

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LMV7235, LMV7239 and LMV7239-Q1 are single supply comparators with 75 ns of propagation delay and only 65  $\mu$ A of supply current.

### 9.2 Typical Applications

#### 9.2.1 Square Wave Oscillator

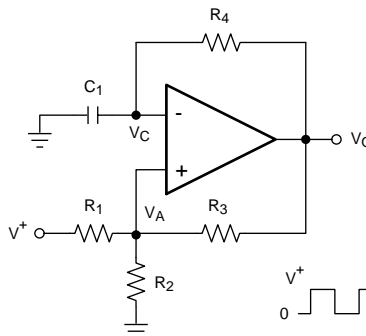


Figure 24. Square Wave Oscillator

##### 9.2.1.1 Design Requirements

A typical application for a comparator is as a square wave oscillator. The circuit in Figure 24 generates a square wave whose period is set by the RC time constant of the capacitor  $C_1$  and resistor  $R_4$ .

##### 9.2.1.2 Detailed Design Procedure

The maximum frequency is limited by the large signal propagation delay of the comparator and by the capacitive loading at the output, which limits the output slew rate.

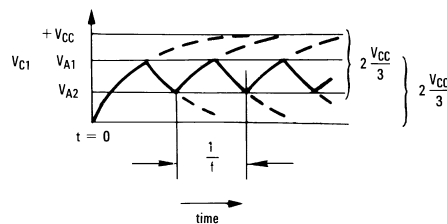


Figure 25. Square Wave Oscillator Timing Thresholds

Consider the output of Figure 24 to be high to analyze the circuit. That implies that the inverted input ( $V_C$ ) is lower than the non-inverting input ( $V_A$ ). This causes the  $C_1$  to be charged through  $R_4$ , and the voltage  $V_C$  increases until it is equal to the non-inverting input. The value of  $V_A$  at this point is:

$$V_{A1} = \frac{V_{CC} \cdot R_2}{R_2 + R_1 \parallel R_3} \quad (8)$$

If  $R_1 = R_2 = R_3$ , then  $V_{A1} = 2 V_{CC}/3$

## Typical Applications (continued)

At this point the comparator switches pulling down the output to the negative rail. The value of  $V_A$  at this point is:

$$V_{A2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + (R_2 \parallel R_3)} \quad (9)$$

If  $R_1 = R_2 = R_3$ , then  $V_{A2} = V_{CC}/3$ .

The capacitor  $C_1$  now discharges through  $R_4$ , and the voltage  $V_C$  decreases until it is equal to  $V_{A2}$ , at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge  $C_1$  from  $2V_{CC}/3$  to  $V_{CC}/3$ , which is given by  $R_4 C_1 \cdot \ln 2$ . Hence the formula for the frequency is:

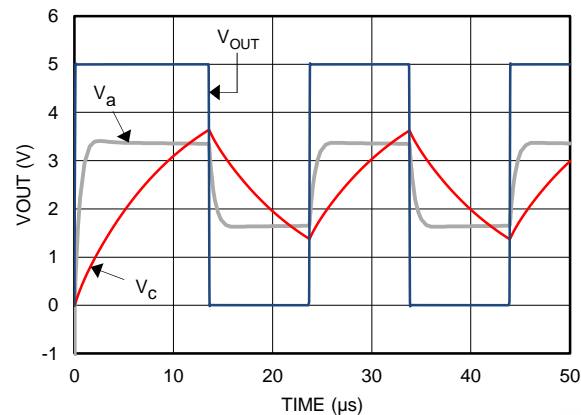
$$F = 1/(2 \cdot R_4 \cdot C_1 \cdot \ln 2) \quad (10)$$

The LMV7239 should be used for a symmetrical output. The LMV7235 will require a pull-up resistor on the output to function, and will have a slightly asymmetrical output due to the reduced sourcing current.

### 9.2.1.3 Application Curves

Figure [Figure 26](#) shows the simulated results of an oscillator using the following values:

1.  $R_1 = R_2 = R_3 = R_4 = 100\text{k}\Omega$
2.  $C_1 = 100\text{pF}$ ,  $C_L = 20\text{pF}$
3.  $V_+ = 5\text{V}$ ,  $V_- = \text{GND}$
4.  $C_{\text{STRAY}}$  (not shown) from  $V_a$  to  $\text{GND} = 10\text{pF}$



**Figure 26. Square Wave Oscillator Output Waveform**

### 9.2.2 Crystal Oscillator

A simple crystal oscillator using the LMV7235, LMV7239 and LMV7239-Q1 is shown in [Figure 27](#). Resistors  $R_1$  and  $R_2$  set the bias point at the comparator's non-inverting input. Resistors,  $R_3$  and  $R_4$  and capacitor  $C_1$  set the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent by the comparator



## Typical Applications (continued)

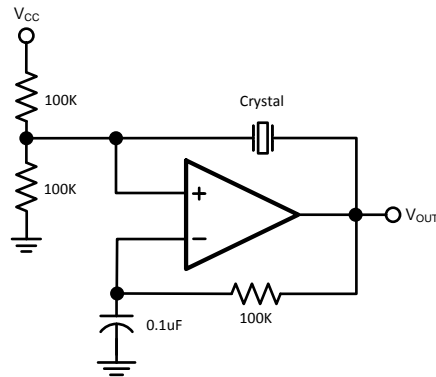


Figure 27. Crystal Oscillator

### 9.2.3 Infrared (IR) Receiver

The LMV7235, LMV7239 and LMV7239-Q1 can also be used as an infrared receiver. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across  $R_D$ . When this voltage level crosses the voltage applied by the voltage divider to the inverting input, the output transitions.

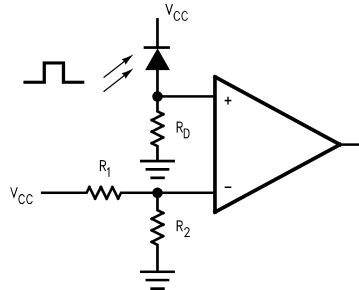


Figure 28. IR Receiver

### 9.2.4 Window Detector

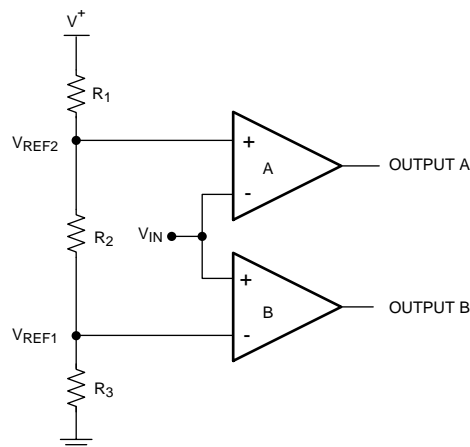
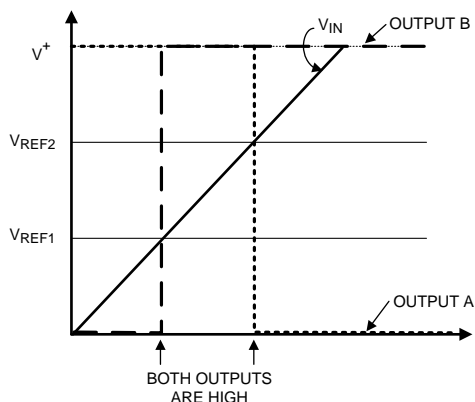


Figure 29. Window Detector

A window detector monitors the input signal to determine if it falls between two voltage levels. Both outputs are true (high) when  $V_{REF1} < V_{IN} < V_{REF2}$

## Typical Applications (continued)



**Figure 30. Window Detector Output Signal**

The comparator outputs A and B are high only when  $V_{REF1} < V_{IN} < V_{REF2}$ , or "within the window", where these are defined as:

$$V_{REF1} = R_3 / (R_1 + R_2 + R_3) * V_+ \quad (11)$$

$$V_{REF2} = (R_2 + R_3) / (R_1 + R_2 + R_3) * V_+ \quad (12)$$

To determine if the input signal falls outside of the two voltage levels, both inputs on each comparators can be reversed to invert the logic.

The LMV7235 with an open drain output should be used if the outputs are to be tied together for a common logic output.

Other names for window detectors are: threshold detector, level detector, and amplitude trigger or detector.

## 10 Power Supply Recommendations

To minimize supply noise, power supplies should be decoupled by a 0.01  $\mu$ F ceramic capacitor in parallel with a 10  $\mu$ F capacitor.

Due to the nanosecond edges on the output transition, peak supply currents will be drawn during the time the output is transitioning. Peak current depends on the capacitive loading on the output. The output transition can cause transients on poorly bypassed power supplies. These transients can cause a poorly bypassed power supply to "ring" due to trace inductance and low self-resonance frequency of high ESR bypass capacitors.

Treat the LMV7235, LMV7239 and LMV7239-Q1 as a high-speed device. Keep the ground paths short and place small (low ESR ceramic) bypass capacitors directly between the V+ and V- pins.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

## 11 Layout

### 11.1 Layout Guidelines

Proper grounding and the use of a ground plane will help to ensure the specified performance of the LMV7235, LMV7239 and LMV7239-Q1. Minimizing trace lengths, reducing unwanted parasitic capacitance and using surface-mount components will also help. Comparators are very sensitive to input noise.

The LMV7235, LMV7239 and LMV7239-Q1 require high speed layout. Follow these layout guidelines:

1. Use printed circuit board with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1 $\mu$ F ceramic surface mount capacitor) as close as possible to  $V_{CC}$  pin.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from output.
4. Solder the device directly to the printed circuit board rather than using a socket.
5. For slow moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to  $t_{PD}$  when the source impedance is low.
6. The topside ground plane runs between the output and inputs.
7. Ground trace from the ground pin runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

### 11.2 Layout Example

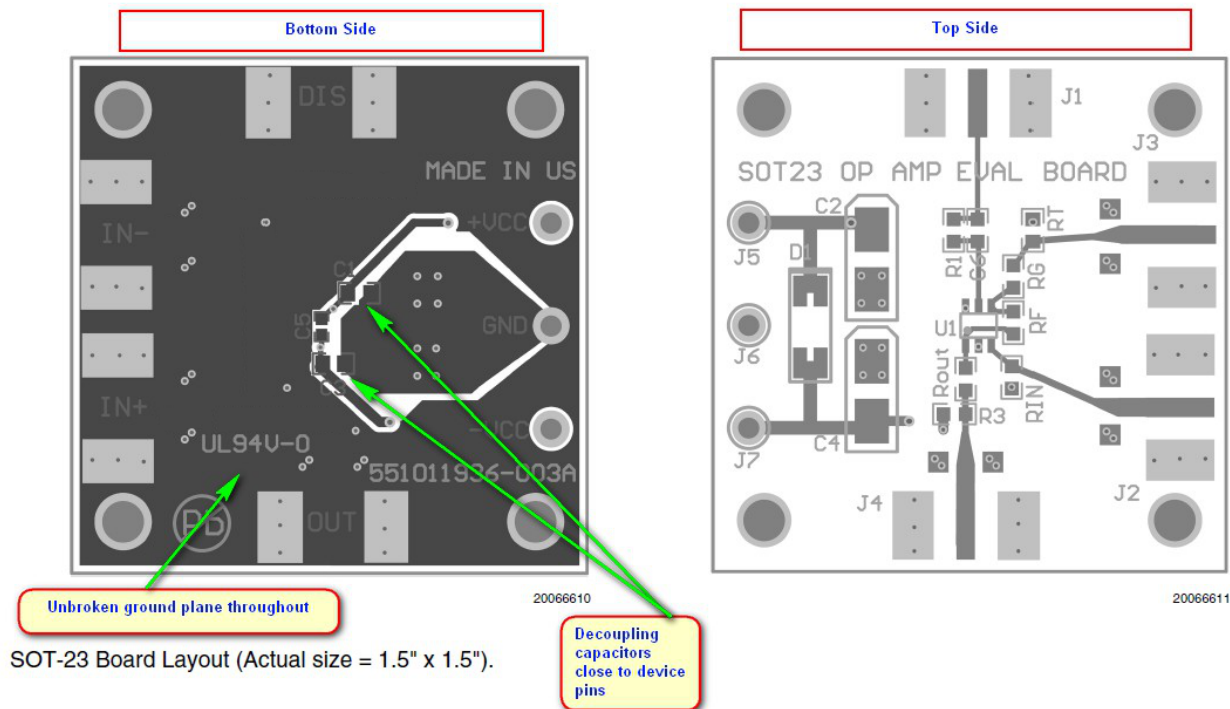


Figure 31. SOT-23 Board Layout Example

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

LMV7239 TINA SPICE Model, [SNOM392](#)

TINA-TI SPICE-Based Analog Simulation Program, <http://www.ti.com/tool/tina-ti>

DIP Adapter Evaluation Module, <http://www.ti.com/tool/dip-adapter-evm>

TI Universal Operational Amplifier Evaluation Module, <http://www.ti.com/tool/opampevm>

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

AN-74 - A Quad of Independently Functioning Comparators, [SNOA654](#)

### 12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV7235	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LMV7239	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LMV7239-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.4 Trademarks

All trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV7235M5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	C21A	
LMV7235M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C21A	<a href="#">Samples</a>
LMV7235M5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	C21A	
LMV7235M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C21A	<a href="#">Samples</a>
LMV7235M7	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	C21	
LMV7235M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C21	<a href="#">Samples</a>
LMV7235M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C21	<a href="#">Samples</a>
LMV7239M5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	C20A	
LMV7239M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C20A	<a href="#">Samples</a>
LMV7239M5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	C20A	
LMV7239M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C20A	<a href="#">Samples</a>
LMV7239M7	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	C20	
LMV7239M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C20	<a href="#">Samples</a>
LMV7239M7X	NRND	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 85	C20	
LMV7239M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C20	<a href="#">Samples</a>
LMV7239QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	ZBMX	<a href="#">Samples</a>
LMV7239QM7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C42	<a href="#">Samples</a>
LMV7239QM7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	C42	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

---

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LMV7239, LMV7239-Q1 :**

- Catalog: [LMV7239](#)
- Automotive: [LMV7239-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



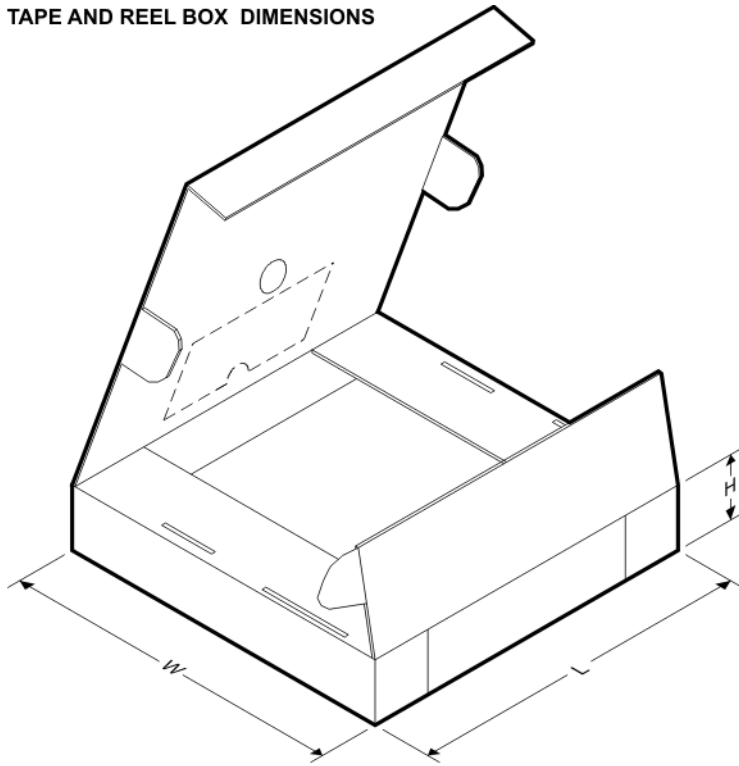
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7235M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7235M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7235M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M7X	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239QDBVRQ1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239QM7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239QM7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7235M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7235M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7235M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7235M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7235M7	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7235M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7235M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV7239M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7239M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7239M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7239M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7239M7	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7239M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7239M7X	SC70	DCK	5	3000	210.0	185.0	35.0
LMV7239M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV7239QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7239QM7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7239QM7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

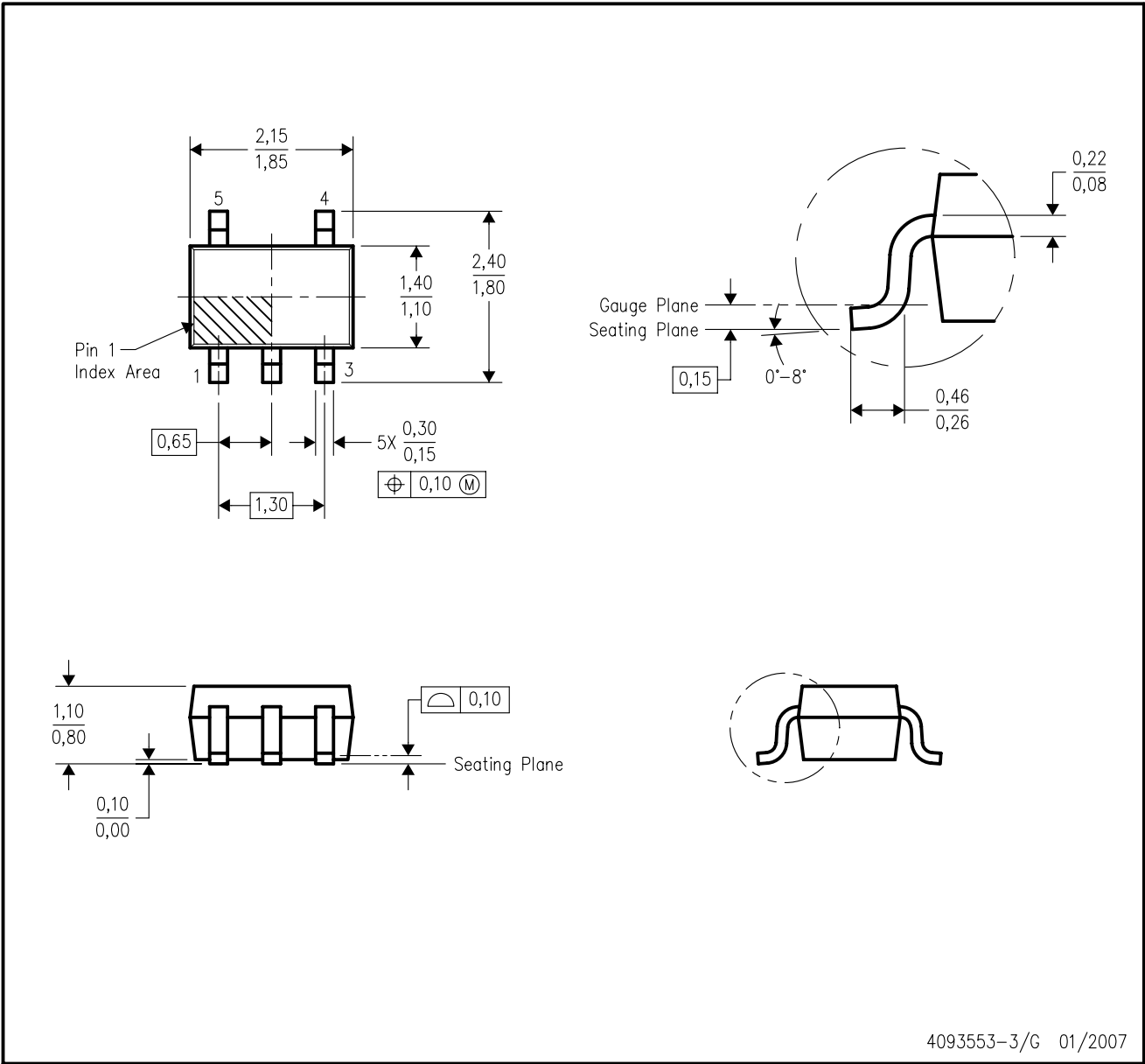
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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