# Product Change Notification - SYST-10VKBQ169

**Date:**

11 Jul 2019

**Product Category:**

8-bit Microcontrollers

**Affected CPNs:**

**Notification subject:**

ERRATA - PIC16(L)F15324/44 Family Silicon Errata and Data Sheet Clarification

**Notification text:**

SYST-10VKBQ169

Microchip has released a new DeviceDoc for the PIC16(L)F15324/44 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC16(L)F15324/44 Family Silicon Errata and Data Sheet Clarification.

**Notification Status:** Final

**Description of Change:** Updated Table 1, Table 2 and section 1. Added new section 3, section 4 and section 5. Added section 6. Other minor corrections.
Data Sheet Clarifications:
Added Module 1: Table 36.3 Instruction Set

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 11 Jul 2019

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

**Attachment(s):**

PIC16(L)F15324/44 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC16F15324-E/7NVAO
PIC16F15324-E/JQ
PIC16F15324-E/JQV04
PIC16F15324-E/JQVAO
PIC16F15324-E/P
PIC16F15324-E/SL
PIC16F15324-E/SLVAO
PIC16F15324-E/ST
PIC16F15324-I/7N
PIC16F15324-I/7NVAO
PIC16F15324-I/JQ
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PIC16F15324-I/SL
PIC16F15324-I/SLC02
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PIC16F15324-I/ST
PIC16F15324T-E/7NVAO
PIC16F15324T-E/JQVAO
PIC16F15324T-E/SL
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PIC16F15344-E/P
PIC16F15344-E/SO
PIC16F15344-E/SS
PIC16F15344-I/GZ
PIC16F15344-I/ML
PIC16F15344-I/MLC01
PIC16F15344-I/MLVAO
PIC16F15344-I/P
PIC16F15344-I/SO
PIC16F15344-I/SS
PIC16F15344T-E/SS
PIC16F15344T-E/SSVAO
PIC16F15344T-I/GZ
PIC16F15344T-I/ML
PIC16F15344T-I/MLC01

PIC16F15344T-I/MLVAO
PIC16F15344T-I/SO
PIC16F15344T-I/SS
PIC16LF15324-E/JQ
PIC16LF15324-E/P
PIC16LF15324-E/SL
PIC16LF15324-E/ST
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PIC16LF15324-I/P
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PIC16LF15344-I/SO
PIC16LF15344-I/SS
PIC16LF15344T-I/GZ
PIC16LF15344T-I/SO
PIC16LF15344T-I/SS

# PIC16(L)F15324/44

## PIC16(L)F15324/44 Family
## Silicon Errata and Data Sheet Clarification

The PIC16(L)F15324/44 family devices that you have received conform functionally to the current Device Data Sheet (DS40001889**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F15324/44 silicon.

| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**). |
|---|---|

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

| **Note:** | If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance. |
|---|---|

The DEVREV values for the various PIC16(L)F15324/44 silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Device ID(1) | Revision ID for Silicon Revision(2) | |
|---|---|---|---|
| | | A1 | A3 |
| PIC16F15324 | 30C2h | 2001h | 2003h |
| PIC16LF15324 | 30C3h | 2001h | 2003h |
| PIC16F15344 | 30C4h | 2001h | 2003h |
| PIC16LF15344 | 30C5h | 2001h | 2003h |

**Note 1:** The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

**2:** Refer to the *"PIC16(L)F153XX Memory Programming Specification"* (DS40001838) for detailed information on Device and Revision IDs for your specific device.

**TABLE 2: SILICON ISSUE SUMMARY**

| Module | Feature | Item Number | Issue Summary | Affected Revisions | |
|---|---|---|---|---|---|
| | | | | A1 | A3 |
| Electrical Specifications | SMBus | 1.1 | The maximum $V_{IL}$ level changes when $V_{DD}$ is below 4.0V at 125°C. | X | |
| | Fixed Voltage Reference (FVR) Accuracy | 1.2 | Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C. | X | X |
| | Minimum $V_{DD}$ Specification for LF Devices | 1.3 | $V_{DD}$ Min for LF devices is 2.0V. | X | X |
| Master Synchronous Serial Port (MSSP) | SPI Slave mode | 2.1 | SSPBUF transmit shift register may be corrupted under certain conditions. | X | |
| Nonvolatile Memory | WRERR Bit Operation | 3.1 | When performing a NVM high-voltage operation, if a Reset is issued in the middle of the operation, the WRERR bit is set. Then, if the user clears the WRERR bit and a Reset occurs again, this sets the WRERR bit because the internal latch has not been cleared earlier. | X | |
| Windowed Watchdog Timer (WWDT) | Window Operation in DOZE mode | 4.1 | Window feature of the WWDT does not operate correctly in DOZE mode. | X | |
| Timer0 | Timer0 Clock Source | 5.1 | Operation of Timer0 is incorrect when $F_{OSC}$/4 is used as the clock source. | X | |
| Reference Clock Output Module (CLKR) | CLKR Output | 6.1 | First output pulse of reference clock output module is incorrect when CLKREN is enabled | X | X |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

### 1. Module: Electrical Specifications

#### 1.1 SMBus 2.0 VIL Level

At 125°C when the VDD voltage level supplied to the device is 4.0V and above, the maximum SMBus 2.0 voltage level for the VIL parameter is 0.8V. When VDD drops below 4.0V, the maximum SMBus voltage level for VIL drops to 0.7V. This issue applies to extended temperature devices only.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

#### 1.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

**Work around**

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

**Affected Silicon Revisions**

| A1 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

#### 1.3 Min VDD Specification for LF Devices

Nonvolatile memory (NVM) access on LF devices may not work when operating at temperatures between -40°C and +25°C and VDD levels below 2.0V. VDD_MIN for parameter (D002) is 2.0V for temperatures between -40°C and 25°C.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 2. Module: Master Synchronous Serial Port (MSSP)

#### 2.1 SSPBUF may become corrupted

When operating in SPI Slave mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF transmit shift register may become corrupted. The transmitted slave byte cannot be guaranteed to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM prior to an SFR read

**Work around**

**Method 1 (Interrupt Based Using SS):**

1. Connect the SS line to both the SS input and either an INT or IOC input pin.
2. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that SS == 0 when the interrupt occurs).
3. Load SSPBUF with the data to be transmitted.
4. Continue program execution.
5. When the Interrupt Service Routine (ISR) is invoked, do either of the following:

   • Add a delay that ensures the first SCK clock will be complete, or

   • Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

   Once either of these are complete, it is safe to return to program execution.

**Method 2 (Bit Polling Based Using SS):**

1. Load SSPBUF with the data to be transmitted.
2. Poll the SS line and wait for the SS to go active (while(!PORTx.nSS == 0)).
3. When SS is active (SS == 0), do either of the following:

   • Add a delay that ensures the first SCK clock will be complete, or

   • Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

   Once one of these two methods are complete, it is safe to return to program execution.

**Method 3 (SS not Available):**

1. Load SSPBUF with the data to be transmitted.

2. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

**Affected Silicon Revisions**

| A1 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 3. Module: Nonvolatile Memory

### 3.1 WRERR Bit Operation

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit of the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset occurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the WRERR condition.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 4. Module: Windowed Watchdog Timer (WWDT)

### 4.1 Window Feature of the WWDT does not Operate Correctly in DOZE Mode

When the Windowed mode of operation is enabled in DOZE mode, a window violation error is issued even though the window is open and has been armed. This condition occurs only when the window size is set to a value other than 100% open.

**Work around**

1. Use the Windowed mode of operation in any other mode than DOZE. If disabling the DOZE mode is not an option, use the WWDT module without the window being enabled.
2. If the device is in DOZE mode, perform the arming process for the window in NORMAL mode, and return to the DOZE mode.
3. If there is an ISR in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

**Affected Silicon Revisions**

| A1 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 5. Module: Timer0

### 5.1 Operation of Timer0 is Incorrect when Fosc/4 is Used as the Clock Source

Clearing the T0ASYNC bit in the T0CON1 register when Timer0 is configured to use FOSC/4 may cause incorrect behavior. This issue is only valid when FOSC/4 is used as the clock source.

**Work around**

Set the T0ASYNC bit in the T0CON1 register when using FOSC/4 as the Timer0 clock.

**Affected Silicon Revisions**

| A1 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 6. Module: Reference Clock Output Module (CLKR)

### 6.1 First Output Pulse of Reference Clock Output Module is Incorrect When CLKREN is Enabled

If CLKREN bit is set by the user, the number of input clock cycles taken to generate the reference clock output might vary by one cycle due to a race condition. This condition occurs only if LCx_out or NCOx_out are the inputs (CLKRCLK bits) to the CLKR module.

**Work around**

Ignore the first output pulse of the CLKR output signal.

**Affected Silicon Revisions**

| A1 | A3 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001889**B**):

| | |
|---|---|
| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |

### 1. Module: Table 36.3 Instruction Set Literal Operations

| LITERAL OPERATIONS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| ADDLW | k | Add literal and W | 1 | 11 | 1110 | kkkk | kkkk | C, DC, Z | |
| ANDLW | k | AND literal with W | 1 | 11 | 1001 | kkkk | kkkk | Z | |
| IORLW | k | Inclusive OR literal with W | 1 | 11 | 1000 | kkkk | kkkk | Z | |
| **MOVLB** | **k** | **Move literal to BSR** | **1** | **00** | **0001** | **01kk** | **kkkk** | | |
| MOVLP | k | Move literal to PCLATH | 1 | 11 | 0001 | 1kkk | kkkk | | |
| MOVLW | k | Move literal to W | 1 | 11 | 0000 | kkkk | kkkk | | |
| SUBLW | k | Subtract W from literal | 1 | 11 | 1100 | kkkk | kkkk | C, DC, Z | |
| XORLW | k | Exclusive OR literal with W | 1 | 11 | 1010 | kkkk | kkkk | Z | |

## APPENDIX A: DOCUMENT REVISION HISTORY

### Rev B Document (7/2019)

Updated Table 1, Table 2 and section 1. Added new section 3, section 4 and section 5. Added section 6. Other minor corrections.

**Data Sheet Clarifications:**

Added Module 1: Table 36.3 Instruction Set

### Rev A Document (3/2017)

Initial release of this document.

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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