# 56F8367

Evaluation Module User Manual

**56F8300**
**16-bit Digital Signal Controllers**

MC56F8367EVMUM
Rev. 2
07/2005

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## Document Revision History

| Version History | Description of Change |
|---|---|
| Rev 1.0 | Initial Public Release |
| Rev 2.0 | Updated look and feel |

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# Preface

This reference manual describes in detail the hardware on the 56F8367 Evaluation Module.

## Audience

This document is intended for application developers who are creating software for devices using the Freescale 56F8367 part or a member of the 56F8300 family that is compatible with this part. Examples would include the 56F8346 and the 56F8357 devices.

## Organization

This manual is organized into two chapters and two appendices:

- **Chapter 1, Introduction** provides an overview of the EVM and its features.
- **Chapter 2, Technical Summary** describes in detail the 56F8367 hardware.
- **Appendix A, "56F8367EVM Schematics"**contains the schematics of the MC56F8367EVM.
- **Appendix B, "56F8367EVM Bill of Material"** provides a list of the materials used on the MC56F8367EVM board.

## Suggested Reading

More documentation on the 56F8367 and the MC56F8367EVM kit may be found at URL:

**www.freescale.com**

# Notation Conventions

This manual uses the following notational conventions:

| Term or Value | Symbol | Examples | Exceptions |
|---|---|---|---|
| Active High Signals (Logic One) | No special symbol attached to the signal name | A0<br>CLKO | |
| Active Low Signals (Logic Zero) | Noted with an overbar in text and in most figures | $\overline{WE}$<br>$\overline{OE}$ | In schematic drawings, Active Low Signals may be noted by a backslash: /WE |
| Hexadecimal Values | Begin with a “$” symbol | $0FF0<br>$80 | |
| Decimal Values | No special symbol attached to the number | 10<br>34 | |
| Binary Values | Begin with the letter “b” attached to the number | b1010<br>b0011 | |
| Numbers | Considered positive unless specifically noted as a negative value | 5<br>-10 | Voltage is often shown as positive: +3.3V |
| Blue Text | Linkable on-line | ...refer to Chapter 7, License | |
| Bold | Reference sources, paths, emphasis | ...see: **www.freescale.com/** | |

# Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference.

| | |
|---|---|
| **A/D** | Analog-to-Digital; a method of converting Analog signals to Digital values |
| **ADC** | Analog-to-Digital Converter; a peripheral on the 56F8367 part |
| **CAN** | Controller Area Network; serial communications peripheral and method |
| **CiA** | CAN in Automation; an international CAN user's group that coordinates standards for CAN communications protocols |
| **D/A** | Digital-to-Analog; a method of converting Digital values to an Analog form |
| **56F8367** | Controller with motor control peripherals |
| **EOnCE** | Enhanced On-Chip Emulation; a debug bus and port was created to enable a designer to create a low-cost hardware interface for a professional-quality debug environment |
| **EVM** | Evaluation Module; a hardware platform which allows a customer to evaluate the silicon and develop his application |
| **FlexCAN** | Flexable CAN Interface Module; a peripheral on the 56F8367 part |
| **GPIO** | General Purpose Input and Output port on Freescale's family of controllers; does not share pin functionality with any other peripheral on the chip and can only be set as an input, output or level-sensitive interrupt input |
| **IC** | Integrated Circuit |
| **JTAG** | Joint Test Action Group; a bus protocol/interface used for test and debug |
| **LED** | Light Emitting Diode |
| **LQFP** | Low-profile Quad Flat Package |
| **MPIO** | Multi-Purpose Input and Output port on Freescale's family of controllers; shares package pins with other peripherals on the chip and can function as a GPIO |
| **OnCE™** | On-Chip Emulation, a debug bus and port created to allow a means for low-cost hardware to provide a professional-quality debug environment |
| **PCB** | Printed Circuit Board |
| **PLL** | Phase Locked Loop |
| **PWM** | Pulse Width Modulation |
| **QuadDec** | Quadrature Decoder; a peripheral on the 56F8367 part |

| | |
|---|---|
| **RAM** | Random Access Memory |
| **R/C** | Resistor/Capacitor Network |
| **ROM** | Read-Only Memory |
| **SCI** | Serial Communications Interface; a peripheral on Freescale's family of controllers |
| **SPI** | Serial Peripheral Interface; a peripheral on Freescale's family of controllers |
| **SRAM** | Static Random Access Memory |
| **WS** | Wait State |

# References

The following sources were referenced to produce this manual:


[1] *DSP56800E Reference Manual*, DSP56800ERM, Freescale Semiconductor

[2] *56F8300 Peripheral User Manual*, MC56F8300UM, Freescale Semiconductor

[3] *56F8367 Technical Data*, MC56F8367, Freescale Semiconductor

[4] *CiA Draft Recommendation DR-303-1, Cabling and Connector Pin Assignment*, Version 1.0, CAN in Automation

[5] *CAN Specification 2.0B*, BOSCH or CAN in Automation

# Chapter 1
# Introduction

The 56F8367EVM is used to demonstrate the abilities of the 56F8367 controller and to provide a hardware tool allowing the development of applications.

The 56F8367EVM is an evaluation module board that includes a 56F8367 part, peripheral expansion connectors, a CAN interface, 512KB of external memory and a pair of daughter card connectors. The daughter card connectors are for signal monitoring and user feature expandability.

The 56F8367EVM is designed for the following purposes:

- Allowing new users to become familiar with the features of the 56800E architecture. The tools and examples provided with the 56F8367EVM facilitate evaluation of the feature set and the benefits of the family.
- Serving as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip or on-board RAM, run it, and debug it using a debugger via the JTAG/Enhanced OnCE (EOnCE) port. The breakpoint features of the EOnCE port enable the user to easily specify complex break conditions and to execute user-developed software at full speed until the break conditions are satisfied. The ability to examine and modify all user-accessible registers, memory and peripherals through the EOnCE port greatly facilitates the task of the developer.
- Serving as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the processor's peripherals. The EOnCE port's unobtrusive design means that all memory on the board and on the processor is available to the user.

## 1.1 56F8367EVM Architecture

The 56F8367EVM facilitates the evaluation of various features present in the 56F8367 part. The 56F8367EVM can be used to develop real-time software and hardware products. The 56F8367EVM provides the features necessary for a user to write and debug software, demonstrate the functionality of that software and interface with the user's application-specific device(s). The 56F8367EVM is flexible enough to allow a user to fully exploit the 56F8367's features to optimize the performance of his product, as shown in **Figure 1-1**.

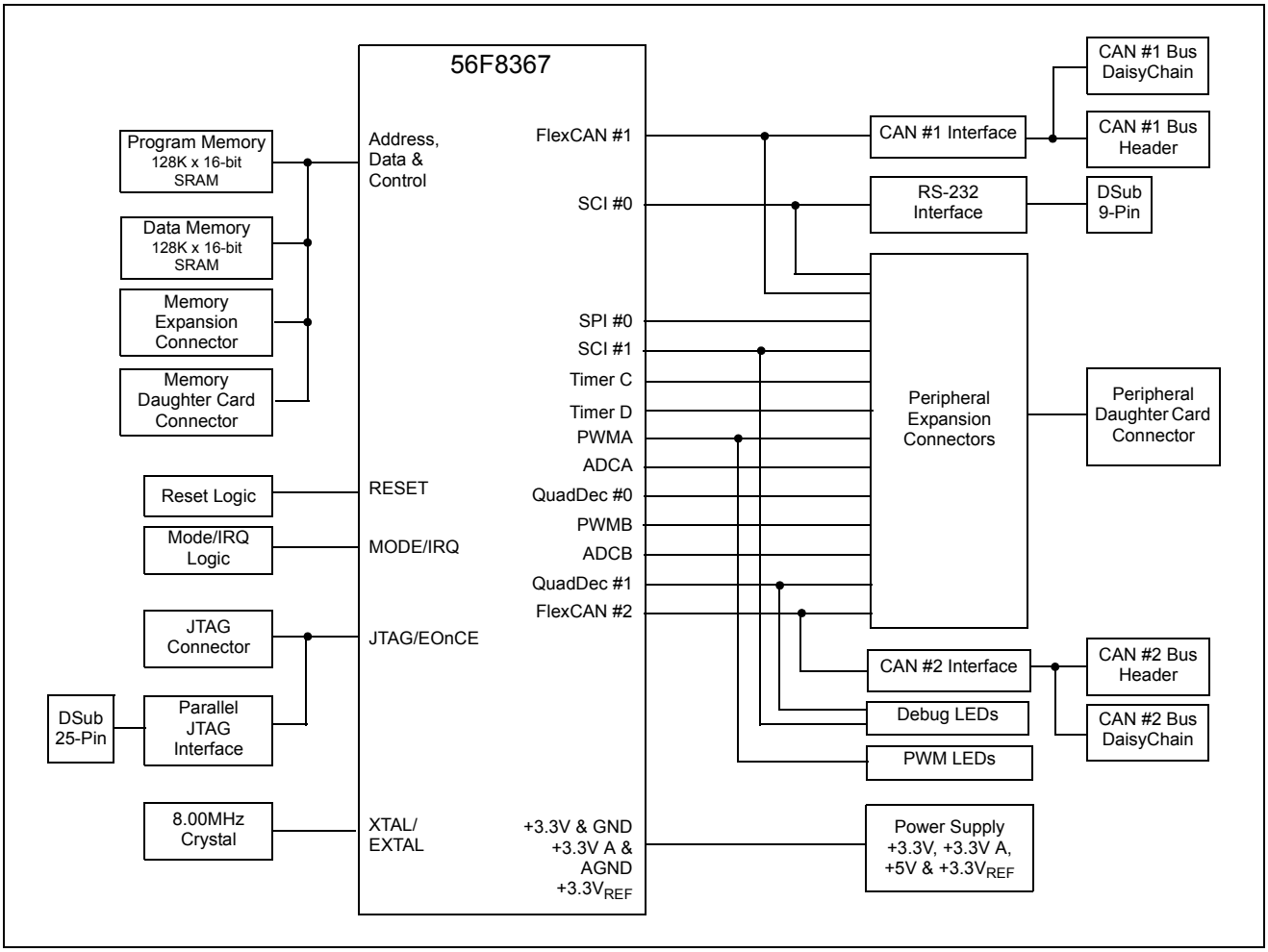


**Figure 1-1. Block Diagram of the 56F8367EVM**

## 1.2 56F8367EVM Configuration Jumpers

Ninteen jumper groups, (JG1-JG19), shown in **Figure 1-2**, are used to configure various features on the 56F8367EVM board. **Table 1-1** describes the default jumper group settings.

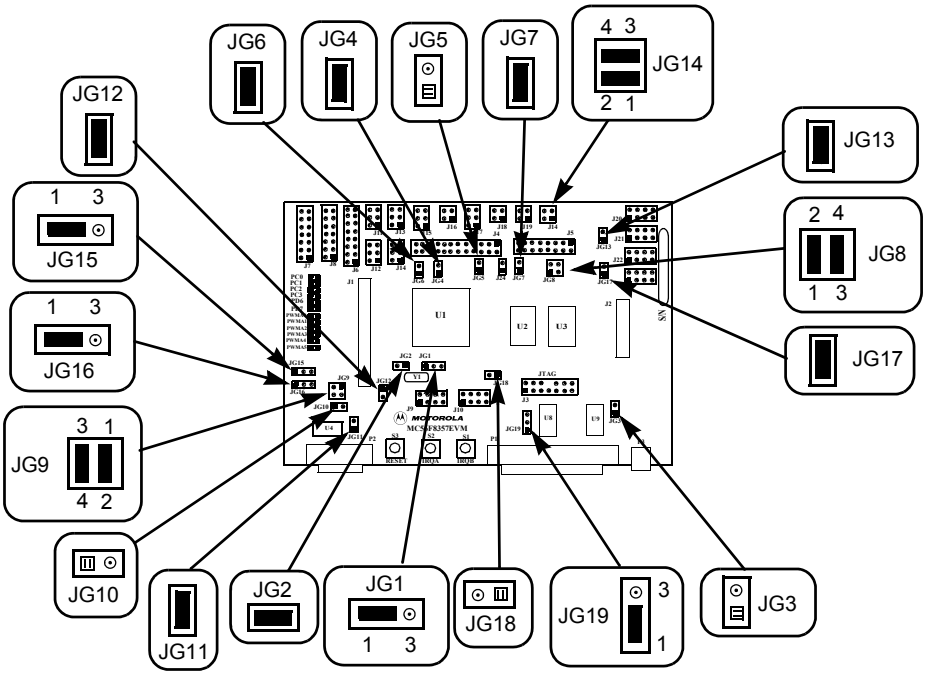


**Figure 1-2. MC56F8367 Default Jumper Options**

## Table 1-1. 56F8367EVM Default Jumper Options

| Jumper Group | Comment | Jumpers Connections |
|---|---|---|
| JG1 | Use on-board EXTAL crystal input for oscillator | 1–2 |
| JG2 | Use on-board XTAL crystal input for oscillator | 1–2 |
| JG3 | Enable on-board Parallel JTAG Host/Target Interface | NC |
| JG4 | Enable Internal Boot Mode | 1–2 |
| JG5 | Enable A0 - A23 for external memory accesses | NC |
| JG6 | Enable Crystal Mode | 1–2 |
| JG7 | Enable SRAM Memory Bank 0 (use CS0) | 1–2 |
| JG8 | Enable SRAM Memory Bank 1 (use CS1 & CS4) | 1–2 & 3–4 |
| JG9 | Pass RXD0 & TXD0 to RS-232 level converter | 1–2 & 3–4 |
| JG10 | Enable RS-232 output | NC |
| JG11 | Pass RS-232 RST to CTS | 1–2 |
| JG12 | Pass Temperature Diode to ANA7 | 1–2 |
| JG13 | CAN #1 termination selected | 1–2 |
| JG14 | Pass CAN2_TX & CAN2_RX to CAN tranceiver | 1–2 & 3–4 |
| JG15 | High selected on User Jumper #0 | 1–2 |
| JG16 | High selected on User Jumper #1 | 1–2 |
| JG17 | CAN2 termination selected | 1–2 |
| JG18 | Analog Ground to Digital Ground not reconnected | NC |
| JG19 | Use +3.3V for Printer Interface to on-board Parallel JTAG Host/Target | 1-2 |

## 1.3 56F8367EVM Connections

An interconnection diagram is shown in **Figure 1-3** for connecting the PC and the external +12.0V DC/AC power supply to the 56F8367EVM board.

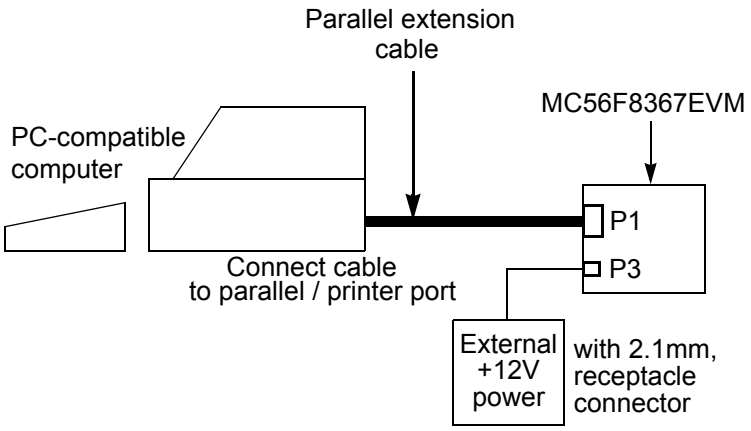


**Figure 1-3. Connecting the 56F8367EVM Cables**

Perform the following steps to connect the 56F8367EVM cables:

1. Connect the parallel extension cable to the parallel port of the host computer.
2. Connect the other end of the parallel extension cable to P1, shown in **Figure 1-3**, on the 56F8367EVM board. This provides the connection which allows the host computer to control the board.
3. Make sure that the external +12V DC, 1.2A power supply is not plugged into a +120V AC power source.
4. Connect the 2.1mm output power plug from the external power supply into P3, shown in **Figure 1-3**, on the 56F8367EVM board.
5. Apply power to the external power supply. The green Power-On LED, LED13, will illuminate when power is correctly applied.

# Chapter 2
# Technical Summary

The 56F8367EVM is designed as a versatile development card using the 56F8367 processor, allowing the creation of real-time software and hardware products to support a new generation of applications in servo and motor control, digital and wireless messaging, digital answering machines, feature phones, modems, and digital cameras. The power of the 16-bit 56F8367 processor, combined with the on-board 128K x 16-bit external Program/Data Static RAM (SRAM), 128K x 16-bit external Data/Program SRAM, RS-232 interface, CAN interface, daughter card interface, peripheral expansion connectors and parallel JTAG interface, makes the 56F8367EVM ideal for developing and implementing many motor controlling algorithms, as well as for learning the architecture and instruction set of the 56F8367 processor.

The main features of the 56F8367EVM, with board and schematic reference designators, include:

- MC56F8367VPY60, a 16-bit +3.3V/+2.5V controller operating at 60MHz [U1]
- External Fast Static RAM (FSRAM) memory, configured as:
  - 128K x 16-bit of memory [U2] with 0 wait state at 60MHz via CS0
  - 128K x 16-bit of memory [U3] with 0 wait state at 60MHz via CS1/CS4
- 8.00MHz crystal oscillator, for base processor frequency generation [Y1]
- Optional external oscillator frequency input connectors [JG1 and JG2]
- Joint Test Action Group (JTAG) port interface connector, for an external debug Host Target Interface [J3]
- On-board parallel JTAG host target interface, with a connector for a PC printer port cable [P1], including a disable jumper [JG3] and a printer port voltage selection jumper [JG19]
- RS-232 interface, for easy connection to a host processor [U4 and P2], including a disable jumper [JG10]
- RTS and CTS RS-232 control signal access [JG11]
- CAN interface, for high speed, 1.0Mbps, FlexCAN communications [U10 and J20]
- CAN bypass and bus termination [J21 and JG13]

- CAN #2 interface, for high speed, 1.0Mbps, FlexCAN communications [U11 and J22]
- CAN #2 bypass and bus termination [J23 and JG17]
- CAN #2 interface signal isolation [JG14]
- Peripheral Daughter Card connector, to allow the user to connect his own SCI, SPI or GPIO-compatible peripheral to the controller [J1]
- Memory Daughter Card connector, to allow the user to connect his own memory or memory device to the device [J2]
- SCI #0 expansion connector, to allow the user to connect his own SCI #0 / MPIO-compatible peripheral [J13]
- SCI #1 expansion connector, to allow the user to connect his own SCI #1 / MPIO-compatible peripheral [J14]
- SPI #0 expansion connector, to allow the user to connect his own SPI #0 / MPIO-compatible peripheral [J11]
- SPI #1 expansion connector, to allow the user to connect his own SPI #1 / MPIO-compatible peripheral [J12]
- PWMA expansion connector, to allow the user to connect his own PWMA-compatible peripheral [J7]
- PWMB expansion connector, to allow the user to connect his own PWMB-compatible peripheral [J8]
- CAN #1 expansion connector, to allow the user to connect his own CAN physical layer peripheral [J18]
- CAN #2 expansion connector, to allow the user to connect his own CAN physical layer peripheral [J19]
- Timer A expansion connector, to allow the user to connect his own Timer A / Encoder #0-compatible peripheral [J15]
- Timer C expansion connector, to allow the user to connect his own Timer C-compatible peripheral [J16]
- Timer D expansion connector, to allow the user to connect his own Timer D-compatible peripheral [J17]
- ADC A expansion connector, to allow the user to attach his own A/D Port A-compatible peripheral [J9]
- ADC B expansion connector, to allow the user to attach his own A/D Port B-compatible peripheral [J10]

- Address bus expansion connector, to allow the user to monitor the external address bus [J4]
- Data bus expansion connector, to allow the user to monitor the external data bus [J5]
- External memory bus control signal connector, to allow the user to monitor the external memory bus [J6]
- On-board power regulation provided from an external +12V DC-supplied power input [P3]
- Light Emitting Diode (LED) power indicator [LED13]
- Six on-board real-time user debugging LEDs [LED1 - 6]
- Six on-board Port A PWM monitoring LEDs [LED7 - 12]
- Internal/external (EXTBOOT) boot mode selector [JG4]
- Address range (EMI_MODE) boot mode selector [JG5]
- Clock mode (CLKMODE) boot selector [JG6]
- Temperature sense diode to ANA7 selector [JG12]
- Manual reset push button [S1]
- Manual interrupt push button for $\overline{\text{IRQA}}$ [S2]
- Manual interrupt push button for $\overline{\text{IRQB}}$ [S3]
- General-purpose jumper on GPIO PE4 [JG15]
- General-purpose jumper on GPIO PE7 [JG16]

## 2.1 MC56F8367

The 56F8367EVM uses a Freescale MC56F8367VPY60 part, designated as U1 on the board and in the schematics. This part will operate at a maximum external bus speed of 60MHz. A full description of the 56F8367, including functionality and user information, is provided in these documents:

- 56F8367 *Technical Data Sheet*, (MC56F8367)**:** Electrical and timing specifications, pin descriptions, device-specific peripheral information and package descriptions (this document)
- *56F8300 Peripheral User Manual*, (MC56F8300UM): Detailed description of peripherals of the 56F8300 family of devices
- *DSP56800E Reference Manual*, (DSP56800ERM): Detailed description of the 56800E family architecture, 16-bit core processor, and the instruction set

Refer to these documents for detailed information about chip functionality and operation. They can be found on this URL:

**www.freescale.com**

## 2.2 Program and Data Memory

The 56F8367EVM contains two 128K x 16-bit Fast Static RAM banks. SRAM bank 0 is controlled by CS0 and SRAM bank 1 is controlled by CS1 and CS4. This provides a total of 256K x 16 bits of external memory.

### 2.2.1 SRAM Bank 0

SRAM bank 0, which is controlled by CS0, uses a 128K x 16-bit Fast Static RAM (GSI GS72116, labeled U2) for external memory expansion; see the FSRAM schematic diagram in **Figure 2-1**. CS0 can be configured to use this memory bank as 16 bits of Program memory, Data memory, or both. Additionally, CS0 can be configured to assign this memory's size and starting address to any modulo address space.

This memory bank will operate with zero wait state access while the 56F8367 is running at 60MHz and can be disabled by removing the jumper at JG7.

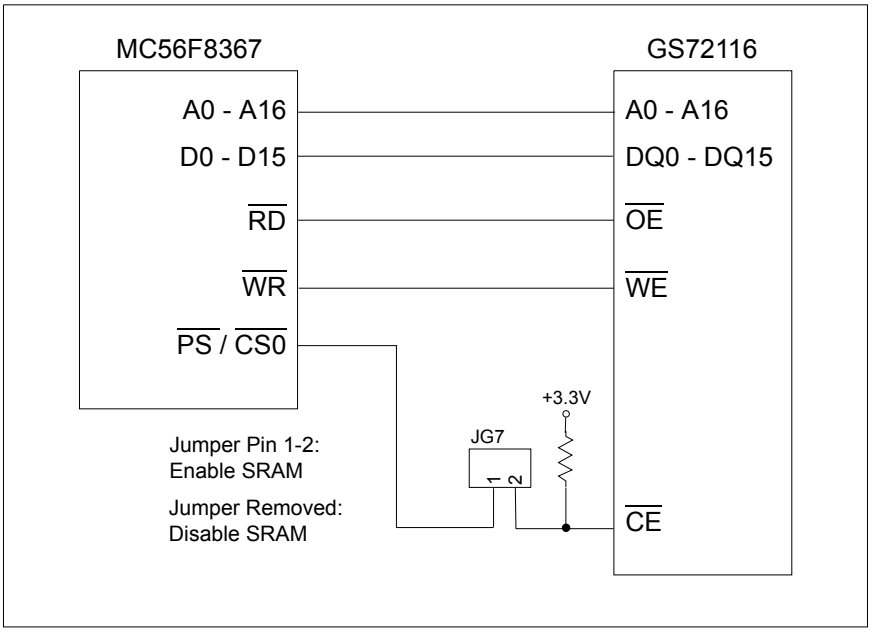


**Figure 2-1. Schematic Diagram of the External CS0 Memory Interface**

### 2.2.2 SRAM Bank 1

SRAM bank 1, which is controlled by CS1 and CS2, uses a 128K x 16-bit Fast Static RAM (GSI GS72116, labeled U3) for external memory expansion; see the FSRAM schematic diagram in **Figure 2-2**. Using CS1 and CS4, this memory bank can be configured as byte (8-bit) or word (16-bit) accessable Program memory, Data memory, or both. Additionally, CS1 and CS4 can be configured to assign this memory's size and starting address to any modulo address space.

This memory bank will operate with zero wait state access while the 56F8367 is running at 60MHz and can be disabled by removing the jumpers at JG8.

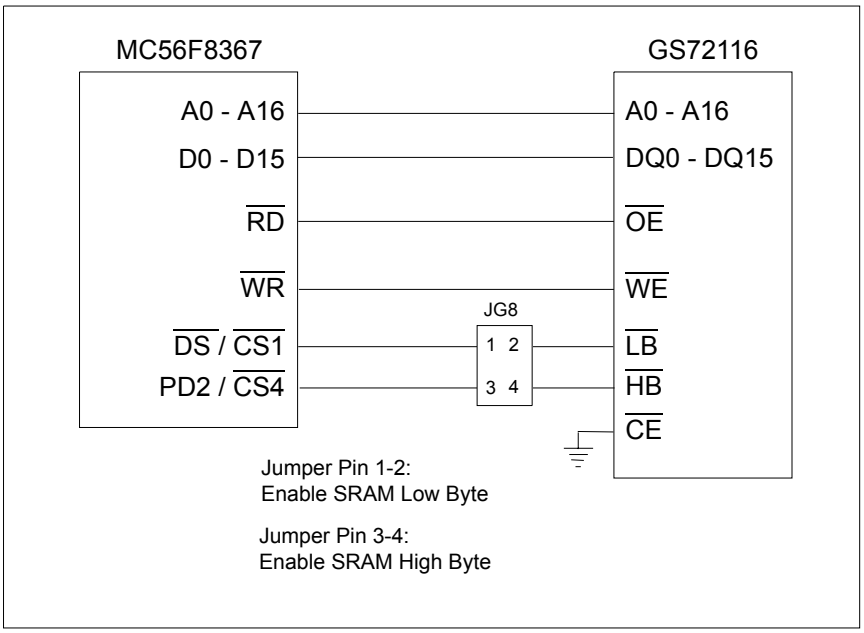


**Figure 2-2. Schematic Diagram of the External CS1 / CS4 Memory Interface**

## 2.3 RS-232 Serial Communications

The 56F8367EVM provides an RS-232 interface by the use of an RS-232 level converter, Maxim MAX3245EEAI, designated as U4. Refer to the RS-232 schematic diagram in **Figure 2-3**. The RS-232 level converter transitions the SCI port's +3.3V signal levels to RS-232-compatible signal levels and connects to the host's serial port via connector P2. RTS/CTS flow control is provided on JG11 as a jumper, but could be implemented using uncommitted GPIO signals. The SCI port #0 signals can be isolated from the RS-232 level converter by removing the jumpers in JG9; see **Table 2-1**. The pin-out of connector P2 is listed in **Table 2-2**. The RS-232 level converter/transceiver can be disabled by placing a jumper at JG10.

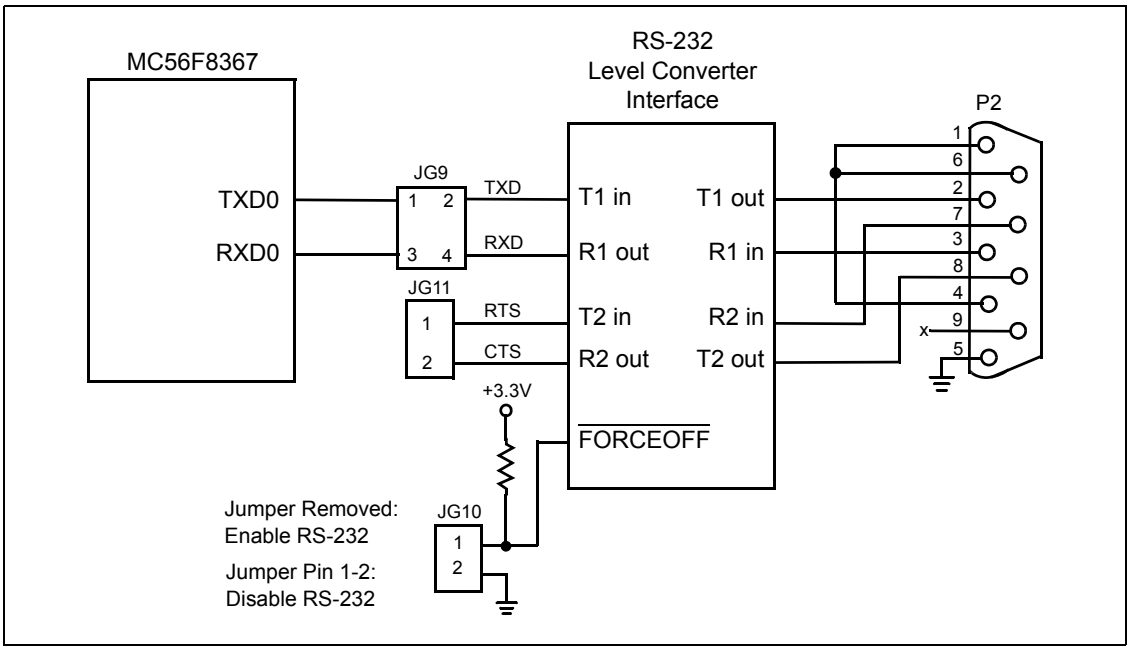


**Figure 2-3. Schematic Diagram of the RS-232 Interface**

**Table 2-1. SCI #0 Jumper Options**

| JG9 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TXD0 | 2 | RS-232 TXD |
| 3 | RXD0 | 4 | RS-232 RXD |

**Table 2-2. RS-232 Serial Connector Description**

| P2 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | Jumper to 6 & 4 | 6 | Jumper to 1 & 4 |
| 2 | TXD | 7 | CTS |
| 3 | RXD | 8 | RTS |
| 4 | Jumper to 1 & 6 | 9 | NC |
| 5 | GND | | |

## 2.4 Clock Source

The 56F8367EVM uses an 8.00MHz crystal, Y1, connected to its external crystal inputs, EXTAL and XTAL. To achieve its maximum internal operating frequency, the 56F8367 uses its internal PLL to multiply the input frequency. An external oscillator source can be connected to the processor by using the oscillator bypass connectors, JG1 and JG2; see **Figure 2-4**. If the input frequency is above 8MHz, then the EXTAL input should be jumpered to ground by adding a jumper between JG1 pins 2 and 3. The input frequency would then be injected on JG2's pin 2. If the input frequency is below 4MHz, then the input frequency can be injected on JG1's pin 2.

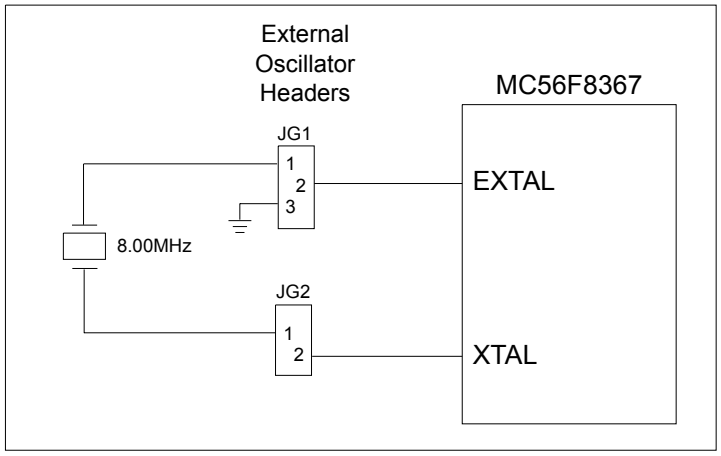


**Figure 2-4. Schematic Diagram of the Clock Interface**

## 2.5 Operating Mode

The 56F8367EVM provides three boot mode selection jumpers, EXTBOOT, EMI_MODE and CLKMODE, to provide boot-up mode options.

### 2.5.1 EXTBOOT

The 56F8367EVM provides an external/internal boot mode jumper, JG4. This jumper is used to select the internal or external memory operation of the processor as it exits reset. Refer to the **56F8300 Peripheral User Manual** and the **56F8367 Technical Data Sheet** for a complete description of the chip's operating modes. **Table 2-3** shows the two external boot operation modes available on the 56F8367.

**Table 2-3. EXTBOOT Operating Mode Selection**

| Operating Mode | JG4 | Comment |
|---|---|---|
| 0 | 1 - 2 | Bootstrap from internal memory (GND) |
| 3 | No Jumper | Bootstrap from external memory (+3.3V) |

### 2.5.2 EMI_MODE

The 56F8367EVM provides an EMI boot mode jumper, JG5. This jumper is used to select the external memory addressing range operating mode of the processor as it exits reset. The user can select between a 64K address space or an 8M address space. Refer to the **56F8300 Peripheral User Manual** and the **56F8367 Technical Data Sheet** for a complete description of the chip's operating modes. **Table 2-4** shows the two EMI operation modes available on the 56F8367.

**Table 2-4. EMI Operating Mode Selection**

| Operating Mode | JG5 | Comment |
|---|---|---|
| V1 | 1 - 2 | A0 - A15 (64K) available for external memory bus (GND) |
| V2 | No Jumper | A0 - A23 (8M) available for external memory bus (+3.3V) |

### 2.5.3 CLKMODE

The 56F8367EVM provides a clock boot mode jumper, JG6. This jumper is used to select the type of clock source being provided to the processor as it exits reset. The user can select between the use of a crystal or an oscillator as the clock source for the processor. Refer to the **56F8300 Peripheral User Manual** and the **56F8367 Technical Data Sheet** for a complete description of the chip's operating modes. **Table 2-5** shows the two CLKMODE operation modes available on the 56F8367.

**Table 2-5. EMI Operating Mode Selection**

| Operating Mode | JG6 | Comment |
|---|---|---|
| Crystal | 1 - 2 | Enables the external clock drive logic so an external crystal can be used as the input clock source. (GND) |
| Oscillator | No Jumper | Disables the external clock drive logic. Use oscillator input on XTAL and Ground on EXTAL. (3.3V) |

## 2.6 Debug LEDs

Six on-board Light Emitting Diodes, (LEDs), are provided to allow real-time debugging for user programs. These LEDs will allow the programmer to monitor program execution without having to stop the program during debugging; refer to **Figure 2-5**. **Table 2-6** describes the control of each LED.

**Table 2-6. LED Control**

| | Controlled by | |
|---|---|---|
| **User LED** | **Color** | **Signal** |
| LED1 | RED | Port C Bit 0 (PC0) |
| LED2 | YELLOW | Port C Bit 1 (PC1) |
| LED3 | GREEN | Port C Bit 2 (PC2) |
| LED4 | RED | Port C Bit 3 (PC3) |
| LED5 | YELLOW | Port D Bit 6 (PD6) |
| LED6 | GREEN | Port D Bit 7 (PD7) |

Setting PC0, PC1, PC2, PC3, PD6, or PD7 to a Logic One value will turn on the associated LED.

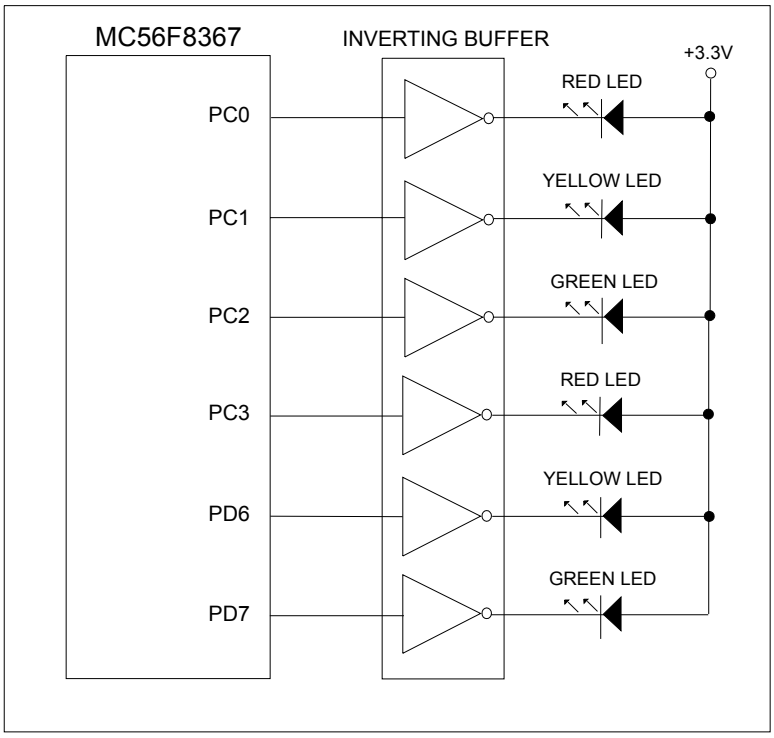


**Figure 2-5. Schematic Diagram of the Debug LED Interface**

## 2.7 Debug Support

The 56F8367EVM provides an on-board parallel JTAG host target interface and a JTAG interface connector for external target interface support. Two interface connectors are provided to support each of these debugging approaches. These two connectors are designated the JTAG connector and the host parallel interface connector.

### 2.7.1 JTAG Connector

The JTAG connector on the 56F8367EVM allows the connection of an external host target interface for downloading programs and working with the 56F8367's registers. This connector is used to communicate with an external host target interface, which passes information and data back and forth with a host processor running a debugger program. **Table 2-7** shows the pin-out for this connector.

**Table 2-7. JTAG Connector Description**

| J3 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TDI | 2 | GND |
| 3 | TDO | 4 | GND |
| 5 | TCK | 6 | GND |
| 7 | NC | 8 | KEY |
| 9 | $\overline{\text{RESET}}$ | 10 | TMS |
| 11 | +3.3V | 12 | NC |
| 13 | $\overline{\text{DE}}$ | 14 | $\overline{\text{TRST}}$ |

When this connector is used with an external host target interface, the parallel JTAG interface should be disabled by placing a jumper in jumper block JG3. Reference **Table 2-8** for this jumper's selection options.

**Table 2-8. Parallel JTAG Interface Disable Jumper Selection**

| JG3 | Comment |
|---|---|
| No jumpers | Enables On-board Parallel JTAG Interface |
| 1 - 2 | Disables on-board Parallel JTAG Interface |

## 2.7.2 Parallel JTAG Interface Connector

The Parallel JTAG Interface Connector, P1, allows the 56F8367 to communicate with a parallel printer port on a Windows PC; reference **Figure 2-6**. Using this connector, the user can download programs and work with the 56F8367's registers. **Table 2-9** shows the pin-out for this connector. When using the parallel JTAG interface, the jumper at JG3 should be removed, as shown in **Table 2-8**. The printer port interface voltage of +3.3V or +5.0V can be selected by a jumper on JG19, as shown in **Table 2-10**.

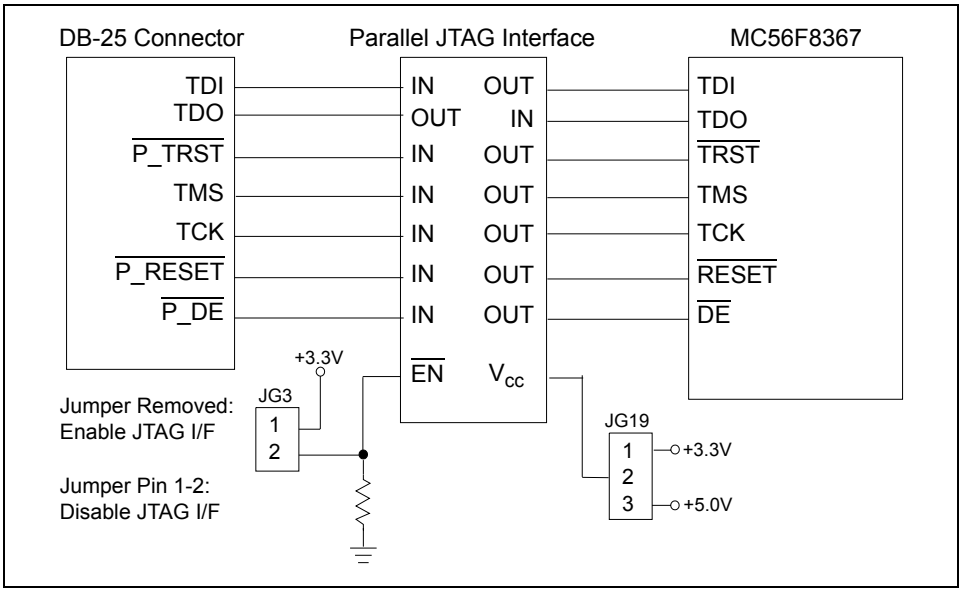


**Figure 2-6. Block Diagram of the Parallel JTAG Interface**

## Table 2-9. Parallel JTAG Interface Connector Description

| P1 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | NC | 14 | NC |
| 2 | PORT_RESET | 15 | PORT_IDENT |
| 3 | PORT_TMS | 16 | NC |
| 4 | PORT_TCK | 17 | NC |
| 5 | PORT_TDI | 18 | GND |
| 6 | $\overline{\text{PORT\_TRST}}$ | 19 | GND |
| 7 | $\overline{\text{PORT\_DE}}$ | 20 | GND |
| 8 | PORT_IDENT | 21 | GND |
| 9 | PORT_VCC | 22 | GND |
| 10 | NC | 23 | GND |
| 11 | PORT_TDO | 24 | GND |
| 12 | NC | 25 | GND |
| 13 | PORT_CONNECT | | |

## Table 2-10. Parallel JTAG Interface Voltage Jumper Selection

| JG19 | Comment |
|---|---|
| 1 - 2 | Interface with the PC's printer port using +3.3V signals |
| 2 - 3 | Interface with the PC's printer port using +5.0V signals |

## 2.8 External Interrupts

Two on-board push button switches are provided for external interrupt generation, as shown in **Figure 2-7**. S2 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQA}}$. S3 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQB}}$. These two switches allow the user to generate interrupts for his user-specific programs.

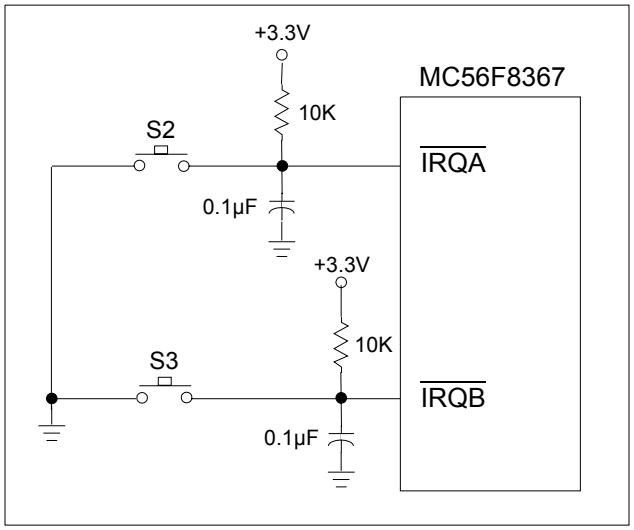


**Figure 2-7. Schematic Diagram of the User Interrupt Interface**

## 2.9 Reset

Logic is provided on the 56F8367 to generate an internal power-on reset. Additional reset logic is provided to support the reset signals from the JTAG connector, the parallel JTAG interface and the user reset push button, S1; refer to **Figure 2-8**.

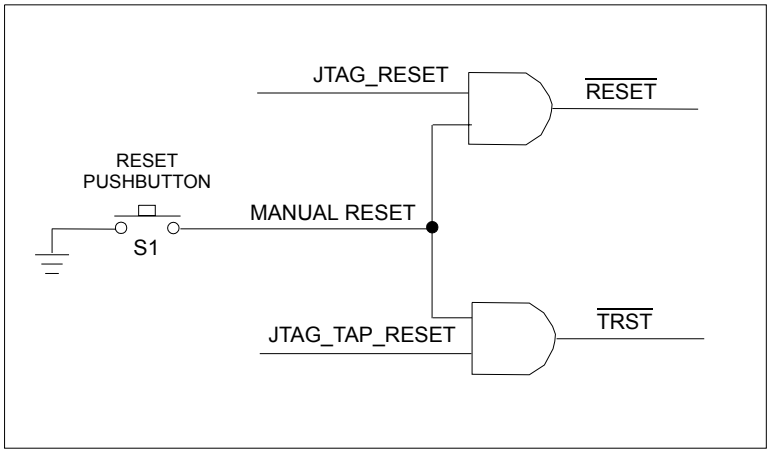


**Figure 2-8. Schematic Diagram of the Reset Interface**

## 2.10 Power Supply

The main power input to the 56F8367EVM, +12V DC at 1.2A, is through a 2.1mm coax power jack. This input power is rectified to provide a DC supply input. This allows a user the option to use a +12V AC power supply. A 1.2 Amp power supply is provided with the 56F8367EVM; however, less than 500mA is required by the EVM. The remaining current is available for custom control applications when connected to the daughter card connectors. The 56F8367EVM provides +5.0V DC regulation for the CAN interface and additional regulators. The 56F8367EVM provides +3.3V DC voltage regulation for the processor, memory, D/A, ADC, parallel JTAG interface and supporting logic; refer to **Figure 2-9**. Additional voltage regulation logic provides a low-noise +3.3V DC voltage reference to the processor's A/D $V_{REFH}$. A jumper, JG18, and resistor, R66, are provided to allow the analog and digital grounds to be isolated on the 56F8367EVM board. This allows the analog ground reference point to be provided on a custom board attached to the 56F8367EVM daughter card connectors. By removing R66, the AGND reference is disconnected from the 56F8367EVM's digital ground. By placing a jumper on JG18, the AGND is reconnected to the 56F8367EVM's digital ground. Power applied to the 56F8367EVM is indicated with a power-on LED, referenced as LED13. Optionally, the user can provide the +2.5 DC voltage needed by the processor's core on connector J24 and disable the on-chip core voltage regulator by moving the resistor at R72 to R71. Additonally, four zero ohm resistors or shorting wires must be added at R67, R68, R69, and R70 to allow the external +2.5V DC to pass to the 56F8367.

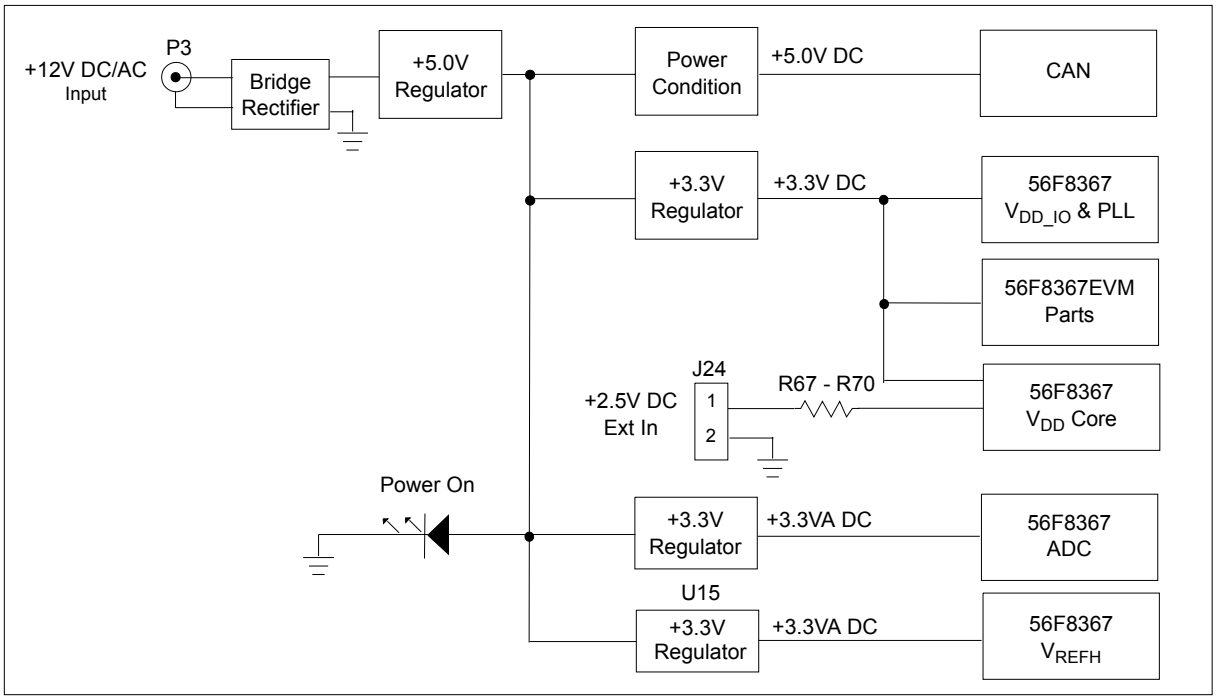


**Figure 2-9. Schematic Diagram of the Power Supply**

## 2.11 Daughter Card Connectors

The EVM board contains two daughter card connectors. One connector, J1, contains the processor's peripheral port signals. The second connector, J2, contains the processor's external memory bus signals.

### 2.11.1 Peripheral Daughter Card Connector

The processor's peripheral port signals are connected to the peripheral daughter card connector, J1. The peripheral daughter card connector is used to connect a daughter card or a user-specific daughter card to the processor's peripheral port signals. The peripheral port daughter card connector is a 100-pin high-density connector with signals for the IRQs, reset, SPI, SCI, PWM, ADC and Quad Timer ports. **Table 2-11** shows the peripheral daughter card connector's signal-to-pin assignments.

**Table 2-11. Peripheral Daughter Card Connector Description**

| J1 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | +12V | 2 | +12V |
| 3 | GND | 4 | GND |
| 5 | +5.0V | 6 | +5.0V |
| 7 | GND | 8 | GND |
| 9 | +3.3V | 10 | +3.3V |
| 11 | GND | 12 | GND |
| 13 | PHASEA0 / TA0 / PC4 | 14 | PHASEB0 / TA1 / PC5 |
| 15 | INDEX0 / TA2 / PC6 | 16 | HOME0 / TA3 / PC7 |
| 17 | GND | 18 | GND |
| 19 | PHASEA1 / PC0 / TB0 / SCLK1 | 20 | PHASEB1 / PC1 / TB1 / MOSI1 |
| 21 | INDEX1 / PC2 / TB2 / MISO1 | 22 | HOME1 / PC3 / TB3 / $\overline{SS1}$ |
| 23 | TXD0 / PE0 | 24 | TXD1 / PD6 |
| 25 | TXD0 / PE0 | 26 | TXD1 / PD6 |
| 27 | RXD0 / PE1 | 28 | RXD1 / PD7 |

## Table 2-11. Peripheral Daughter Card Connector Description (Continued)

| J1 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 29 | $\overline{\text{IRQA}}$ | 30 | $\overline{\text{IRQB}}$ |
| 31 | RXD0 / PE1 | 32 | RXD1 / PD7 |
| 33 | PWMB0 | 34 | PWMB1 |
| 35 | PWMB2 | 36 | PWMB3 |
| 37 | PWMB4 | 38 | PWMB5 |
| 39 | GND | 40 | GND |
| 41 | ISB0 / PD10 | 42 | ISB1 / PD11 |
| 43 | ISB2 / PD12 | 44 | GND |
| 45 | FAULTB1 | 46 | FAULTB0 |
| 47 | FAULTB3 | 48 | FAULTB2 |
| 49 | GND | 50 | GND |
| 51 | PWMA0 | 52 | PWMA1 |
| 53 | PWMA2 | 54 | PWMA3 |
| 55 | PWMA4 | 56 | PWMA5 |
| 57 | GND | 58 | GND |
| 59 | FAULTA0 | 60 | FAULTA1 |
| 61 | FAULTA2 | 62 | MISO0 / PE6 |
| 63 | ISA0 / PC8 | 64 | ISA1 / PC9 |
| 65 | ISA2 / PC10 | 66 | $\overline{\text{RSTO}}$ |
| 67 | MOSI0 / PE5 | 68 | $\overline{\text{SS0}}$ / PE7 |
| 69 | TD0 / PE10 | 70 | TD1 / PE11 |
| 71 | SCLK0 / PE7 | 72 | TC0 / PE8 |
| 73 | CAN_TX | 74 | CAN_RX |
| 75 | MOSI0 / PE5 | 76 | MISO0 / PE6 |
| 77 | SCLK0 / PE4 | 78 | $\overline{\text{SS0}}$ / PE7 |
| 79 | GND | 80 | GND |

**Table 2-11. Peripheral Daughter Card Connector Description (Continued)**

| J1 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 81 | $+V_{REFH}$ | 82 | $+V_{REFH}$ |
| 83 | GNDA | 84 | GNDA |
| 85 | AN0 | 86 | AN1 |
| 87 | AN2 | 88 | AN3 |
| 89 | AN4 | 90 | AN5 |
| 91 | AN6 | 92 | AN7 |
| 93 | AN8 | 94 | AN9 |
| 95 | AN10 | 96 | AN11 |
| 97 | AN12 | 98 | AN13 |
| 99 | AN14 | 100 | AN15 |

## 2.11.2 Memory Daughter Card Connector

The processor's external memory bus signals are connected to the memory daughter card connector, J2. **Table 2-12** shows the port signal-to-pin assignments.

**Table 2-12. Memory Daughter Card Connector Description**

| J2 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | A4 / PA12 | 2 | A5 / PA13 |
| 3 | A3 / PA11 | 4 | A6 / PE2 |
| 5 | A2 / PA10 | 6 | A7 / PE3 |
| 7 | A1 / PA9 | 8 | $\overline{RD}$ |
| 9 | GND | 10 | GND |
| 11 | A0 / PA8 | 12 | $\overline{DS}$ / $\overline{CS1}$ |
| 13 | $\overline{PS}$ / $\overline{CS0}$ | 14 | PD0 / $\overline{CS2}$ / CAN2_TX |

## Table 2-12. Memory Daughter Card Connector Description (Continued)

| J2 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 15 | D0 / PF9 | 16 | D15 / PF8 |
| 17 | D1 / PF10 | 18 | D14 / PF7 |
| 19 | GND | 20 | GND |
| 21 | GND | 22 | GND |
| 23 | D2 / PF11 | 24 | D13 / PF6 |
| 25 | D3 / PF12 | 26 | D12 / PF5 |
| 27 | D4 / PF13 | 28 | D11 / PF4 |
| 29 | D5 / PF14 | 30 | D10 / PF3 |
| 31 | GND | 32 | GND |
| 33 | GND | 34 | GND |
| 35 | D6 / PF15 | 36 | D9 / PF2 |
| 37 | D7 / PF0 | 38 | D8 / PF1 |
| 39 | $\overline{WR}$ | 40 | PD1 / $\overline{CS3}$ / CAN2_RX |
| 41 | A15 / PA7 | 42 | A8 / PA0 |
| 43 | GND | 44 | GND |
| 45 | A14 / PA6 | 46 | A9 / PA1 |
| 47 | A13 / PA5 | 48 | A10 / PA2 |
| 49 | A12 / PA4 | 50 | A11 / PA3 |
| 51 | PB0 / A16 | 52 | GND |
| 53 | GND | 54 | GND |
| 55 | +3.3V | 56 | +3.3V |
| 57 | GND | 58 | GND |
| 59 | +5.0V | 60 | +5.0V |

## 2.12 Motor Control PWM Signals and LEDs

The 56F8367 has two independent groups of dedicated PWM units. Each unit contains six PWM, three phase current sense inputs and four fault input lines. PWM group A's PWM lines are connected to a set of six PWM LEDs via inverting buffers. The buffers are used to isolate and drive the Processor's PWM group A's outputs to the PWM LEDs. The PWM LEDs indicate the status of PWM group A signals; refer to **Figure 2-10**. PWM Group A and B signals are routed out to headers, J7 and J8 respectively, and to the peripheral daughter card connector for easy use by the end user.

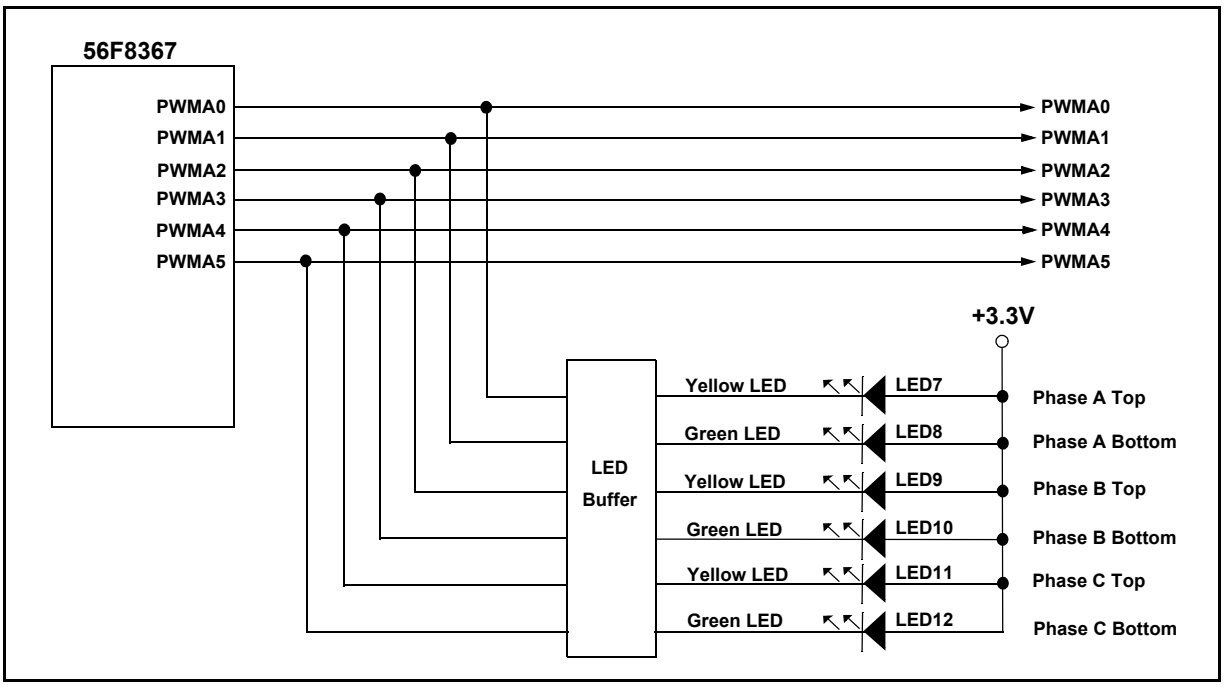


**Figure 2-10. PWM Group A Interface and LEDs**

## 2.13 CAN Interfaces

The 56F8367EVM board contains two FlexCAN interfaces. The primary CAN interface uses the CAN1_RX and CAN1_TX pins on the 56F8367. The secondary CAN interface uses the CAN2_RX and CAN2_TX pins on the 56F8367.

### 2.13.1 FlexCAN #1 Interface

The 56F8367EVM board contains a CAN physical-layer interface chip that is attached to the FlexCAN port's CAN1_RX and CAN1_TX pins on the 56F8367. The EVM board uses a Phillips high-speed, 1.0Mbps, physical layer interface chip, PCA82C250. Due to the +5.0V operating voltage of the CAN interface chip, a pull-up to +5.0V is required to level shift the transmit data output line from the 56F8367. The CANH and CANL signals pass through inductors before attaching to the CAN bus connectors. A primary, J20, and daisy-chain, J21, CAN connector are provided to allow easy daisy-chaining of CAN devices. CAN bus termination of 120 ohms can be provided by adding a jumper to JG13. Refer to **Table 2-14** for the CAN connector signals and **Figure 2-12** for a connection diagram.

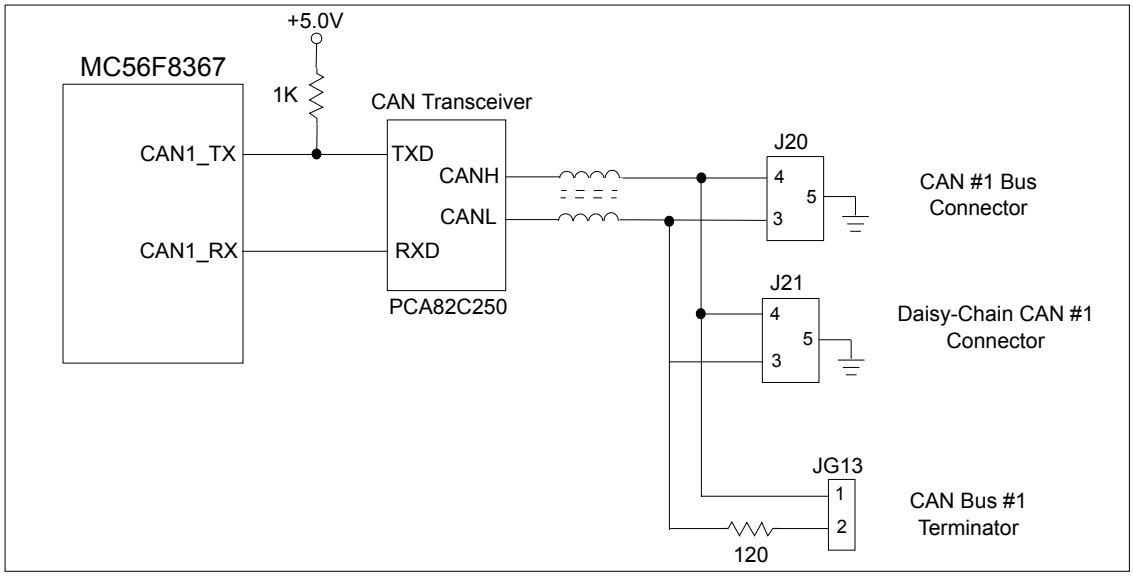


**Figure 2-11. CAN #1 Interface**

**Table 2-13. CAN #1 Header Description**

| J20 and J21 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | NC | 2 | NC |
| 3 | CANL | 4 | CANH |
| 5 | GND | 6 | NC |
| 7 | NC | 8 | NC |
| 9 | NC | 10 | NC |

## 2.13.2 FlexCAN #2 Interface

The 56F8367EVM board contains a second FlexCAN port, the CAN2_RX and CAN2_TX pins on the 56F8367. These signals pass through an isolation jumper, JG14, before going to the CAN physical layer interface. The EVM board uses a Phillips high-speed, 1.0Mbps, physical layer interface chip, PCA82C250. Due to the +5.0V operating voltage of the CAN interface chip, a pull up to +5.0V is required to level shift the transmit data output line from the 56F8367. The CAN2H and CAN2L signals pass through inductors before attaching to the CAN bus connectors. A primary, J22, and daisy-chain, J23, CAN connector are provided to allow easy daisy-chaining of CAN devices. CAN bus termination of 120 ohms can be provided by adding a jumper to JG17. Refer to **Figure 2-12** for a connection diagram and to **Table 2-14** and **Table 2-15** for the CAN connector signals.

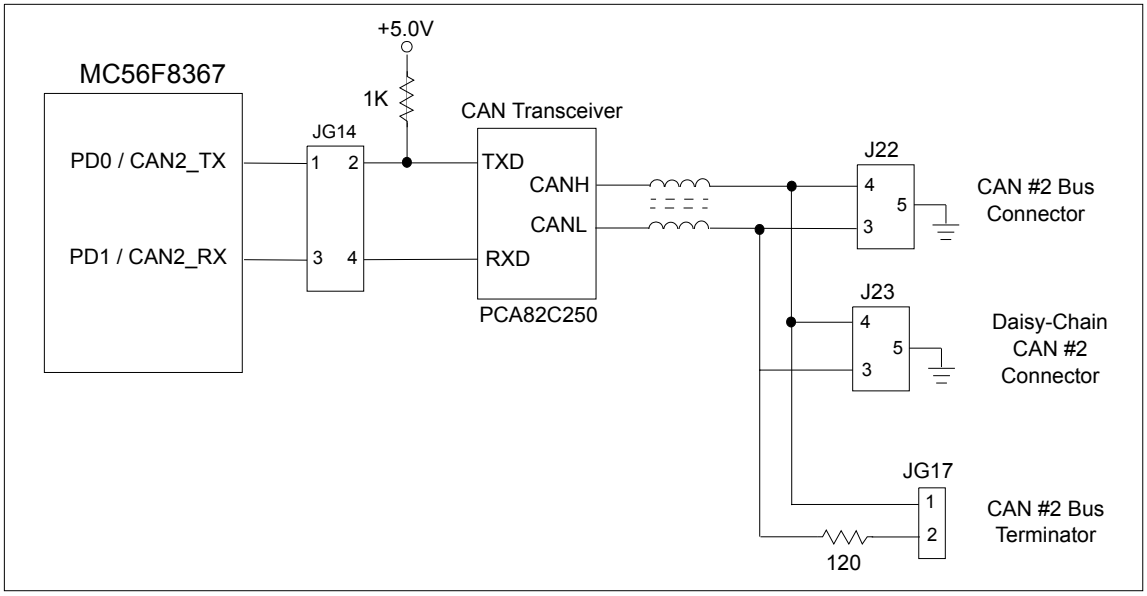


**Figure 2-12. CAN #2 Interface**

## Table 2-14. CAN #2 Header Description

| J22 and J23 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | NC | 2 | NC |
| 3 | CAN2L | 4 | CAN2H |
| 5 | GND | 6 | NC |
| 7 | NC | 8 | NC |
| 9 | NC | 10 | NC |

## Table 2-15. CAN #2 Pass-Through Jumper Description

| JG14 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | PD0 | 2 | CAN2_TX |
| 3 | PD1 | 4 | CAN2_RX |

## 2.14 Software Feature Jumpers

The 56F8367EVM board contains two software feature jumpers that allow the user to select user-defined software features. Two GPIO port pins, PE4 and PE7, are pulled high or low with 10K ohm resistors on JG15 and JG16. Attaching a jumper between pins 1 and 2 will place a high or 1 on the port pin. Attaching a jumper between pins 2 and 3 will place a low or 0 on the port pin; see **Figure 2-13**.

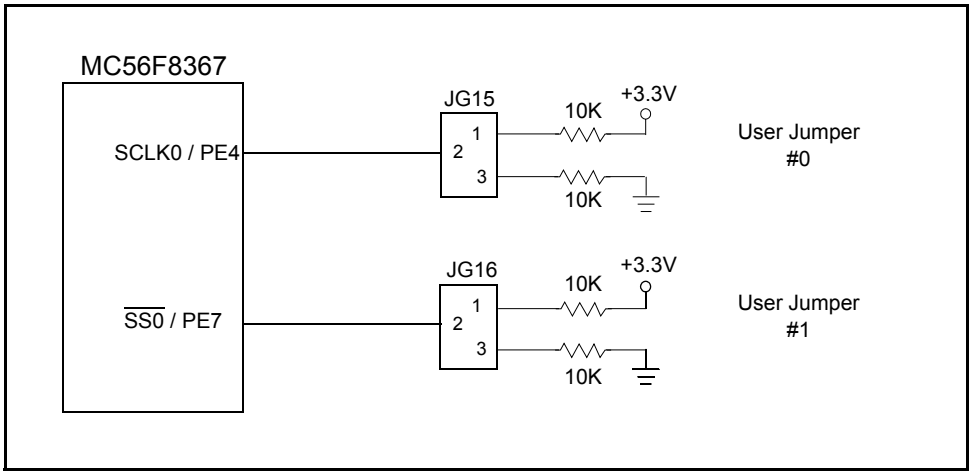


**Figure 2-13. Software Feature Jumpers**

## 2.15 Peripheral Expansion Connectors

The EVM board contains a group of peripheral expansion connectors used to gain access to the resources of the 56F8367. The following signal groups have expansion connectors:

- External Memory Address Bus (A0 - A23)
  General Purpose Port A (bits 0 - 13)
  General Purpose Port E (bits 2 & 3)
  General Purpose Port B (bit 0 - 7)
- External Memory Data Bus (D0 - D15)
  General Purpose Port F (bits 0 - 15)
- External Memory Control
  General Purpose Port D (bits 0 - 5, 8 & 9)
- Quadrature Decoder #0
  Quad Timer Channel A
- Quadrature Decoder #1
  Serial Peripheral Interface Port #1
  Quad Timer Channel B
  General Purpose Port C (bits 0 - 3)
- Quad Timer Channel C
  General Purpose Port E (bits 8 & 9)
- Quad Timer Channel D
  General Purpose Port E (bits 10 - 13)
- A/D Input Port A
- A/D Input Port B
- Serial Communications Port #0 / General Purpose Port E (bits 0 and 1)
- Serial Communications Port #1 / General Purpose Port D (bits 6 and 7)
- Serial Peripheral Interface Port #0 / General Purpose Port E (bits 4 - 7)
- PWM Port A / General Purpose Port C (bits 8 - 10)
- PWM Port B / General Purpose Port C (bits 0 - 3)
- CAN Port #1
- CAN Port #2

### 2.15.1 Address Bus Expansion Connector

The address bus expansion connector contains the 56F8367's 24 external memory address signal lines. Address lines A6 and A7 can optionally be used as GPIO Port E lines (bits 2 and 3). Address lines A8 - A15 can optionally be used as GPIO Port A lines (bits 0 - 7). Address lines A0 - A5 can optionally be used as GPIO Port A lines (bits 8 - 13). Address lines A16 - A23 are MPIO signals, which can be configured as A16 - A23 or GPIO Port B bits 0 - 7. Refer to **Table 2-16** for the address bus connector information.

**Table 2-16. External Memory Address Bus Connector Description**

| J4 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | A0 / PA8 | 2 | A1 / PA9 |
| 3 | A2 / PA10 | 4 | A3 / PA11 |
| 5 | A4 / PA12 | 6 | A5 / PA13 |
| 7 | A6 / PE2 | 8 | A7 / PE3 |
| 9 | A8 / PA0 | 10 | A9 / PA1 |
| 11 | A10 / PA2 | 12 | A11 / PA3 |
| 13 | A12 / PA4 | 14 | A13 / PA5 |
| 15 | A14 / PA6 | 16 | A15 / PA7 |
| 17 | PB0 / A16 | 18 | PB1 / A17 |
| 19 | PB2 / A18 | 20 | PB3 / A19 |
| 21 | PB4 / A20 | 22 | PB5 / A21 |
| 23 | PB6 / A22 | 24 | PB7 / A23 |
| 19 | GND | 20 | +3.3V |

## 2.15.2 Data Bus Expansion Connector

The data bus expansion connector contains the 56F8367's 16 external memory data signal lines. Refer to **Table 2-17** for the data bus connector information. Data lines D0 - D15 can also be used as GPIO Port F lines (bits 0 - 15).

**Table 2-17. External Memory Address Bus Connector Description**

| J5 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | D0 / PF9 | 2 | D1 / PF10 |
| 3 | D2 / PF11 | 4 | D3 / PF12 |
| 5 | D4 / PF13 | 6 | D5 / PF14 |
| 7 | D6 / PF15 | 8 | D7 / PF0 |
| 9 | D8 / PF1 | 10 | D9 / PF2 |
| 11 | D10 / PF3 | 12 | D11 / PF4 |
| 13 | D12 / PF5 | 14 | D13 / PF6 |
| 15 | D14 / PF7 | 16 | D15 / PF8 |
| 17 | GND | 18 | +3.3V |

### 2.15.3 External Memory Control Signal Expansion Connector

The external memory control signal connector contains the 56F8367's external memory control signal lines. CS2 and CS3 are MPIO signals, which can be configured as GPIO Port D lines (bits 0 and 1). Refer to **Table 2-18** for the names of these signals.

**Table 2-18. External Memory Control Signal Connector Description**

| J6 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | $\overline{RD}$ | 2 | $\overline{IRQA}$ |
| 3 | $\overline{WR}$ | 4 | $\overline{IRQB}$ |
| 5 | $\overline{PS}$ / $\overline{CS0}$ | 6 | $\overline{DS}$ / $\overline{CS1}$ |
| 7 | PD0 / $\overline{CS2}$ / CAN2_TX | 8 | PD1 / $\overline{CS3}$ / CAN2_RX |
| | PD2 / $\overline{CS4}$ | | PD3 / $\overline{CS5}$ |
| | PD4 / $\overline{CS6}$ | | PD5 / $\overline{CS7}$ |
| 9 | CLKO | 10 | $\overline{RESET}$ |
| 11 | GND | 12 | $\overline{RSTO}$ |

### 2.15.4 Encoder #0 / Quad Timer Channel A Expansion Connector

The Encoder #0 / Quad Timer Channel A port is an MPIO port attached to the Timer A expansion connector. This port can be configured as a Quadrature Decoder interface port or as a Quad Timer port. Refer to **Table 2-19** for the signals attached to the connector.

**Table 2-19. Timer A Signal Connector Description**

| J15 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | PHASEA0 / TA0 | 2 | PHASEB0 / TA1 |
| 3 | INDEX0 / TA2 | 4 | HOME0 / TA3 |
| 5 | GND | 6 | +3.3V |

### 2.15.5 Encoder #1 / SPI #1 Expansion Connector

The Encoder #1 / SPI #1 port is an MPIO port attached to the SPI #1 expansion connector. This port can be configured as a Quadrature Decoder interface port, a Serial Peripherial Interface, Quad Timer port or General Purpose I/O port. Refer to **Table 2-20** for the signals attached to the connector.

**Table 2-20. SPI #1 Signal Connector Description**

| J12 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | PHASEB1 / MOSI1 / TB1 / PC1 | 2 | INDEX1 / MISO1 / TB2 / PC2 |
| 3 | PHASEA1 / SCLK1 / TB0 / PC0 | 4 | HOME1 / $\overline{SS1}$ / TB3 / PC3 |
| 5 | GND | 6 | +3.3V |

### 2.15.6 Timer Channel C Expansion Connector

The Timer Channel C port is a Quad Timer port attached to the Timer C expansion connector. This port can be configured as a Quad Timer port or a General Purpose I/O port. Refer to **Table 2-21** for the signals attached to the connector.

**Table 2-21. Timer Channel C Connector Description**

| J16 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TC0 / PE8 | 2 | TC1 / PE9 |
| 3 | GND | 4 | +3.3V |

### 2.15.7 Timer Channel D Expansion Connector

The Timer Channel D port is a Quad Timer attached to the Timer D expansion connector. This port can be configured as a Quad Timer port or a General Purpose I/O port. Refer to **Table 2-22** for the signals attached to the connector.

**Table 2-22. Timer Channel D Connector Description**

| J17 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TD0 / PE10 | 2 | TD1 / PE11 |
| 3 | TD2 / PE12 | 4 | TD3 / PE13 |
| 3 | GND | 4 | +3.3V |

## 2.15.8 A/D Port A Expansion Connector

The eight-channel Analog-to-Digital conversion Port A is attached to this connector. Refer to **Table 2-23** for connection information. There is a Resistor/Connector (R/C) network on each of the Analog Port A input signals; see **Figure 2-14**.

**Table 2-23. A/D Port A Connector Description**

| J9 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | AN0 | 2 | AN1 |
| 3 | AN2 | 4 | AN3 |
| 5 | AN4 | 6 | AN5 |
| 7 | AN6 | 8 | AN7 |
| 9 | GNDA | 10 | $+V_{REFH}$ |

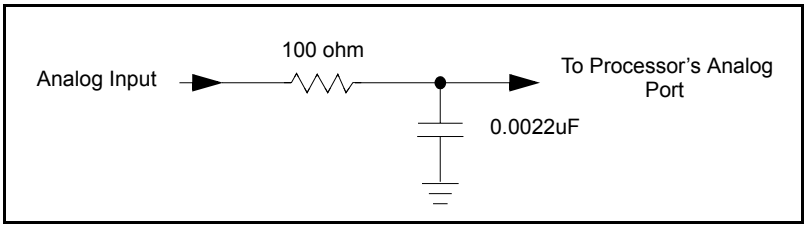


**Figure 2-14. Typical Analog Input RC Filter**

### 2.15.9 A/D Port B Expansion Connector

The eight-channel Analog-to-Digital conversion Port B is attached to this connector. Refer to **Table 2-24** for connection information. There is an R/C network on each of the Analog Port B input signals; see **Figure 2-14**.

**Table 2-24. A/D Port B Connector Description**

| J10 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | AN8 | 2 | AN9 |
| 3 | AN10 | 4 | AN11 |
| 5 | AN12 | 6 | AN13 |
| 7 | AN14 | 8 | AN15 |
| 9 | GNDA | 10 | $+V_{REFH}$ |

### 2.15.10 Serial Communications Port #0 Expansion Connector

The Serial Communications Port #0 is an MPIO port attached to the SCI #0 expansion connector. This port can be configured as a Serial Communications Interface or as a General Purpose I/O port. Refer to **Table 2-25** for connection information.

**Table 2-25. SCI #0 Connector Description**

| J13 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TXD0 / PE0 | 2 | RXD0 / PE1 |
| 3 | GND | 4 | +3.3V |
| 5 | GND | 6 | +5.0V |

## 2.15.11 Serial Communications Port #1 Expansion Connector

The Serial Communications Port #1 is an MPIO port attached to the SCI #1 expansion connector. This port can be configured as a Serial Communications Interface or as a General Purpose I/O port. Refer to **Table 2-26** for connection information.

**Table 2-26. SCI #1 Connector Description**

| J14 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | TXD1 / PD6 | 2 | RXD1 / PD7 |
| 3 | GND | 4 | +3.3V |
| 5 | GND | 6 | +5.0V |

## 2.15.12 Serial Peripheral Interface #0 Expansion Connector

The Serial Peripheral Interface #0 is an MPIO port attached to this connector. This port can be configured as a Serial Peripheral Interface or as a General Purpose I/O port. Refer to **Table 2-27** for the connection information.

**Table 2-27. SPI #0 Connector Description**

| J11 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | MOSI0 / PE5 | 2 | MISO0 / PE6 |
| 3 | SCLK0 / PE4 | 4 | $\overline{SS0}$ / PE7 |
| 5 | GND | 6 | +3.3V |

### 2.15.13 FlexCAN #1 Expansion Connector

The FlexCAN Port #1 is attached to this connector. Refer to **Table 2-28** for connection information.

**Table 2-28. CAN #1 Connector Description**

| J18 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | CAN1_TX | 2 | GND |
| 3 | CAN1_RX | 4 | GND |

### 2.15.14 FlexCAN #2 Expansion Connector

The FlexCAN Port #2 is attached to this connector. Refer to **Table 2-29** for connection information.

**Table 2-29. CAN #2 Connector Description**

| J19 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | CAN2_TX | 2 | GND |
| 3 | CAN2_RX | 4 | GND |

### 2.15.15 PWM Port A Expansion Connector

The PWM Port A is attached to this connector. Refer to **Table 2-30** for connection information.

**Table 2-30. PWM Port A Connector Description**

| J7 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | PWMA0 | 2 | PWMA1 |
| 3 | PWMA2 | 4 | PWMA3 |
| 5 | PWMA4 | 6 | PWMA5 |
| 7 | FAULTA0 | 8 | FAULTA1 |
| 9 | FAULTA2 | 10 | FAULTA3 |
| 11 | ISA0 / PC8 | 12 | ISA1 / PC9 |
| 13 | ISA2 / PC10 | 14 | GND |

### 2.15.16 PWM Port B Expansion Connector

The PWM Port B is attached to this connector. Refer to **Table 2-31** for connection information.

**Table 2-31. PWM Port B Connector Description**

| J8 | | | |
|---|---|---|---|
| **Pin #** | **Signal** | **Pin #** | **Signal** |
| 1 | PWMB0 | 2 | PWMB1 |
| 3 | PWMB2 | 4 | PWMB3 |
| 5 | PWMB4 | 6 | PWMB5 |
| 7 | FAULTB0 | 8 | FAULTB1 |
| 9 | FAULTB2 | 10 | FAULTB3 |
| 11 | ISB0 / PD10 | 12 | ISB1 / PD11 |
| 13 | ISB2 / PD12 | 14 | GND |

## 2.16 Test Points

The 56F8367EVM board has a total of seven test points:

- Analog Ground (AGND)
- Three Digital Grounds (GND)
- +3.3V
- +3.3VA
- +5.0V

# Appendix A
# 56F8367EVM Schematics

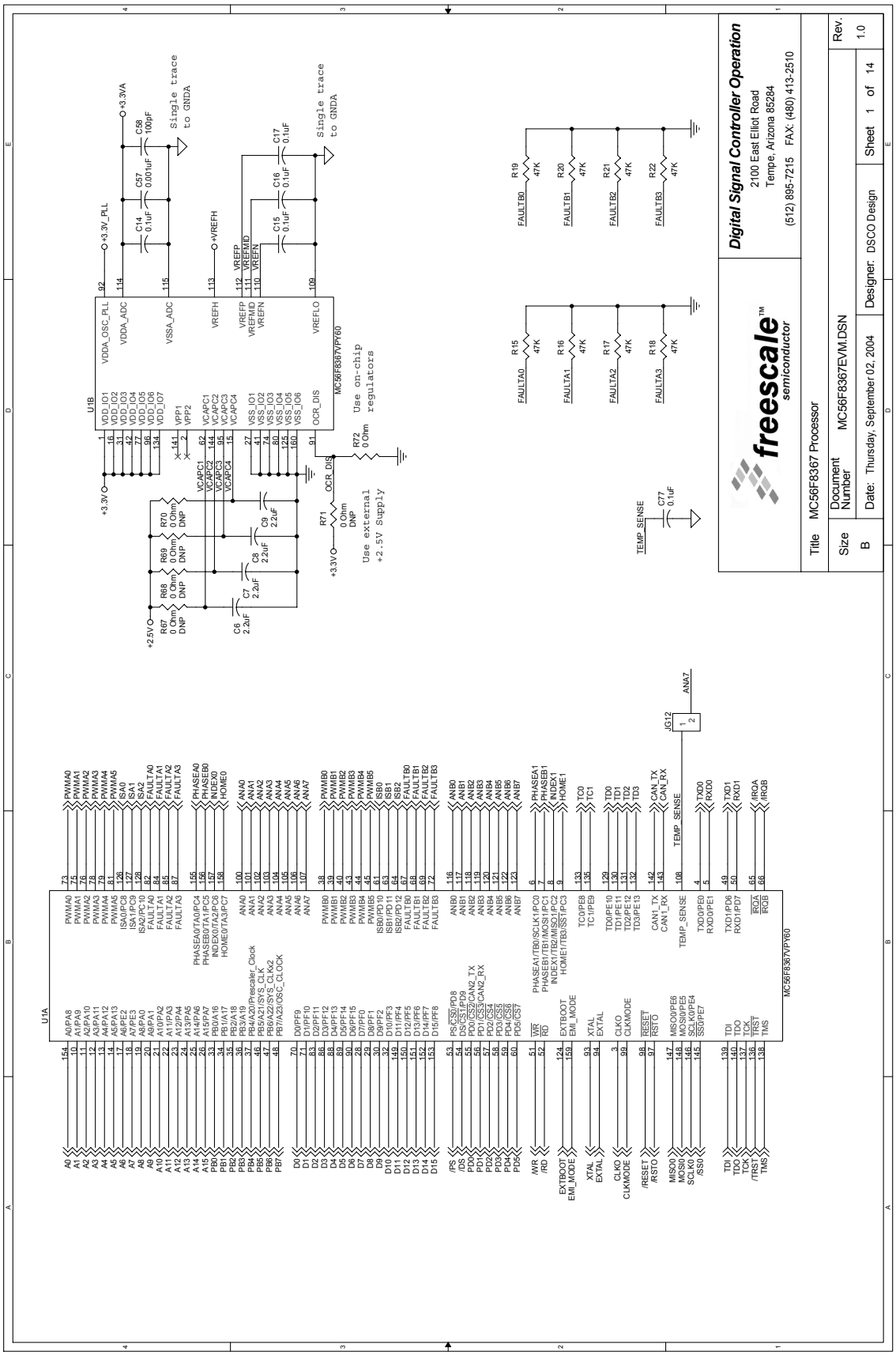


**Figure A-1. 56F8367 Processor**

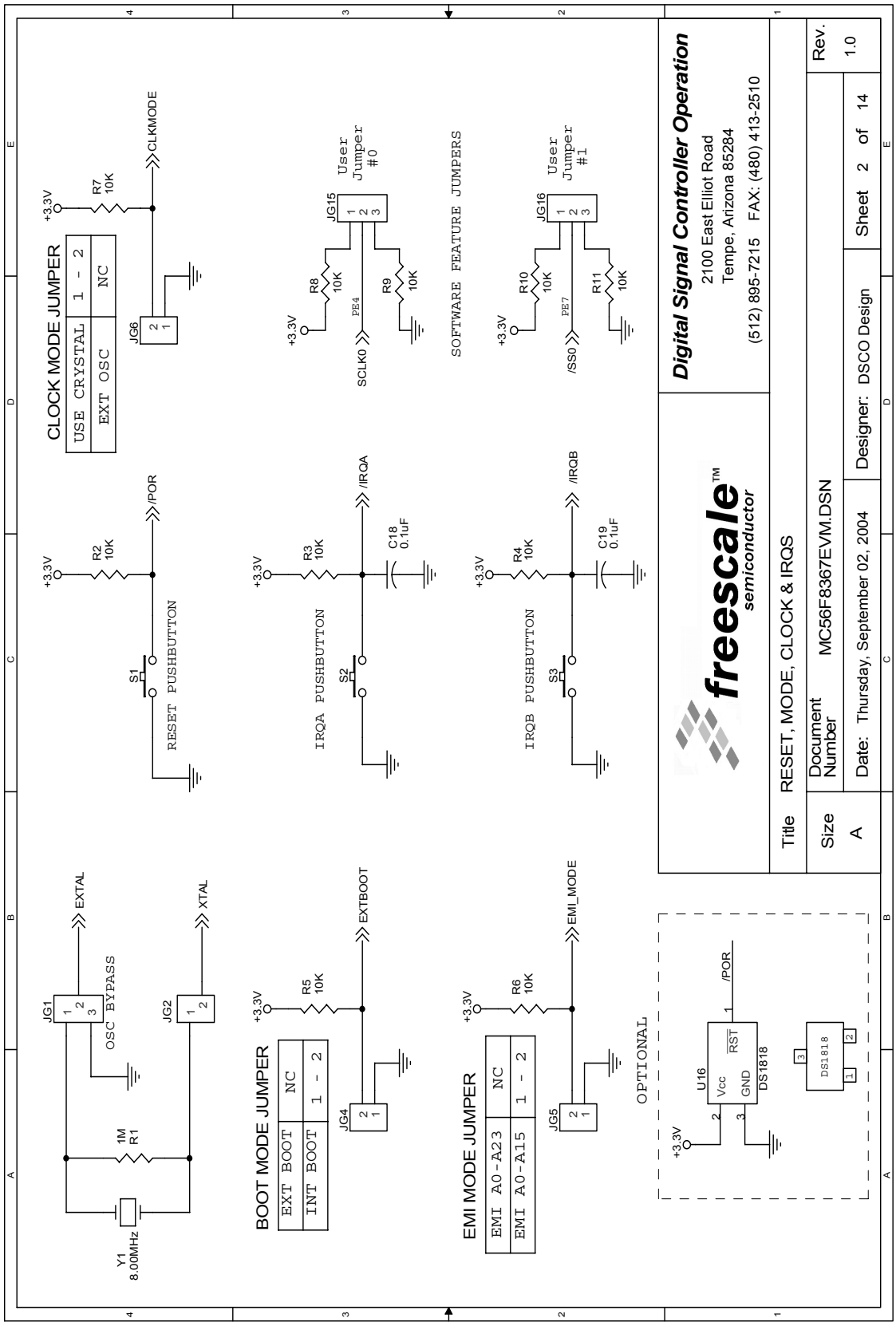


**Figure A-2. Reset, Mode, Clock & IRQs**

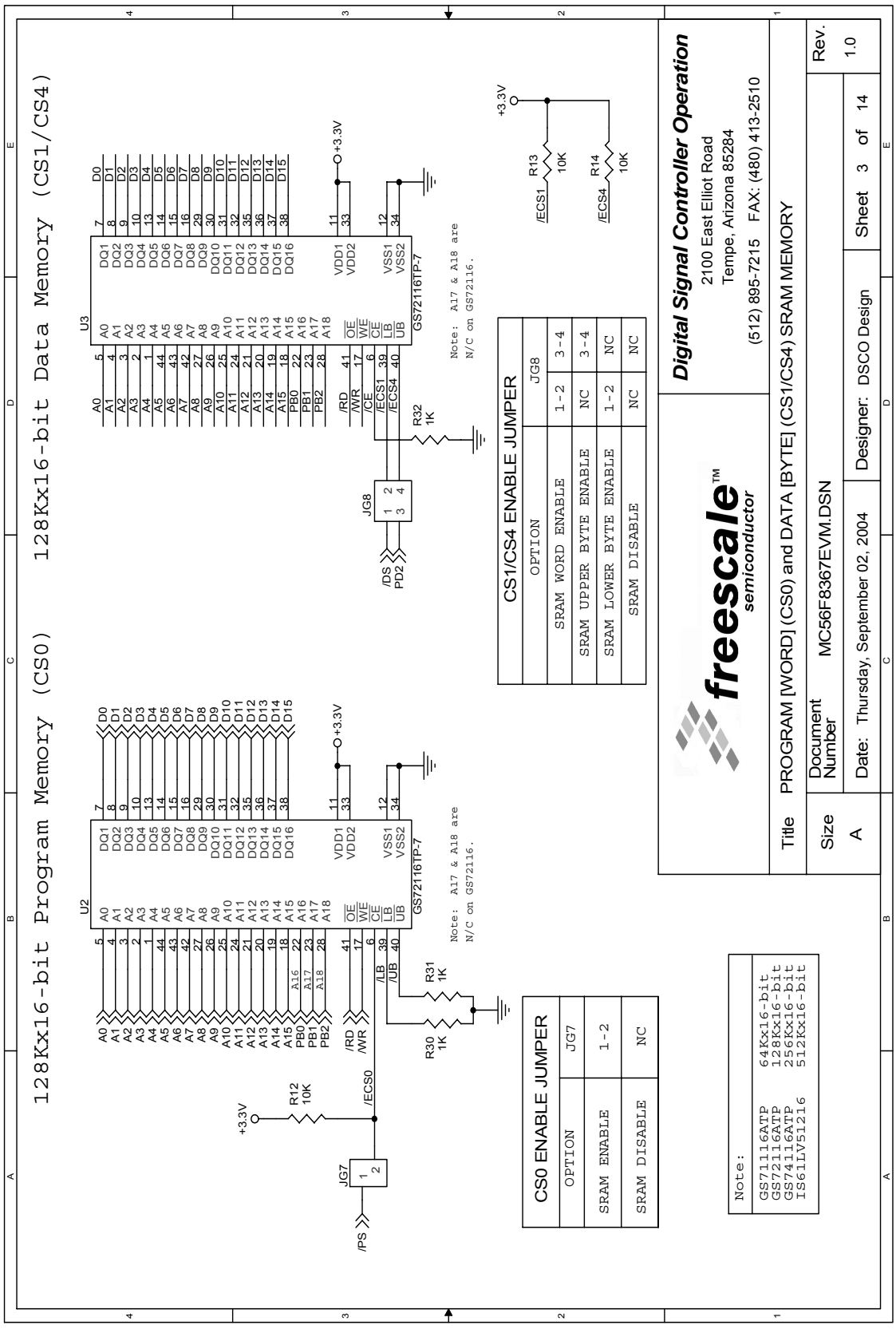


**Figure A-3. Program [Word] (CS0) & Data [Byte] (CS1/CS4) SRAM Memory**

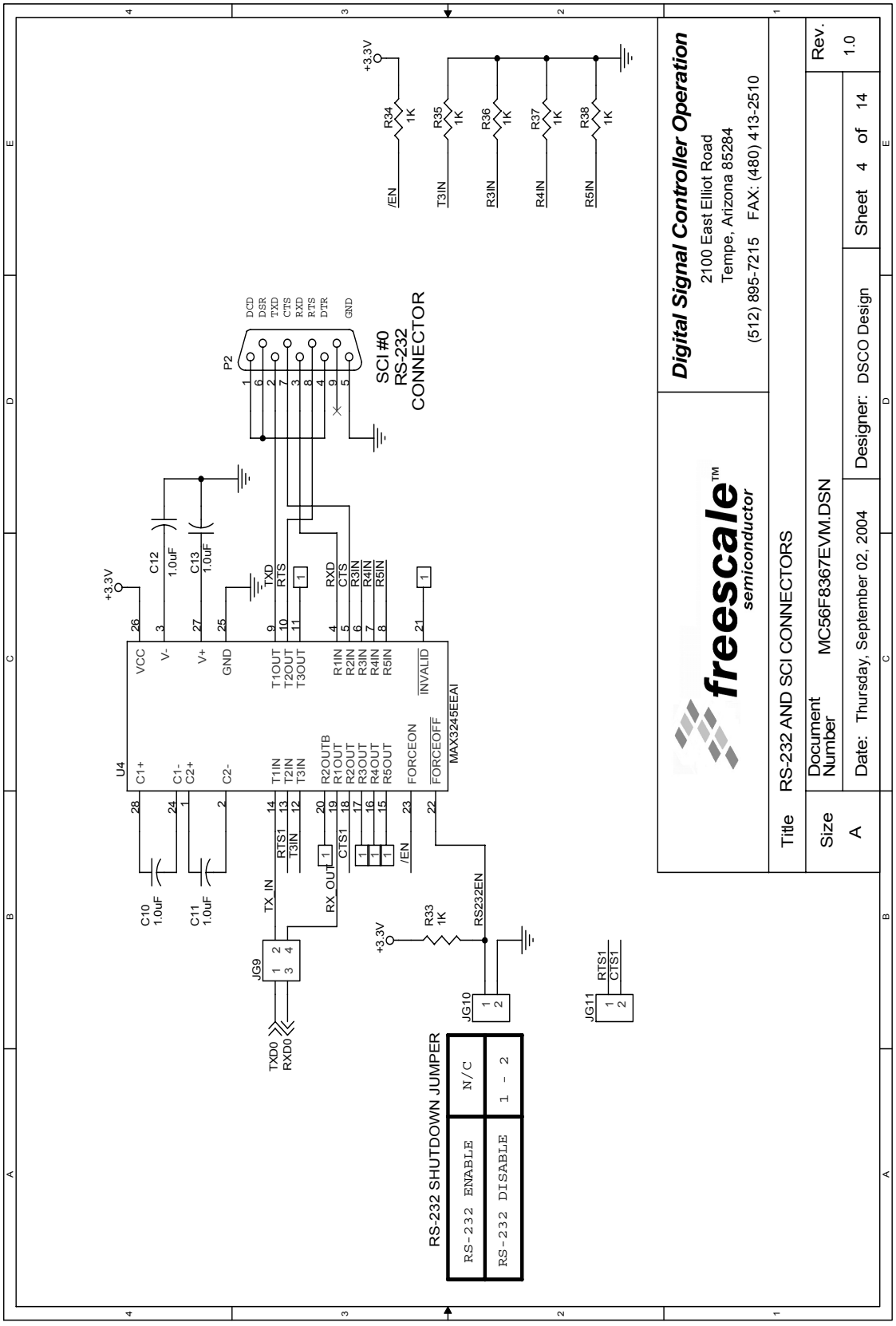


**Figure A-4. RS-232 and SCI Connectors**

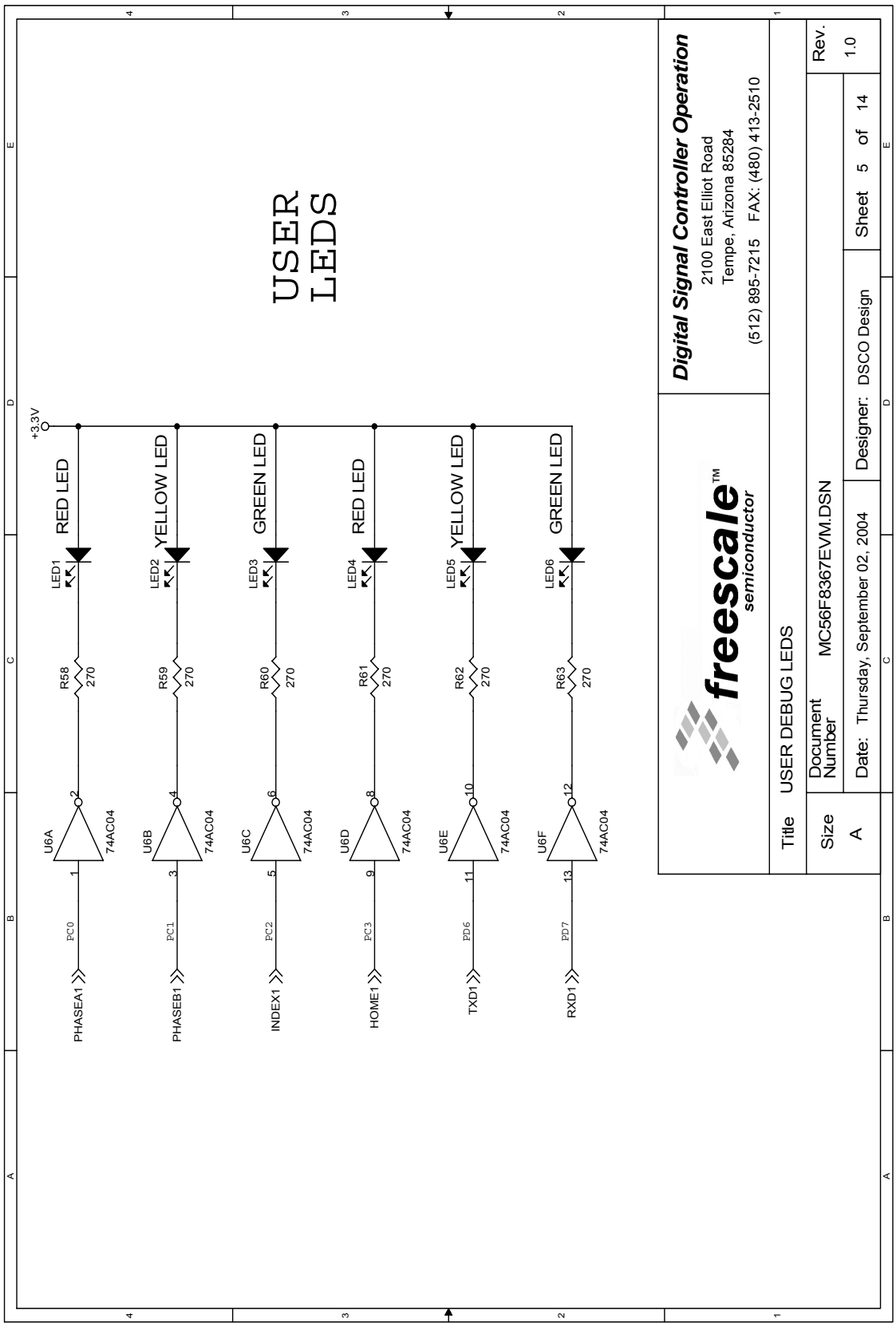


**Figure A-5. User Debug LEDs**

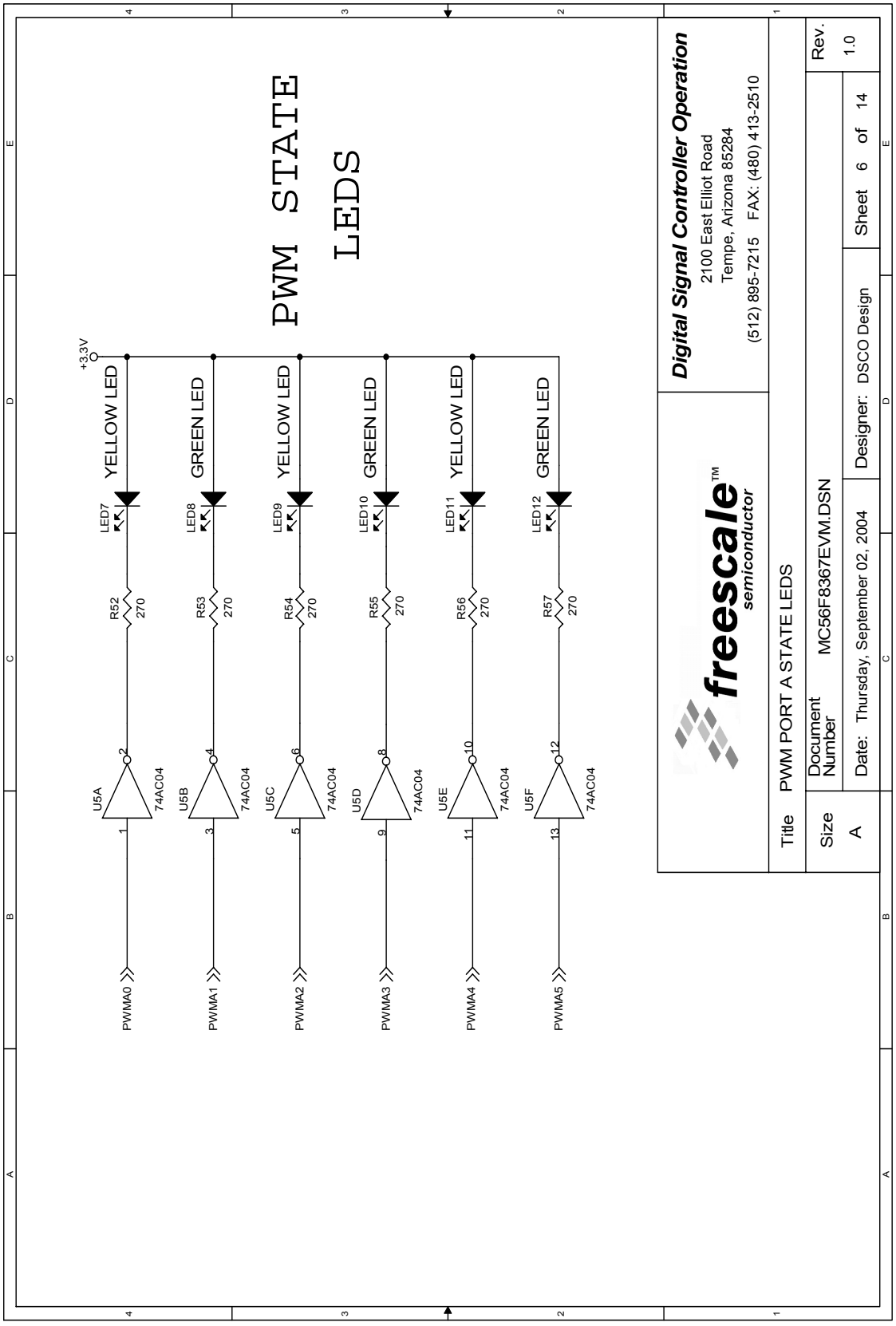


**Figure A-6. PWM Port A State LEDs**

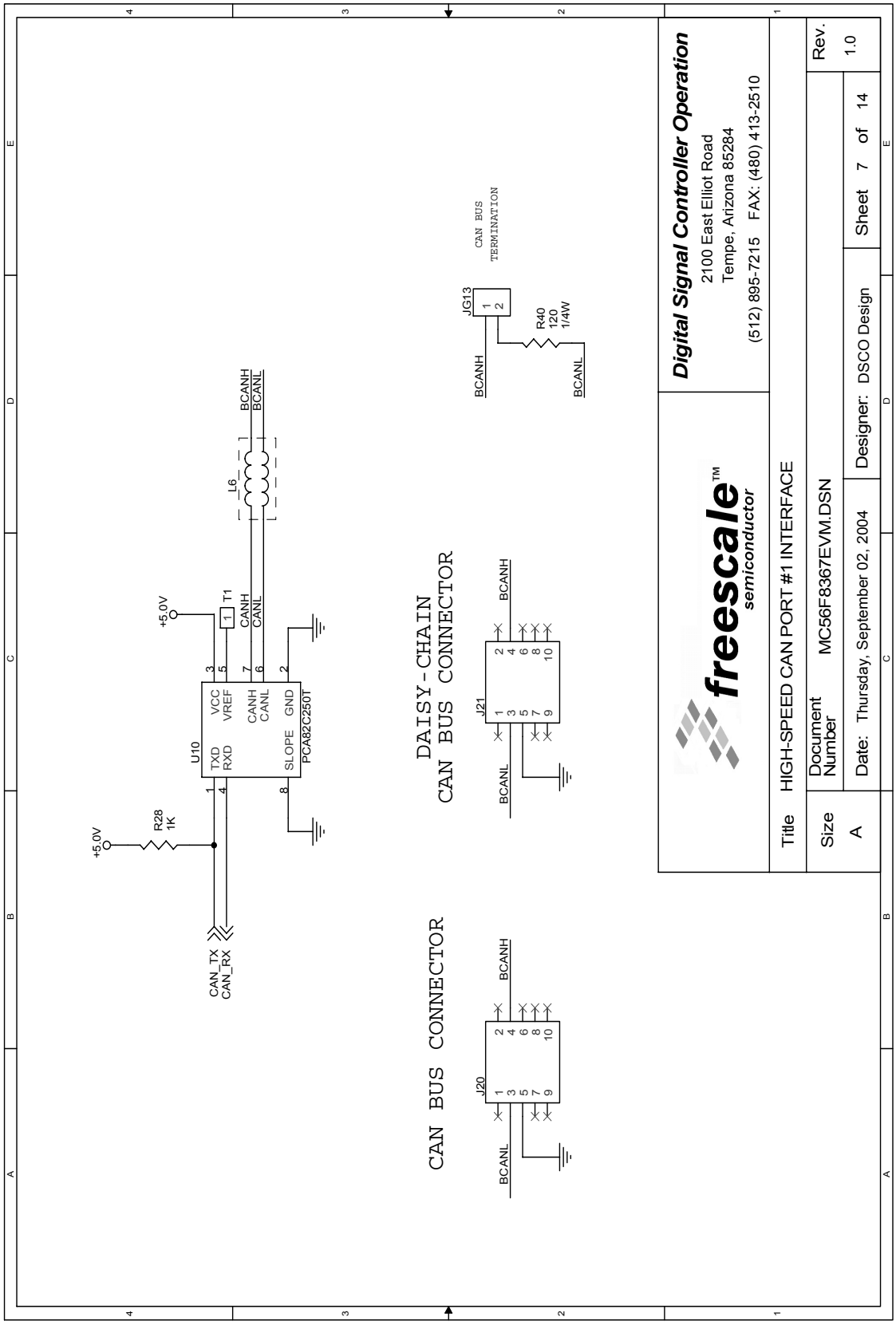


**Figure A-7. High-Speed CAN Port #1 Interface**

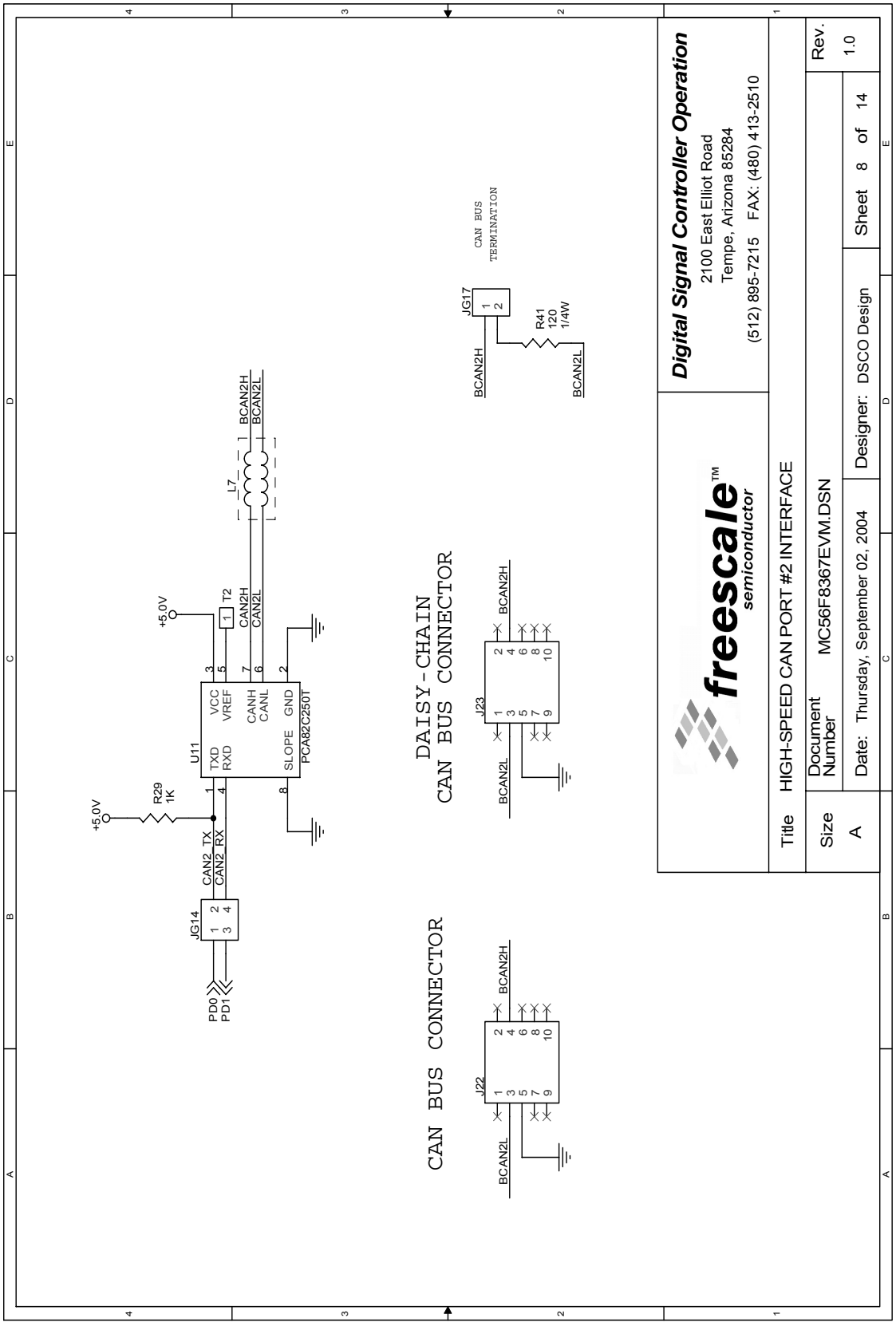


**Figure A-8. High-Speed CAN Port #2 Interface**

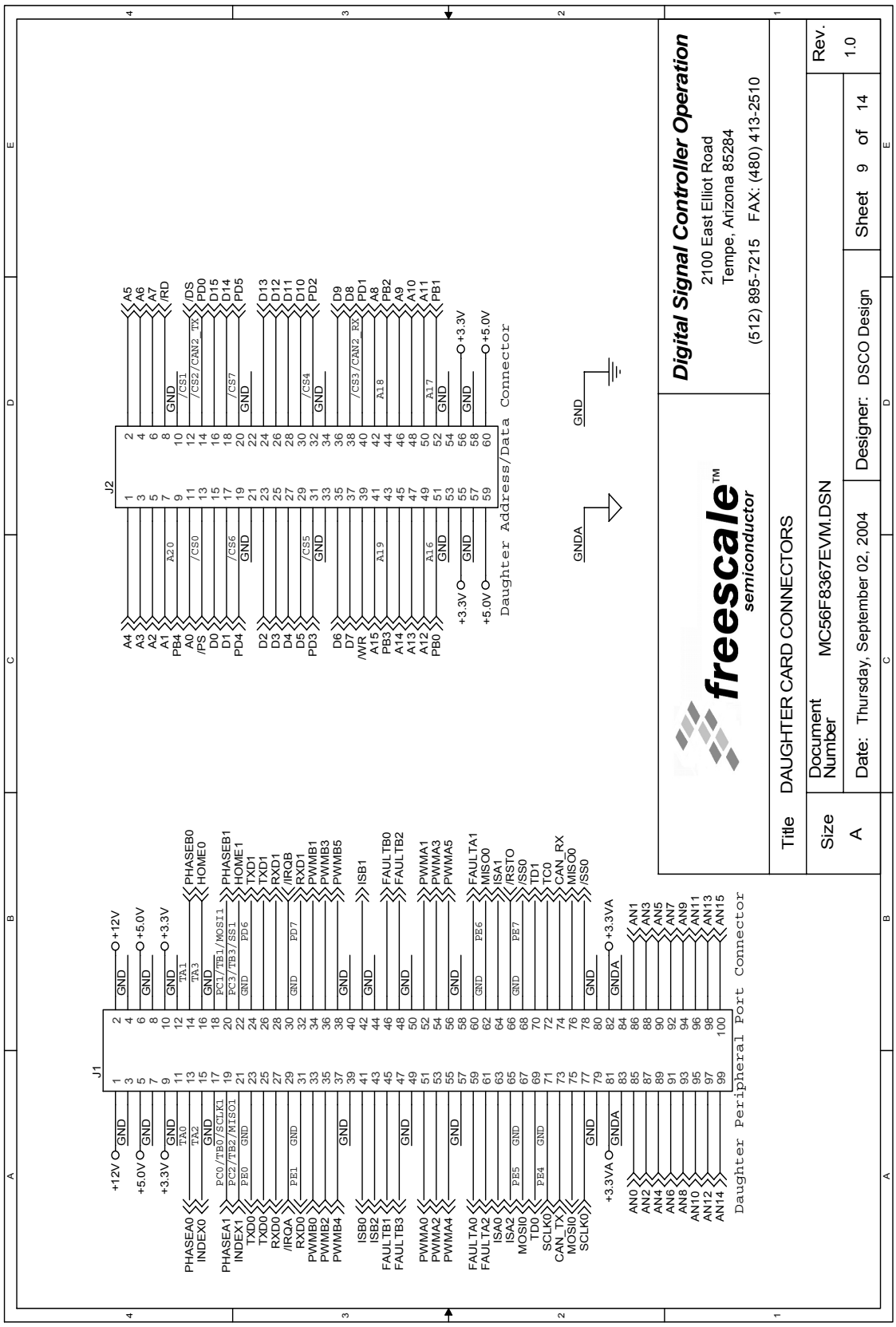


**Figure A-9. Daughter Card Connectors**

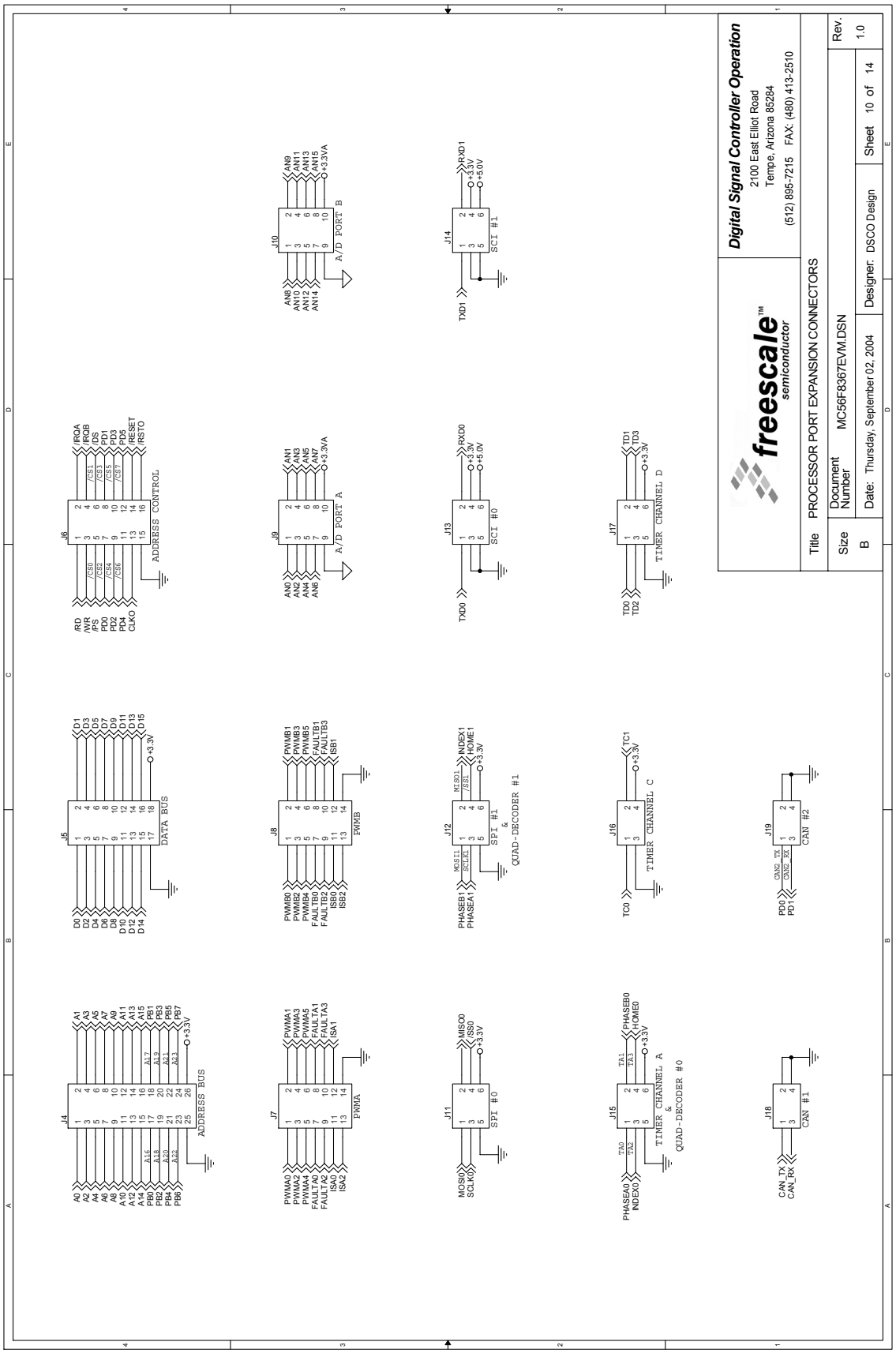


**Figure A-10. Processor Port Expansion Connectors**

**56F8367EVM Schematics, Rev. 2**

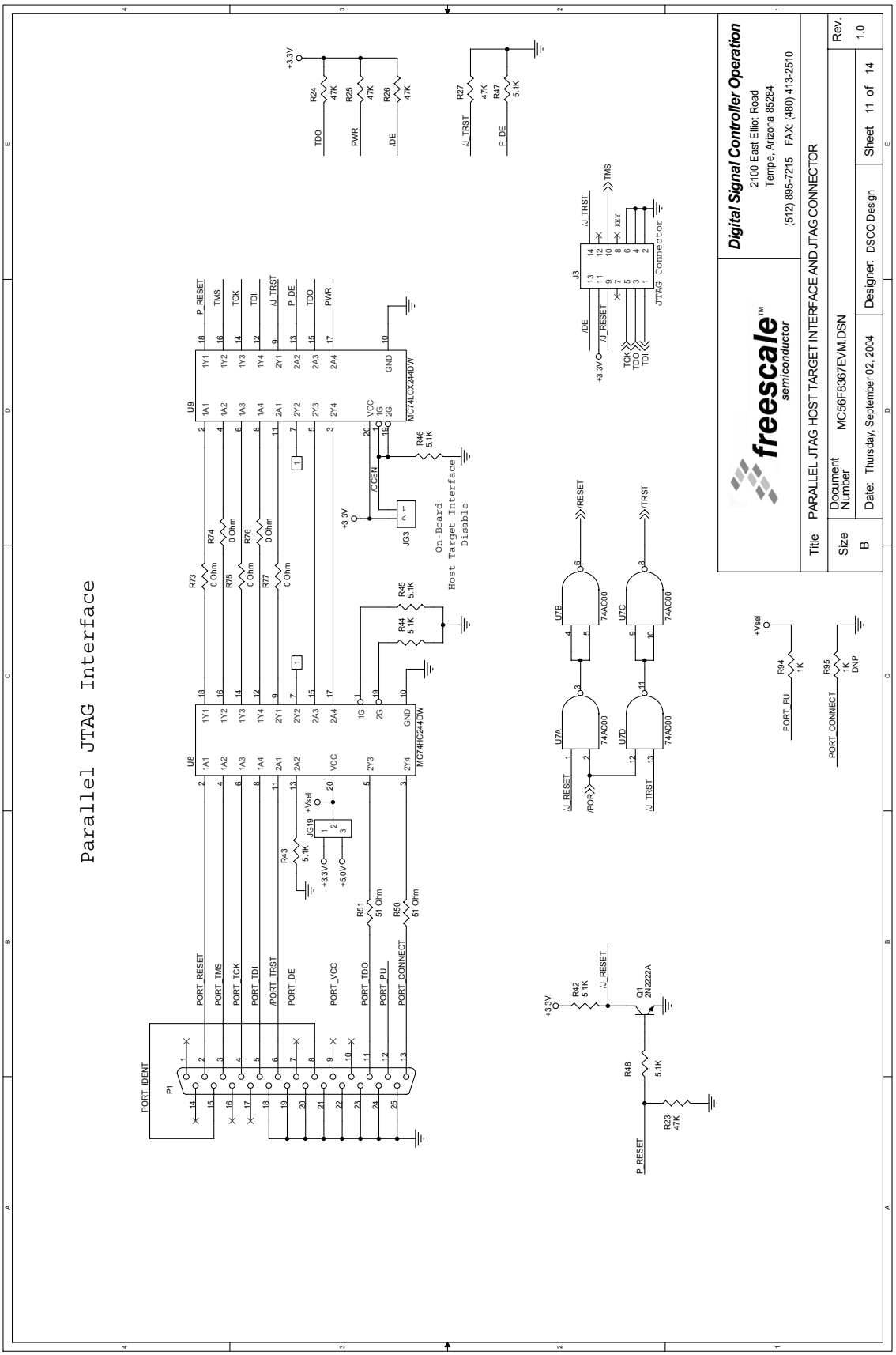


**Figure A-11. Parallel JTAG Host Target Interface and JTAG Connector**

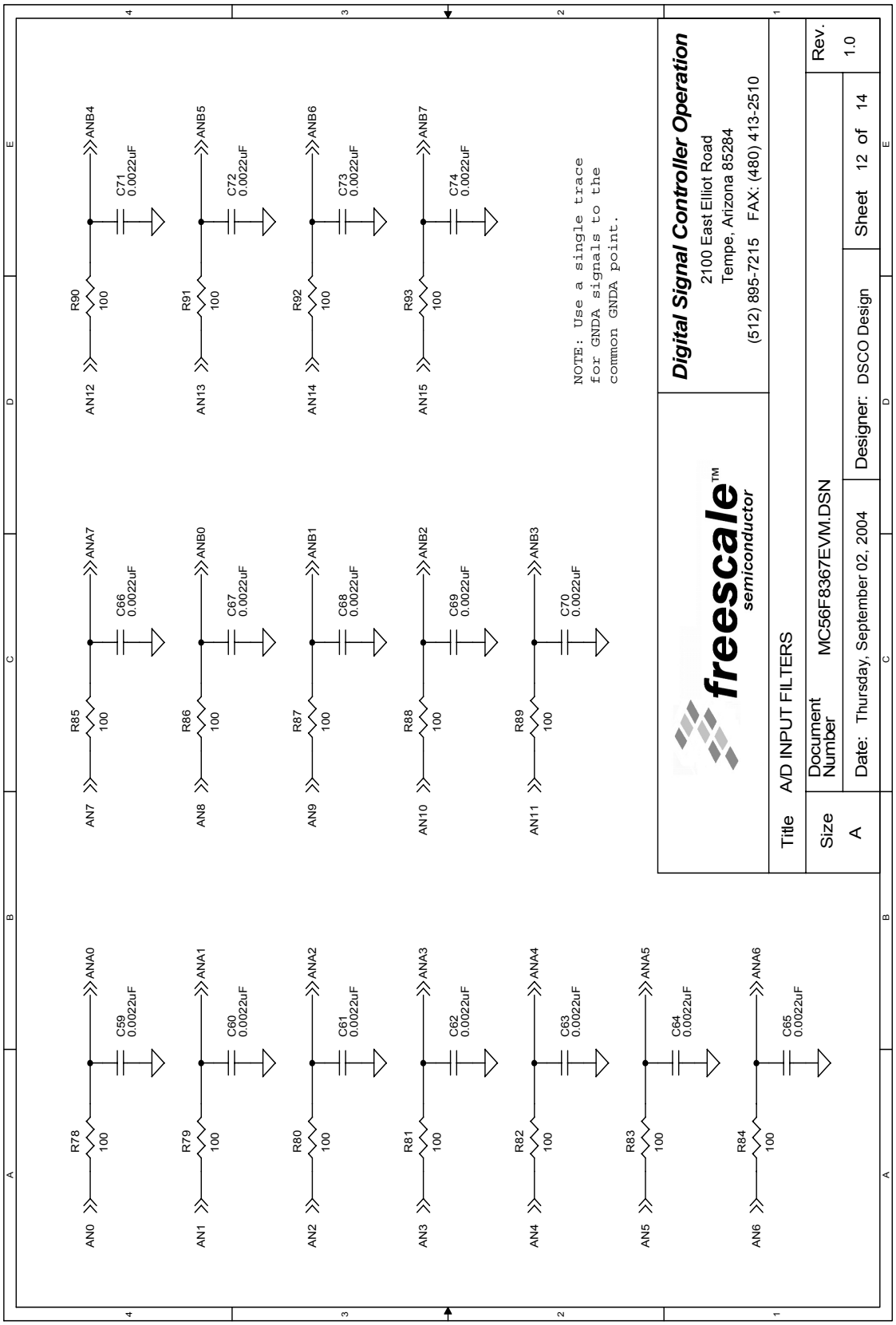


**Figure A-12. A/D Input Filters**

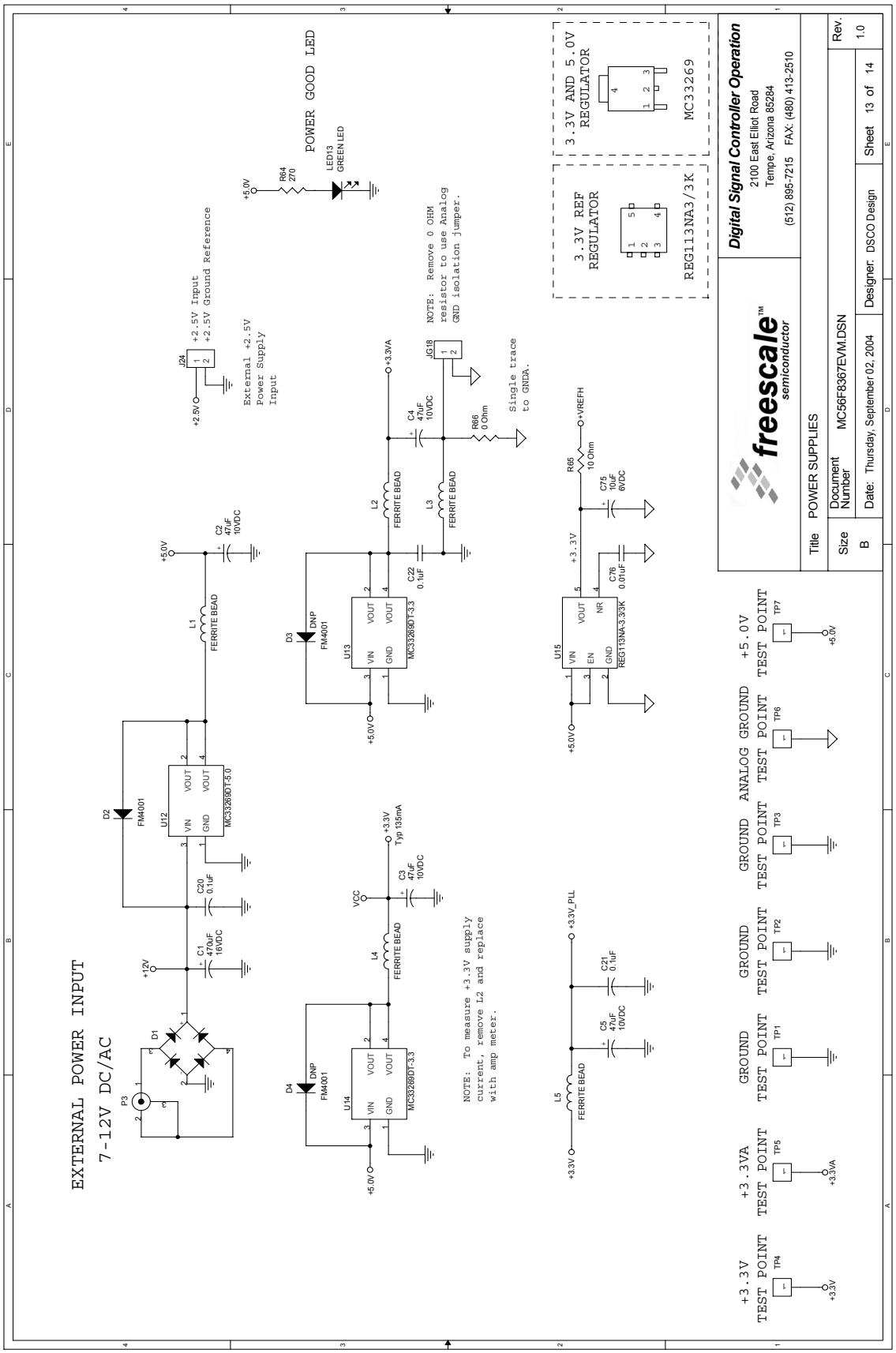


**Figure A-13. Power Supplies**

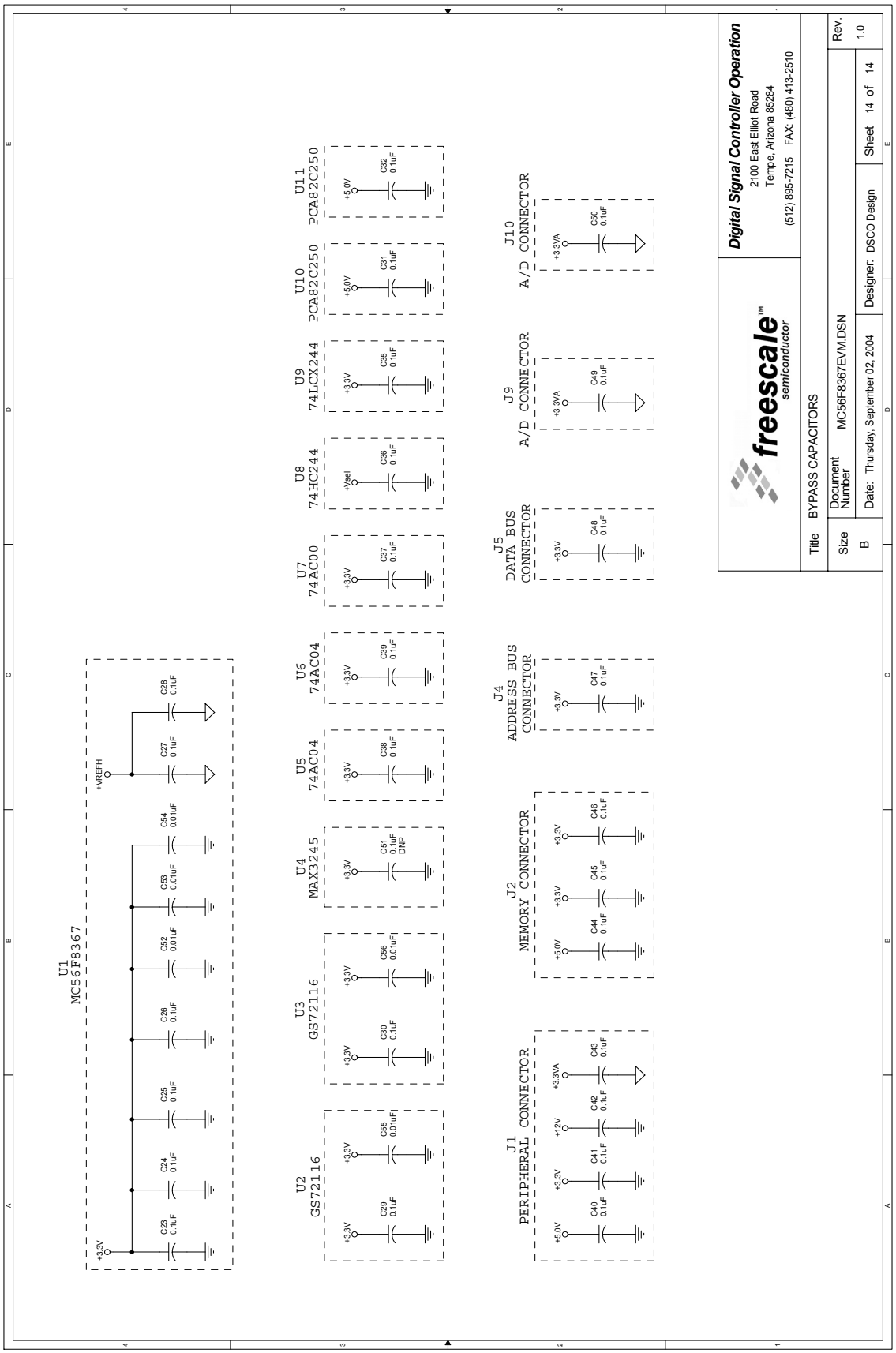


**Figure A-14. Bypass Capacitors**

# Appendix B
# 56F8367EVM Bill of Material

| Qty | Description | Ref. Designators | Vendor Part # |
|---|---|---|---|
| **Integrated Circuits** | | | |
| 1 | MC56F8367 | U1 | Freescale, MC56F8367VPY60 |
| 2 | 128K x 16-Bit SRAM | U2, U3 | GSI, GS72116ATP-8 |
| 1 | RS-232 Transceiver | U4 | Maxim, MAX3245EEAI |
| 2 | 74AC04 | U5, U6 | ON Semiconductor, MC74AC04AD |
| 1 | 74AC00 | U7 | Fairchild, 74AC00SC |
| 1 | 74HC244 | U8 | ON Semiconductor, MC74LHC44AADW |
| 1 | 74LCX244 | U9 | ON Semiconductor, MC74LCX244ADW |
| 2 | CAN Transceiver | U10, U11 | Philips Semiconductor, PCA82C250T |
| 1 | +5.0V Voltage Regulator | U12 | ON Semiconductor, MC33269DT-5 |
| 2 | +3.3V Voltage Regulator | U13, U14 | ON Semiconductor, MC33269DT-3.3 |
| 1 | +3.3V Voltage Regulator | U15 | Burr-Brown, REG113NA-3.3 |
| 0 | Power-On Reset | U16 (Optional) | Dallas Semiconductor, DS1818 |
| **Resistors** | | | |
| 1 | 1MΩ | R1 | SMEC, RC73L2A105OHMJT |
| 13 | 10KΩ | R2 - R14 | SMEC, RC73L2A103OHMJT |
| 13 | 47KΩ | R15 - R27 | SMEC, RC73L2A473OHMJT |
| 12 | 1KΩ | R28 - R38, R94 | SMEC, RC73L2A103OHMJT |
| 0 | 1KΩ | R95 (Optional) | SMEC, RC73L2A103OHMJT |
| 2 | 120Ω, 1/4W | R40, R41 | YAGEO, CFR 120QBK |

| Qty | Description | Ref. Designators | Vendor Part # |
|---|---|---|---|
| **Resistors (Continued)** | | | |
| 7 | 5.1KΩ | R42 - R48 | SMEC, RC73L2A512OHMJT |
| 2 | 51Ω | R50, R51 | SMEC, RC73L2A51OHMJT |
| 13 | 270Ω | R52 - R64 | SMEC, RC73L2A271OHMJT |
| 1 | 10Ω | R65 | SMEC, RC73L2A100OHMJT |
| 7 | 0Ω | R66, R72 - R77 | SMEC, RC73JP2A |
| 0 | 0Ω | R67 - R71 (Optional) | SMEC, RC73JP2A |
| 16 | 100Ω | R78 - R93 | SMEC, RC73L2A101OHMJT |
| **Inductors** | | | |
| 5 | 1.0mH FERRITE BEAD | L1 - L5 | Panasonic, EXC-ELSA35V |
| 2 | CAN Bus Filter | L6, L7 | EPCOS, B82790-S0513-N201 |
| **LEDs** | | | |
| 2 | Red LED | LED1, LED4 | Hewlett-Packard, HSMS-C650 |
| 5 | Yellow LED | LED2, LED5, LED7, LED9, LED11 | Hewlett-Packard, HSMY-C650 |
| 6 | Green LED | LED3, LED6, LED8, LED10, LED12, LED13 | Hewlett-Packard, HSMG-C650 |
| **Diode** | | | |
| 1 | +50V 1A BRIDGE RECT | D1 | DIODES, DF02S |
| 1 | S2B-FM401 | D2 | Vishay, DL4001DICT |
| 0 | S2B-FM401 | D3, D4 (Optional) | Vishay, DL4001DICT |
| **Capacitors** | | | |
| 1 | 470μF, +16V DC | C1 | ELMA, RV-16V471MH10R |
| 4 | 47μF, +16V DC | C2 - C5 | ELMA, RV2-16V470M-R |
| 4 | 2.2μF, +25V DC (Low ESR) | C6 - C9 | TAIYO YUDEN, CELMK212BJ225MG-T |
| 4 | 1.0μF, +25V DC | C10 - C13 | SMEC, MCCE105K3NR-T1 |
| 37 | 0.1μF | C14 - C32, C35 - C51, C77 | SMEC, MCCE104K2NR-T1 |
| 6 | 0.01μF | C52 - C56, C76 | SMEC, MCCE103K2NR-T1 |

| Qty | Description | Ref. Designators | Vendor Part # |
|---|---|---|---|
| **Capacitors (Continued)** | | | |
| 1 | 0.001μF | C57 | SMEC, MCCE102K2NR-T1 |
| 1 | 100pF | C58 | SMEC, MCCE101K2NR-T1 |
| 16 | 0.0022μF | C59 - C74 | SMEC, MCCE222K2NR-T1 |
| 1 | 10μF, +10V DC | C75 | KEMET, T494B106M010AS |
| **Jumpers** | | | |
| 4 | 3 × 1 Bergstick | JG1, JG15, JG16, JG19 | SAMTEC, TSW-103-07-S-S |
| 12 | 1 × 2 Bergstick | JG2 - JG7, JG10 - JG13, JG17, JG18 | SAMTEC, TSW-102-07-S-S |
| 3 | 2 × 2 Bergstick | JG8, JG9, JG14 | SAMTEC, TSW-102-07-S-D |
| **Test Points** | | | |
| 3 | GND Test Point | TP1, TP2, TP3 | KEYSTONE, 5001, BLACK |
| 1 | +3.3V Test Point | TP4 | KEYSTONE, 5000, RED |
| 1 | +3.3V A Test Point | TP5 | KEYSTONE, 5004, YELLOW |
| 1 | GNDA Test Point | TP6 | KEYSTONE, 5002, WHITE |
| 1 | +5.0V Test Point | TP7 | KEYSTONE, 5003, ORANGE |
| **Crystals** | | | |
| 1 | 8.00MHz Crystal | Y1 | CTS, ATS08ASM-T |
| **Connectors** | | | |
| 1 | DB25M Connector | P1 | AMPHENOL, 617-C025P-AJ121 |
| 1 | DE9S Connector | P2 | AMPHENOL, 617-C009S-AJ120 |
| 1 | 2.1mm coax Power Connector | P3 | Switchcraft, RAPC-722 |
| 1 | Peripheral Daughter Card Connector | J1 | HRS, FX6-100P-0.8SV2 |
| 1 | Memory Bus Daughter Card Connector | J2 | HRS, FX6-60P-0.8SV2 |
| 1 | 7 x 2 JTAG Header | J3 | SAMTEC, TSW-106-07-S-D |
| 1 | 13 x 2 Header | J4 | SAMTEC, TSW-106-13-S-D |

**56F8367EVM Bill of Material, Rev. 2**

| Qty | Description | Ref. Designators | Vendor Part # |
|---|---|---|---|
| **Connectors (Continued)** | | | |
| 1 | 9 x 2 Header | J5 | SAMTEC, TSW-106-09-S-D |
| 1 | 8 x 2 Header | J6 | SAMTEC, TSW-106-08-S-D |
| 2 | 7 x 2 Header | J7, J8 | SAMTEC, TSW-106-07-S-D |
| 6 | 5 x 2 Header | J9, J10, J20 - J23 | SAMTEC, TSW-106-05-S-D |
| 6 | 3 x 2 Header | J11 - J15, J17 | SAMTEC, TSW-106-03-S-D |
| 3 | 2 x 2 Header | J16, J18, J19 | SAMTEC, TSW-106-02-S-D |
| **Switches** | | | |
| 3 | SPST Push button | S1 - S3 | Panasonic, EVQ-PAD05R |
| **Transistors** | | | |
| 1 | 2N2222A | Q1 | ZETEX, FMMT2222ACT |
| **Miscellaneous** | | | |
| 18 | Shunt | SH1 - SH13 | Samtec, SNT-100-BL-T |
| 4 | Rubber Feet | RF1 - RF4 | 3M, SJ5018BLKC |

# INDEX

## Numerics



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**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
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support.japan@freescale.com

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