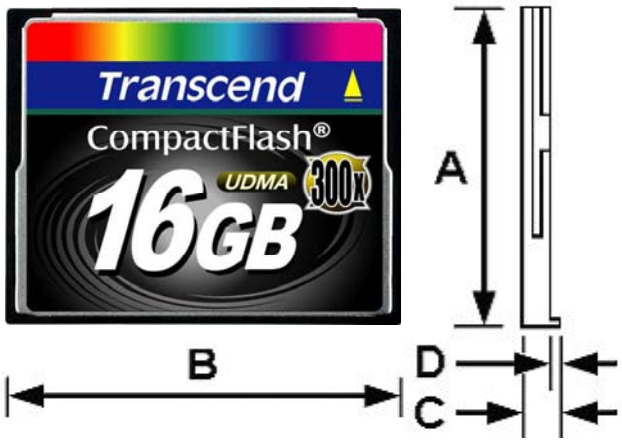
Description

The Transcend CF 300X is a High Speed Compact Flash Card with high quality Flash Memory assembled on a printed circuit board.

Placement

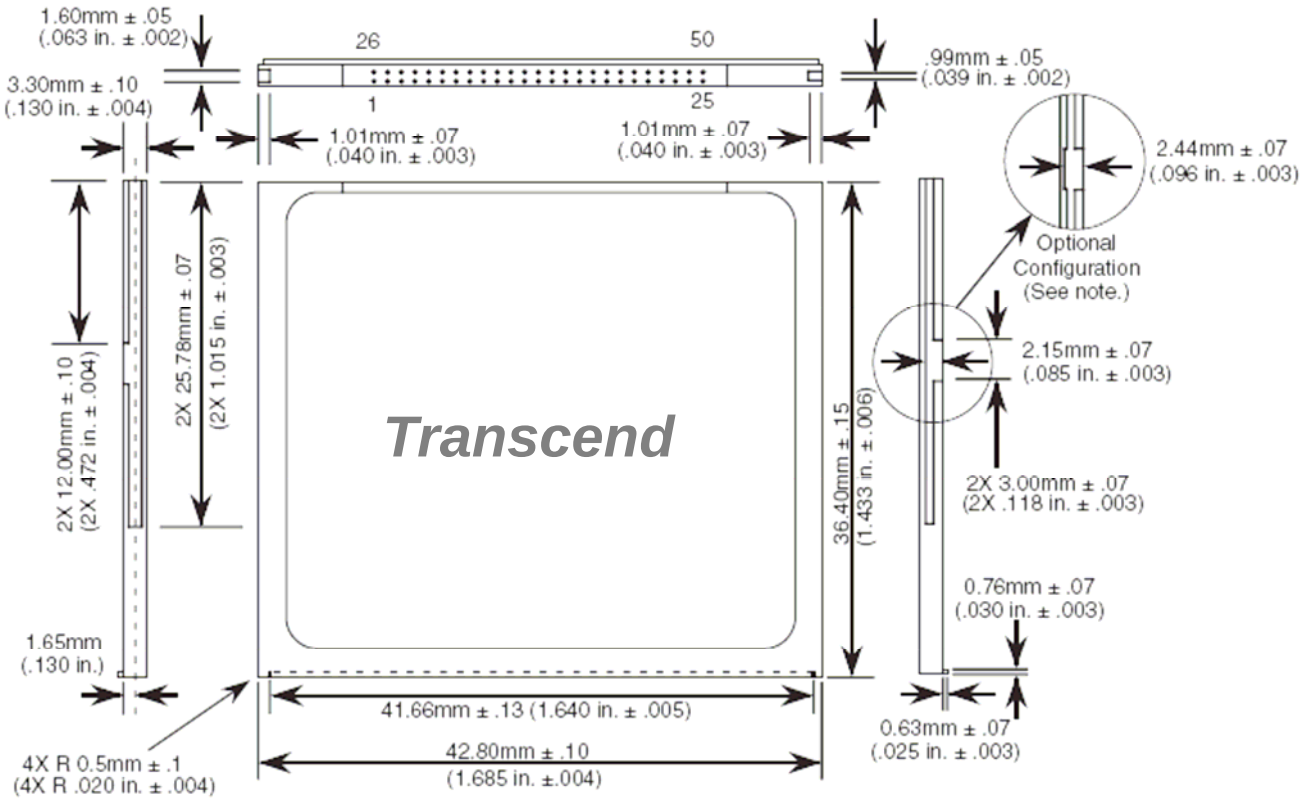


Features

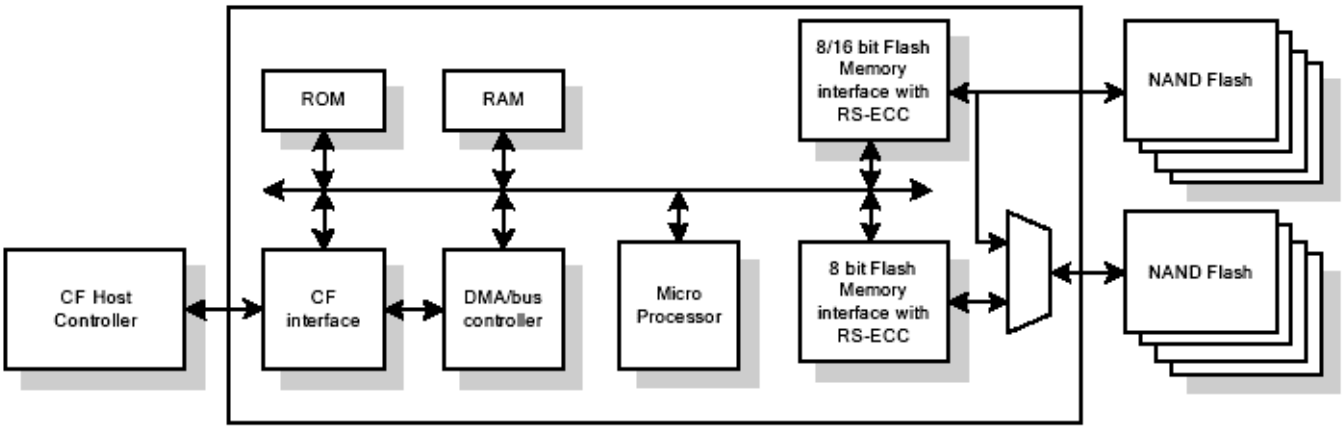
- CompactFlash Specification Version 4.1 Complaint
- RoHS compliant products
- Single Power Supply: 3.3V±5% or 5V±10%
- Operating Temperature: -25°C to 85°C
- Storage Temperature: -40°C to 85°C
- Operation Modes:
  - ✓ PC Card Memory Mode
  - ✓ PC Card IO Mode
  - ✓ True IDE Mode
- True IDE Mode supports:
  - ✓ Ultra DMA Mode 0 to Ultra DMA Mode 5 (Ultra DMA mode 5 must use Power supply: 3.3V)
  - ✓ MultiWord DMA Mode 0 to MultiWord DMA Mode 4
  - ✓ PIO Mode 0 to PIO Mode 6
- PC Card Mode supports up to Ultra DMA Mode 5
- Support PIO mode 0 to PIO mode 6
- True IDE mode: Fixed Disk (Standard)
- PC Card Mode: Removable Disk (Standard)
- Durability of Connector: 10,000 times
- Support S.M.A.R.T (Self-defined)
- Support Security Command
- Support Wear-Leveling to extend product life
- Compliant to CompactFlash, PCMCIA, and ATA standards

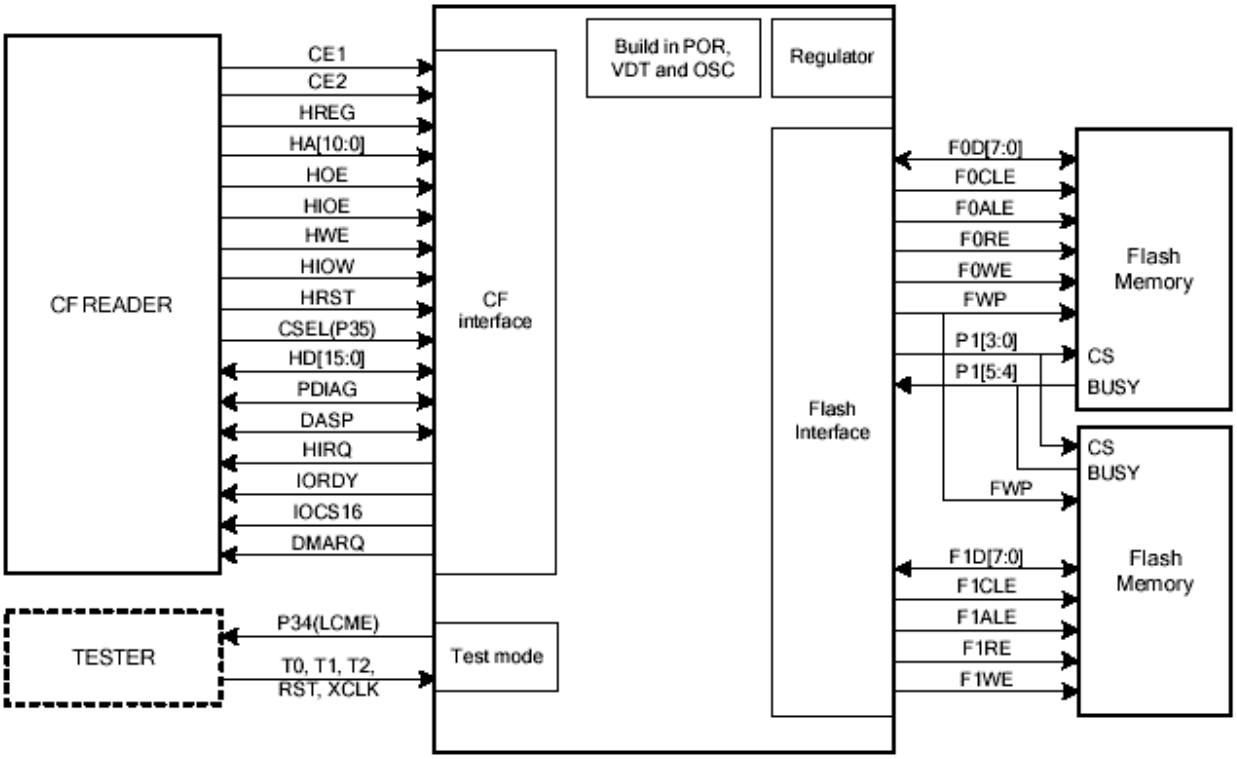
Dimensions

Side	Millimeters	Inches
A	36.40 ± 0.150	1.43 ± 0.005
B	42.80 ± 0.100	1.69 ± 0.004
C	3.30 ± 0.100	0.13 ± 0.004
D	0.63 ± 0.070	0.02 ± 0.003


1.60mm ± .05
(.063 in. ± .002)
3.30mm ± .10
(.130 in. ± .004)
26
50
1
25
.99mm ± .05
(.039 in. ± .002)
1.01mm ± .07
(.040 in. ± .003)
1.01mm ± .07
(.040 in. ± .003)
2.44mm ± .07
(.096 in. ± .003)
Optional
Configuration
(See note.)
2.15mm ± .07
(.085 in. ± .003)
2X 12.00mm ± .10
(2X .472 in. ± .004)
2X 25.78mm ± .07
(2X 1.015 in. ± .003)
Transcend
36.40mm ± .15
(1.433 in. ± .006)
2X 3.00mm ± .07
(2X .118 in. ± .003)
0.76mm ± .07
(.030 in. ± .003)
1.65mm
(.130 in.)
41.66mm ± .13 (1.640 in. ± .005)
0.63mm ± .07
(.025 in. ± .003)
4X R 0.5mm ± .1
(4X R .020 in. ± .004)
42.80mm ± .10
(1.685 in. ±.004)

Block Diagram





Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3
7	-CE1	I	I3U	7	-CE1	I	I3U	7	-CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10[2]	I	I1Z
9	-OE	I	I3U	9	-OE	I	I3U	9	-ATA SEL	I	I3U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09[2]	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08[2]	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07[2]	I	I1Z
13	VCC		Power	13	VCC		Power	13	VCC		Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06[2]	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05[2]	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04[2]	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03[2]	I	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3
22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3
23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3
24	WP	O	OT3	24	-IOIS16	O	OT3	24	-IOCS16	O	ON3
25	-CD2	O	Ground	25	-CD2	O	Ground	25	-CD2	O	Ground
26	-CD1	O	Ground	26	-CD1	O	Ground	26	-CD1	O	Ground
27	D11[1]	I/O	I1Z, OZ3	27	D11[1]	I/O	I1Z, OZ3	27	D11[1]	I/O	I1Z, OZ3
28	D121	I/O	I1Z, OZ3	28	D12[1]	I/O	I1Z, OZ3	28	D12[1]	I/O	I1Z, OZ3
29	D13[1]	I/O	I1Z, OZ3	29	D13[1]	I/O	I1Z, OZ3	29	D13[1]	I/O	I1Z, OZ3
30	D14[1]	I/O	I1Z, OZ3	30	D14[1]	I/O	I1Z, OZ3	30	D14[1]	I/O	I1Z, OZ3
31	D15[1]	I/O	I1Z, OZ3	31	D15[1]	I/O	I1Z, OZ3	31	D15[1]	I/O	I1Z, OZ3
32	-CE2[1]	I	I3U	32	-CE2[1]	I	I3U	32	-CS1[1]	I	I3Z
33	-VS1	O	Ground	33	-VS1	O	Ground	33	-VS1	O	Ground

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
34	-IORD HSTROBE[10] HDMARDY[11]	I	I3U	34	-IORD HSTROBE[10] -HDMARDY[11]	I	I3U	34	-IORD[7] HSTROBE[8] -HDMARDY[9]	I	I3Z
35	-IOWR STOP[10,11]	I	I3U	35	-IOWR STOP[10,11]	I	I3U	35	-IOWR[7] STOP[8,9]	I	I3Z
36	-WE	I	I3U	36	-WE	I	I3U	36	-WE[3]	I	I3U
37	READY	O	OT1	37	-IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		Power	38	VCC		Power	38	VCC		Power
39	-CSEL[5]	I	I2Z	39	-CSEL[5]	I	I2Z	39	-CSEL	I	I2U
40	-VS2	O	OPEN	40	-VS2	O	OPEN	40	-VS2	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	-RESET	I	I2Z
42	-WAIT -DDMARDY[10] DSTROBE[11]	O	OT1	42	-WAIT -DDMARDY[10] DSTROBE[11]	O	OT1	42	IORDY[7] -DDMARDY[8] DSTROBE[9]	O	ON1 OT1[13]
43	-INPACK -DMARQ[12]	O	OT1	43	-INPACK -DMARQ[12]	O	OT1	43	DMARQ	O	OZ1
44	-REG -DMACK [12]	I	I3U	44	-REG DMACK [12]	I	I3U	44	-DMACK [6]	I	I3U
45	BVD2	O	OT1	45	-SPKR	O	OT1	45	-DASP	I/O	I1U, ON1
46	BVD1	O	OT1	46	-STSCHG	O	OT1	46	-PDIAG	I/O	I1U, ON1
47	D08[1]	I/O	I1Z, OZ3	47	D08[1]	I/O	I1Z, OZ3	47	D08[1]	I/O	I1Z, OZ3
48	D09[1]	I/O	I1Z, OZ3	48	D09[1]	I/O	I1Z, OZ3	48	D09[1]	I/O	I1Z, OZ3
49	D10[1]	I/O	I1Z, OZ3	49	D10[1]	I/O	I1Z, OZ3	49	D10[1]	I/O	I1Z, OZ3
50	GND		Ground	50	GND		Ground	50	GND		Ground

Note: 1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2) The signal should be grounded by the host.
3) The signal should be tied to VCC by the host.
4) The mode is required for CompactFlash Storage Cards.
5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled upon the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.
6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal,including a floating condition
7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.
10) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active.
11) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active.
12) Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active.

Signal Description

Signal Name	Dir.	Pin	Description
A10 – A00 (PC Card Memory Mode) A10 – A00 (PC Card I/O Mode) A02 - A00 (True IDE Mode)	I I	8,10,11,12, 14,15,16,17, 18,19,20 18,19,20	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card , the memory mapped port address registers within the CompactFlash Storage Card, a byte in the card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, only A[02:00] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode) -STSCHG (PC Card I/O Mode) Status Changed -PDIAG (True IDE Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported. This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register. In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode) -SPKR (PC Card I/O Mode) -DASP (True IDE Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported. This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated. In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode) -CD1, -CD2 (PC Card I/O Mode) -CD1, -CD2 (True IDE Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Storage Card. They are used by the host to determine that the CompactFlash Storage Card is fully inserted into its socket. This signal is the same for all modes. This signal is the same for all modes.

Signal Name	Dir.	Pin	Description
-CE1, -CE2 (PC Card Memory Mode) Card Enable -CE1, -CE2 (PC Card I/O Mode) Card Enable -CS0, -CS1 (True IDE Mode)	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word.-CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0,-CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 27, Table 29, Table 31, Table 35, Table 36 and Table 37. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, -CS0 is the address range select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
-CSEL (PC Card Memory Mode) -CSEL (PC Card I/O Mode) -CSEL (True IDE Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode) D15 - D00 (PC Card I/O Mode) D15 - D00 (True IDE Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode) GND (PC Card I/O Mode) GND (True IDE Mode)	--	1,50	Ground. This signal is the same for all modes. This signal is the same for all modes.

Signal Name	Dir.	Pin	Description
-INPACK (PC Card Memory Mode except Ultra DMA Protocol Active) -INPACK (PC Card I/O Mode except Ultra DMA Protocol Active) Input Acknowledge -DMARQ (PC Card Memory Mode -Ultra DMA Protocol Active) -DMARQ (PC Card I/O Mode -Ultra DMA Protocol Active) DMARQ (True IDE Mode)	O	43	This signal is not used in this mode. The Input Acknowledge signal is asserted by the CompactFlash Storage Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card and the CPU. Hosts that support a single socket per interface logic, such as for Advanced Timing Modes and Ultra DMA operation may ignore the –INPACK signal from the device and manage their input buffers based solely on Card Enable signals. This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with (-)DMACK, i.e., the device shall wait until the host asserts (-)DMACK before negating (-)DMARQ, and re-asserting (-)DMARQ if there is more data to transfer. In PCMCIA I/O Mode, the -DMARQ shall be ignored by the host while the host is performing an I/O Read cycle to the device. The host shall not initiate an I/O Read cycle while -DMARQ is asserted by the device. In True IDE Mode, DMARQ shall not be driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 (-CE1)and -CS1 (-CE2) shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode operation. A host that does not support DMA mode and implements both PC Card and True IDE modes of operation need not alter the PC Card mode connections while in True IDE mode as long as this does not prevent proper operation in any mode.
-IORD (PC Card Memory Mode except Ultra DMA Protocol Active) -IORD (PC Card I/O Mode except Ultra DMA Protocol Active) -IORD (True IDE Mode – Except Ultra DMA Protocol Active) -HDMARDY (All Modes - Ultra DMA Protocol DMA Read) HSTROBE (All Modes - Ultra DMA Protocol DMA Write)	I	34	This signal is not used in this mode. This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card when the card is configured to use the I/O interface. In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode. In all modes when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate – HDMARDY to pause an Ultra DMA transfer. In all modes when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.

Signal Name	Dir.	Pin	Description
-IOWR (PC Card Memory Mode– Except Ultra DMA Protocol Active) -IOWR (PC Card I/O Mode –Except Ultra DMA Protocol Active) -IOWR (True IDE Mode – Except Ultra DMA Protocol Active) STOP (All Modes – Ultra DMA Protocol Active)	I	35	This signal is not used in this mode. The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card controller registers when the CompactFlash Storage Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge). In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol. In All Modes, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA data burst.
-OE (PC Card Memory Mode) -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode) -IREQ (PC Card I/O Mode) INTRQ (True IDE Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash Storage Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state. I/O Operation – After the CompactFlash Storage Card Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host.

Signal Name	Dir.	Pin	Description
-REG (PC Card Memory Mode– Except Ultra DMA Protocol Active) Attribute Memory Select -REG (PC Card I/O Mode –Except Ultra DMA Protocol Active)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. In PC Card Memory Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal negated during the execution of any DMA Command by the device. The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. In PC Card I/O Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal asserted during the execution of any DMA Command by the device.
-DMACK (PC Card Memory Mode when Ultra DMA Protocol Active) DMACK (PC Card I/O Mode when Ultra DMA Protocol Active) -DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to (-)DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the (-)DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PC Card and True-IDE modes of operation need not alter the PC Card mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
RESET (PC Card Memory Mode) RESET (PC Card I/O Mode) -RESET (True IDE Mode)	I	41	The CompactFlash Storage Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode) VCC (PC Card I/O Mode) VCC (True IDE Mode)	--	13,38	+5 V, +3.3 V power. This signal is the same for all modes. This signal is the same for all modes.

Signal Name	Dir.	Pin	Description
-VS1 -VS2 (PC Card Memory Mode) -VS1 -VS2 (PC Card I/O Mode) -VS1 -VS2 (True IDE Mode)	O	33 40	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Storage Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card. This signal is the same for all modes. This signal is the same for all modes.
-WAIT (PC Card Memory Mode – Except Ultra DMA Protocol Active) -WAIT (PC Card I/O Mode –Except Ultra DMA Protocol Active) IORDY (True IDE Mode – Except Ultra DMA Protocol Active) -DDMARDY (All Modes – Ultra DMA Write Protocol Active) DSTROBE (All Modes – Ultra DMA Read Protocol Active)	O	42	The -WAIT signal is driven low by the CompactFlash Storage Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer. In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.
-WE (PC Card Memory Mode) -WE (PC Card I/O Mode) -WE (True IDE Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect -IOIS16 (PC Card I/O Mode) -IOCS16 (True IDE Mode)	O	24	Memory Mode – The CompactFlash Storage Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O Operation – When the CompactFlash Storage Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

Electrical Specification

The following tables indicate all D.C. Characteristics for the CompactFlash Storage Card. Unless otherwise stated, conditions are:

Vcc = 5V ±10%

Vcc = 3.3V ± 5%

■ Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	Vcc	-0.3V min. to 6.5V max.
Voltage on any pin except Vcc with respect to GND.	V	-0.5V min. to Vcc + 0.5V max.

■ DC Characteristics

CompactFlash Interface I/O at 5.0V

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply Voltage	V_{CC}	4.5	5.5	V	
High level output voltage	V_{OH}	V_{CC} — 0.8		V	
Low level output voltage	V_{OL}		0.8	V	
High level input voltage	V_{IH}	4.0		V	Non-schmitt trigger
		2.92		V	Schmitt trigger[1]
Low level input voltage	V_{IL}		0.8	V	Non-schmitt trigger
			1.70	V	Schmitt trigger[1]
Pull up resistance[2]	R_{PU}	50	73	KOhm	
Pull down resistance	R_{PD}	50	97	KOhm	

CompactFlash Interface I/O at 3.3V

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply Voltage	V_{CC}	3.135	3.465	V	
High level output voltage	V_{OH}	V_{CC} — 0.8		V	
Low level output voltage	V_{OL}		0.8	V	
High level input voltage	V_{IH}	2.4		V	Non-schmitt trigger
		2.05		V	Schmitt trigger[1]
Low level input voltage	V_{IL}		0.6	V	Non-schmitt trigger
			1.25	V	Schmitt trigger[1]
Pull up resistance[2]	R_{PU}	52.7	141	KOhm	
Pull down resistance	R_{PD}	47.5	172	KOhm	

1. Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW pins
2. Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW, CSEL (P35), PDIAG, DASP pins

Input Power

Voltage	Maximum Average RMS Current	Measurement Method
3.3V ± 5%	75 mA (500 mA in Power Level 1)	3.3V at 25°C
5.0V ± 10%	100 mA (500 mA in Power Level 1)	5.0V at 25°C

Input Leakage Current

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
IxZ	Input Leakage Current	IL	Vih = Vcc / Vil = Gnd	-1		1	µA
IxU	Pull-Up Resistor	RPU1	Vcc = 5.0V	50k		500k	Ohm
IxD	Pull-Down Resistor	RPD1	Vcc = 5.0V	50k		500k	Ohm

Input Characteristics for UDMA mode >4

In UDMA modes greater than 4, the following characteristics apply. Voltage output high and low values shall be met at the source connector to include the effect of series termination.

Table: Input Characteristics (UDMA Mode > 4)

Parameter	Symbol	MIN	MAX	Units
DC supply voltage to drivers	V_{DD3}	3.3 –8%	3.3% + 8%	Volts
Low to high input threshold	V+	1.5	2.0	Volts
High to low input threshold	V-	1.0	1.5	Volts
Difference between input thresholds: $((V+_{current\ value}) - (V-_{current\ value}))$	V_{HYS}	320		Volts
Average of thresholds: $((V+_{current\ value}) + (V-_{current\ value}))/2$	V_{THRAVG}	1.3	1.7	Volts

Output Drive Type

Type	Output Type	Valid Conditions
OTx	Totempole	Ioh & Iol
OZx	Tri-State N-P Channel	Ioh & Iol
OPx	P-Channel Only	Ioh Only
ONx	N-Channel Only	Iol Only

Output Drive Characteristics for UDMA mode > 4

In UDMA modes greater than 4, the characteristics specified in the following table apply. Voltage output high and low values shall be met at the source connector to include the effect of series termination.

Table: Output Drive Characteristics (UDMA Mode > 4)

Parameter	Symbol	MIN	MAX	Units
DC supply voltage to drivers	V_{DD3}	3.3 –8%	3.3% + 8%	Volts
Voltage output high at -6 mA to +3 mA (at VoH2 the output shall be able to supply and sink current toVDD3)	V_{oH2}	V_{DD3}–0.51	V_{DD3}+0.3	Volts
Voltage output low at 6 mA	V_{oL2}		0.51	Volts

Notes:
1) I_{oLDASP} shall be 12 mA minimum to meet legacy timing and signal integrity.
2) I_{oH} value at 400 μA is insufficient in the case of DMARQ that is pulled low by a 5.6 kΩ resistor.
3) Voltage output high and low values shall be met at the source connector to include the effect of series termination.
4) A device shall have less than 64 μA of leakage current into a 6.2 KΩ pull-down resistor while the INTRQ signal is in the released state.

Signal Interface

Electrical specifications shall be maintained to ensure data reliability. Additional requirements are necessary for Advanced Timing Modes and Ultra DMA modes operations. See next sections for additional information.

Item	Signal	Card[10]	Host[10]
Control Signal	-CE1 -CE2 -REG -IORD -IOWR	Pull-up to V_{CC} 500 KΩ ≧ R≧ 50 KΩ and shall be sufficient to keep inputs inactive when the pins are not connected at the host.[1]	
	-OE -WE	Pull-up to V_{CC} 500 KΩ ≧ R ≧ 50 KΩ.[1,2]	
	RESET	Pull-up to V_{CC} 500 KΩ ≧ R ≧ 50 KΩ.[1,2,9,]	
Status Signal	READY -WAIT WP		Pull-up to V_{CC} R ≧ 10 KΩ.[3]
	-INPACK		In PCMCIA PC Card modes Pull-up to V_{CC} R ≧ 10 KΩ.[4] In True IDE mode, if DMA operation is supported by the host, Pull-down to Gnd R ≧ 5.6 KΩ.[5] PC Card / True IDE hosts switch the pull-up to pull down in True IDE mode if DMA operation is supported. The PC Card mode Pull-up may be left active during True IDE mode if True IDE DMA operation is not supported.
Address	A[10:00] -CSEL		
Data Bus	D[15:00]		[1.]
Card Detect	-CD[2:1]	Connected to GND in the card	
Voltage Sense	-VS1 -VS2		Pull-up to Vcc 10 KΩ ≦ R ≦100KΩ.
Battery/Detect	BVD[2:1]		Pull-up R ≧ 50 KΩ.[3.6]

Notes: 1) Control Signals: each card shall present a load to the socket no larger than 50 pF [10] at a DC current of 700 μA low state and 150 μA high state, including pull-resistor. The socket shall be able to drive at least the following load [10] while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (50 pF with DC current 700 μA low state and 150 μA high state per socket).

2) Resistor is optional.

3) Status Signals: the socket shall present a load to the card no larger than 50 pF [10] at a DC current of 400 μA low state and 100 μA high state, including pull-up resistor. The card shall be able to drive at least the following load [10] while meeting all AC timing requirements: 50 pF at a DC current of 400 μA low state and 100 μA high state.

4) Status Signals: the socket shall present a load to the card no larger than 50 pF [10] at a DC current of 400 μA low state and 100 μA high state, including pull-up resistor. The card shall be able to drive at least the following load [10] while meeting all AC timing requirements: 50 pF at a DC current of 400 μA low state and 100 μA high state.

5) Status Signals: the socket shall present a load to the card no larger than 50 pF [10] at a DC current of 400 μA low state and 100 μA high state, including pull-up resistor. The card shall be able to drive at least the following load [10] while meeting all AC timing requirements: 50 pF at a DC current of 400 μA low state and 1100 μA high state.

6) BVD2 was not defined in the JEIDA 3.0 release. Systems fully supporting JEIDA release 3 SRAM cards shall pull-up pin 45 (BVD2) to avoid sensing their batteries as “Low.”

7) Address Signals: each card shall present a load of no more than 100pF [10] at a DC current of 450 μA low state and 150 μA high state. The host shall be able to drive at least the following load [10] while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (100pF with DC current 450 μA low state and 150 μA high state per socket).

8) Data Signals: the host and each card shall present a load no larger than 50pF [10] at a DC current of 450 μA and 150 μA high state. The host and each card shall be able to drive at least the following load [10] while meeting all AC timing requirements: 100pF with DC current 1.6mA low state and 300 μA high state. This permits the host to wire two sockets in parallel without derating the card access speeds.

9) Reset Signal: This signal is pulled up to prevent the input from floating when a CFA to PCMCIA adapter is used in a PCMCIA revision 1 host. However, to minimize DC current drain through the pull-up resistor in normal operation the pull-up should be turned off once the Reset signal has been actively driven low by the host. Consequently, the input is specified as an I2Z because the resistor is not necessarily detectable in the input current leakage test.

10) Host and card restrictions for CF Advanced Timing Modes and Ultra DMA modes: Additional Requirements for CF Advanced Timing Modes and Ultra DMA Electrical Requirements for additional required limitations on the implementation of CF Advanced Timing modes and Ultra DMA modes respectively.

■ Additional Requirements for CF Advanced Timing Modes

The CF Advanced Timing modes include PC Card I/O and Memory modes that are 100ns or faster, PC Card Ultra DMA modes 3 or above and True IDE PIO Modes 5,6, Multiword DMA Modes 3,4 and True IDE Ultra DMA modes 3 or above.

When operating in CF Advanced timing modes, the host shall conform to the following requirements:

1) Only one CF device shall be attached to the CF Bus.

2) The host shall not present a load of more than 40pF to the device for all signals, including any cabling.

3) The maximum cable length is 0.15 m (6 in). The cable length is measured from the card connector to the host controller. 0.46 m (18 in) cables are *not* supported.

4) The -WAIT and IORDY signals shall be ignored by the host.

Devices supporting CF Advanced timing modes shall also support slower timing modes, to ensure operability with systems that do not support CF Advanced timing modes

Ultra DMA Electrical Requirements

- **Host and Card signal capacitance limits for Ultra DMA operation**
  The host interface signal capacitance at the host connector shall be a maximum of 25 pF for each signal as measured at 1 MHz.

  The card interface signal capacitance at the card connector shall be a maximum of 20 pF for each signal as measured at 1 MHz.

- **Series termination required for Ultra DMA operation**
  Series termination resistors are required at both the host and the card for operation in any of the Ultra DMA modes. Table describes typical values for series termination at the host and the device.

Table: Typical Series Termination for Ultra DMA

Signal	Host Termination	Device Termination
-IORD (-HDMARDY,HSTROBE)	22 ohm	82 ohm
-IOWR (STOP)	22 ohm	82 ohm
-CS0, -CS1	33 ohm	82 ohm
A00, A01, A02	33 ohm	82 ohm
-DMACK	22 ohm	82 ohm
D15 through D00	33 ohm	33 ohm
DMARQ	82 ohm	22 ohm
INTRQ	82 ohm	22 ohm
IORDY (-DDMARDY, DSTROBE)	82 ohm	22 ohm
-RESET	33 ohm	82 ohm
NOTE – Only those signals requiring termination are listed in this table. If a signal is not listed, series termination is not required for operation in an Ultra DMA mode. Shows signals also requiring a pull-up or pull-down resistor at the host. The actual termination values should be selected to compensate for transceiver and trace impedance to match the characteristic cable impedance.		

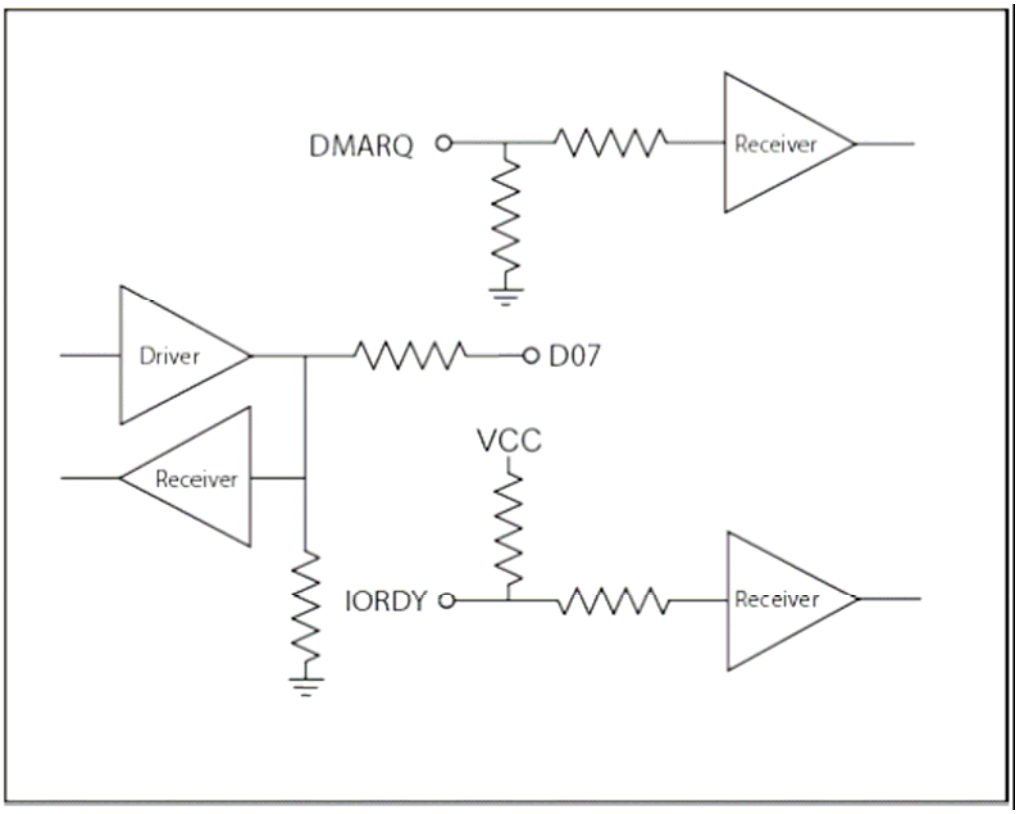


Table: Ultra DMA Termination with Pull-up or Pull down Example

- **Printed Circuit Board (PCB) Trace Requirements for Ultra DMA**

  On any PCB for a host or device supporting Ultra DMA:

  - ✓ The longest D[15:00] trace shall be no more than 0.5" longer than either STROBE trace as measured from the IC pin to the connector.
  - ✓ The shortest D[15:00] trace shall be no more than 0.5" shorter than either STROBE trace as measured from the IC pin to the connector.

- **Ultra DMA Mode Cabling Requirement**

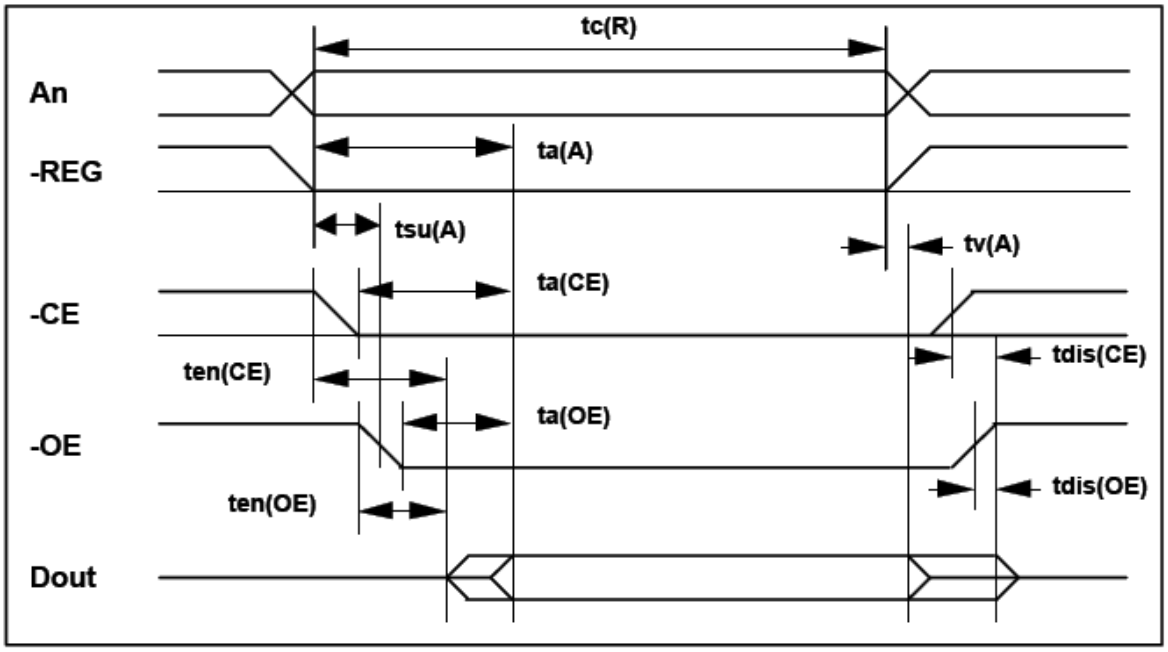
  - ✓ Operation in Ultra DMA mode requires a crosstalk suppressing cable. The cable shall have a grounded line between each signal line.
  - ✓ For True IDE mode operation using a cable with IDE (ATA) type 40 pin connectors it is recommended that the host sense the cable type using the method described in the ANSI INCITS 361-2002 AT Attachment - 6 standard, to prevent use of Ultra DMA with a 40 conductor cable.

■ Attribute Memory Read Timing Specification

Attribute Memory access time is defined as 300 ns. Detailed timing specs are shown in Table below

Speed Version			300 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVGL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

Note: All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card to the system. The -CE signal or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations.



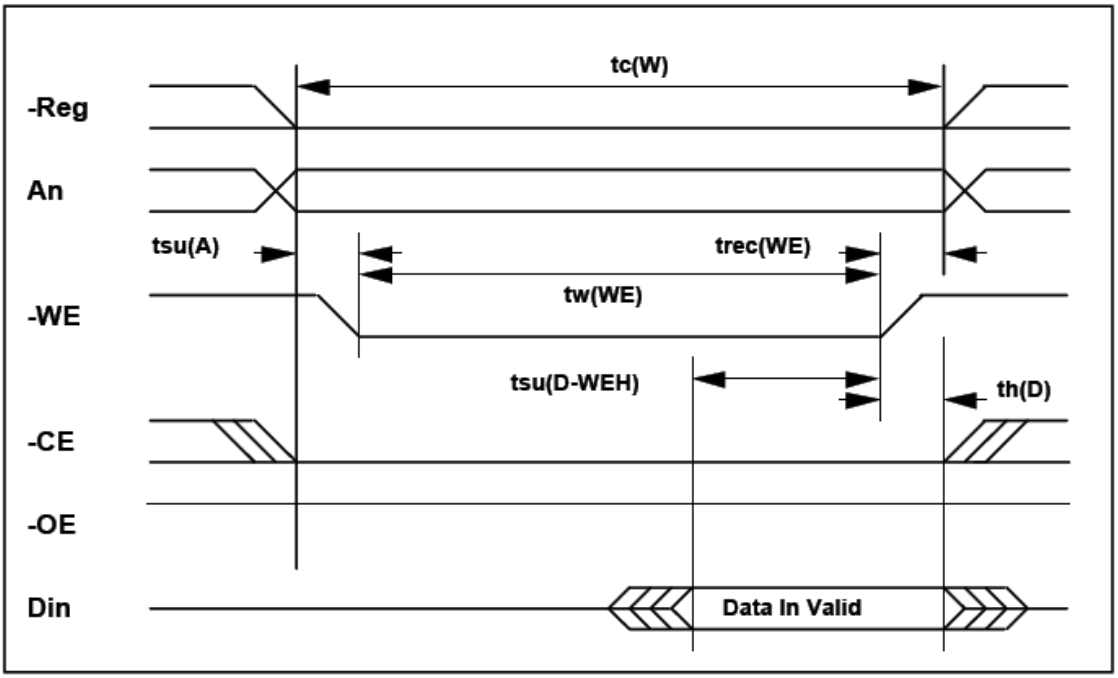
■ Configuration Register (Attribute Memory) Write Timing Specification

The Card Configuration write access time is defined as 250 ns. Detailed timing specifications are shown in Table below.

Table: Configuration Register (Attribute Memory) Write Timing

Speed Version			250 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns**	**Max ns**
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

Note: All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card .

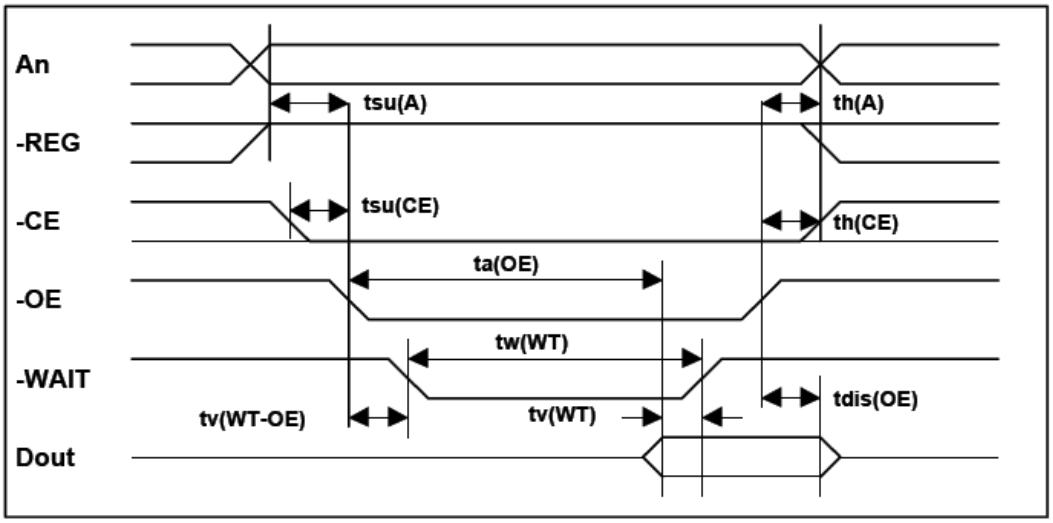


Common Memory Read Timing Specification

		Cycle Time Mode:	250 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35		35		35		na[1]
Data Setup for Wait Release	tv(WT)	tQVWTH		0		0		0		na[1]
Wait Width Time[2]	tw(WT)	tWTLWTH		350		350		350		na[1]

Notes:1) –WAIT is not supported in this mode.

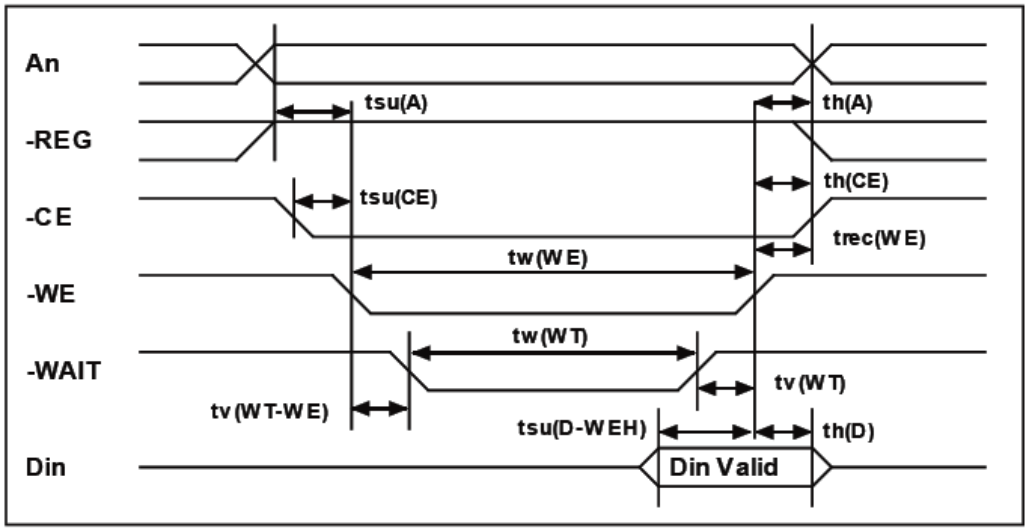
2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA PC Card specification of 12μs but is intentionally less in this specification.



Common Memory Write Timing Specification

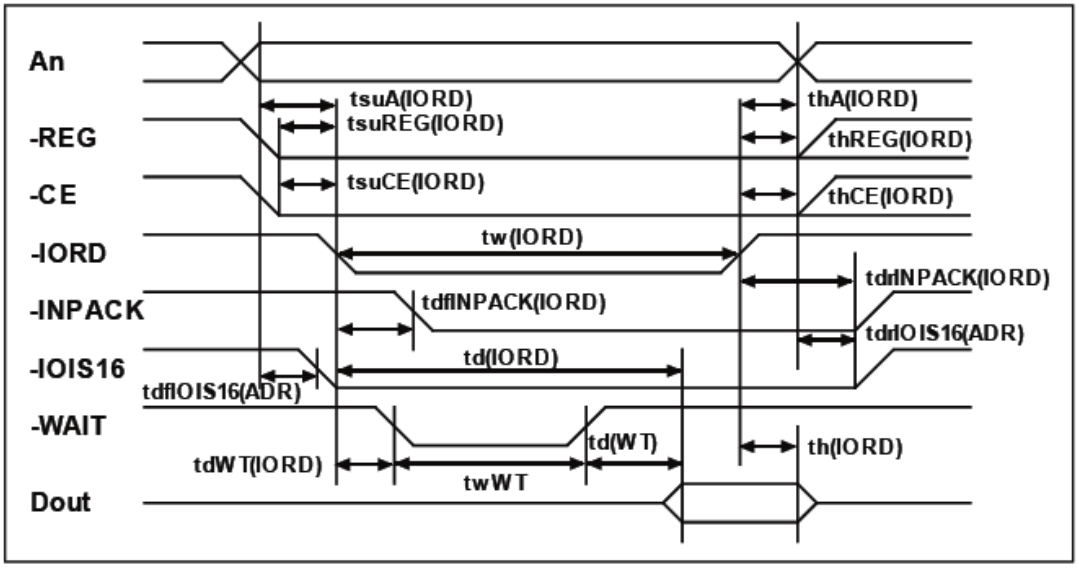
		Cycle Time Mode:	250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before WE	tsu (D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from WE	tv (WT-WE)	tWLWTV		35		35		35		na[1]
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		na[1]	
Wait Width Time[2]	tw (WT)	tWTLWTH		350		350		350		na[1]

Notes: 1) –WAIT is not supported in this mode.
2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA PC Card specification of 12μs but is intentionally less in this specification.



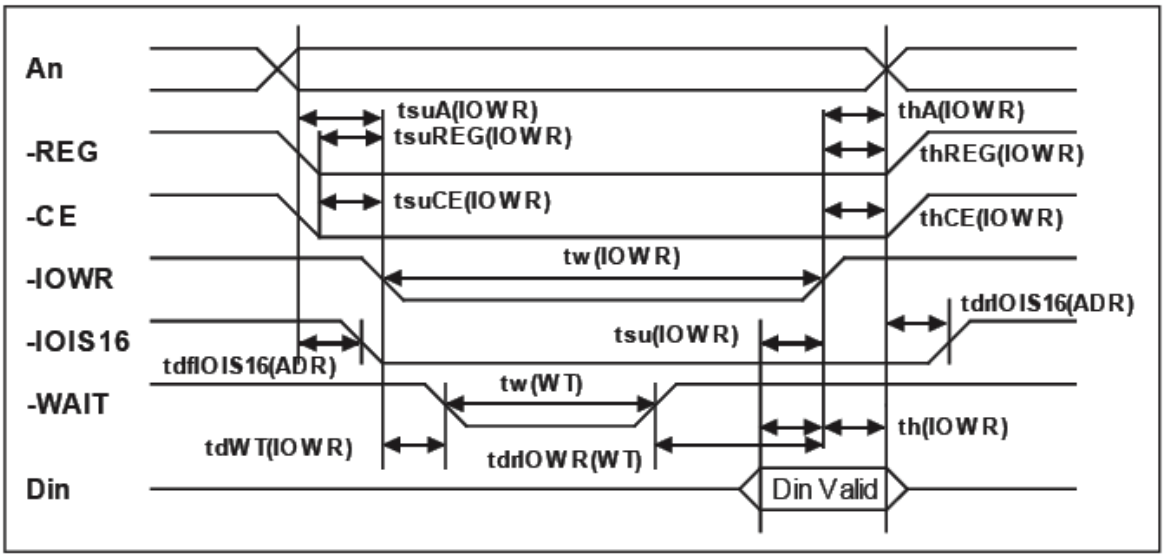
■ I/O Input (Read) Timing Specification

		Cycle Time Mode:	250 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG Setup before IORD	tsuREG (IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG (IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD[3]	tdfINPACK (IORD)	tIGLIAL	0	45	0	na[1]	0	na[1]	0	na[1]
INPACK Delay Rising from IORD[3]	tdrINPACK (IORD)	tIGHIAH		45		na[1]		na[1]		na[1]
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IORD[3]	tdWT(IORD)	tIGLWTL		35		35		35		na[2]
Data Delay from Wait Rising[3]	td(WT)	tWTHQV		0		0		0		na[2]
Wait Width Time3	tw(WT)	tWTLWTH		350		350		350		na[2]



■ I/O Output (Write) Timing Specification

		Cycle Time Mode:	255 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tIWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE (IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE (IOWR)	tIWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG (IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG (IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IOWR[3]	tdWT(IOWR)	tIWLWTL		35		35		35		na[2]
IOWR high from Wait high[3]	tdrIOWR (WT)	tWTJIWH	0		0		0		na[2]	
Wait Width Time[3]	tw(WT)	tWTLWTH		350		350		350		na[2]



■ True IDE PIO Mode Read/Write Timing Specification

	Item	Mode							Note
		0	1	2	3	4	5	6	
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	1
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data hold (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
T6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	4
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	na[5]	na[5]	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na[5]	na[5]	
tC	IORDY assertion to release (max)	5	5	5	5	5	na[5]	na[5]	

Notes: All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

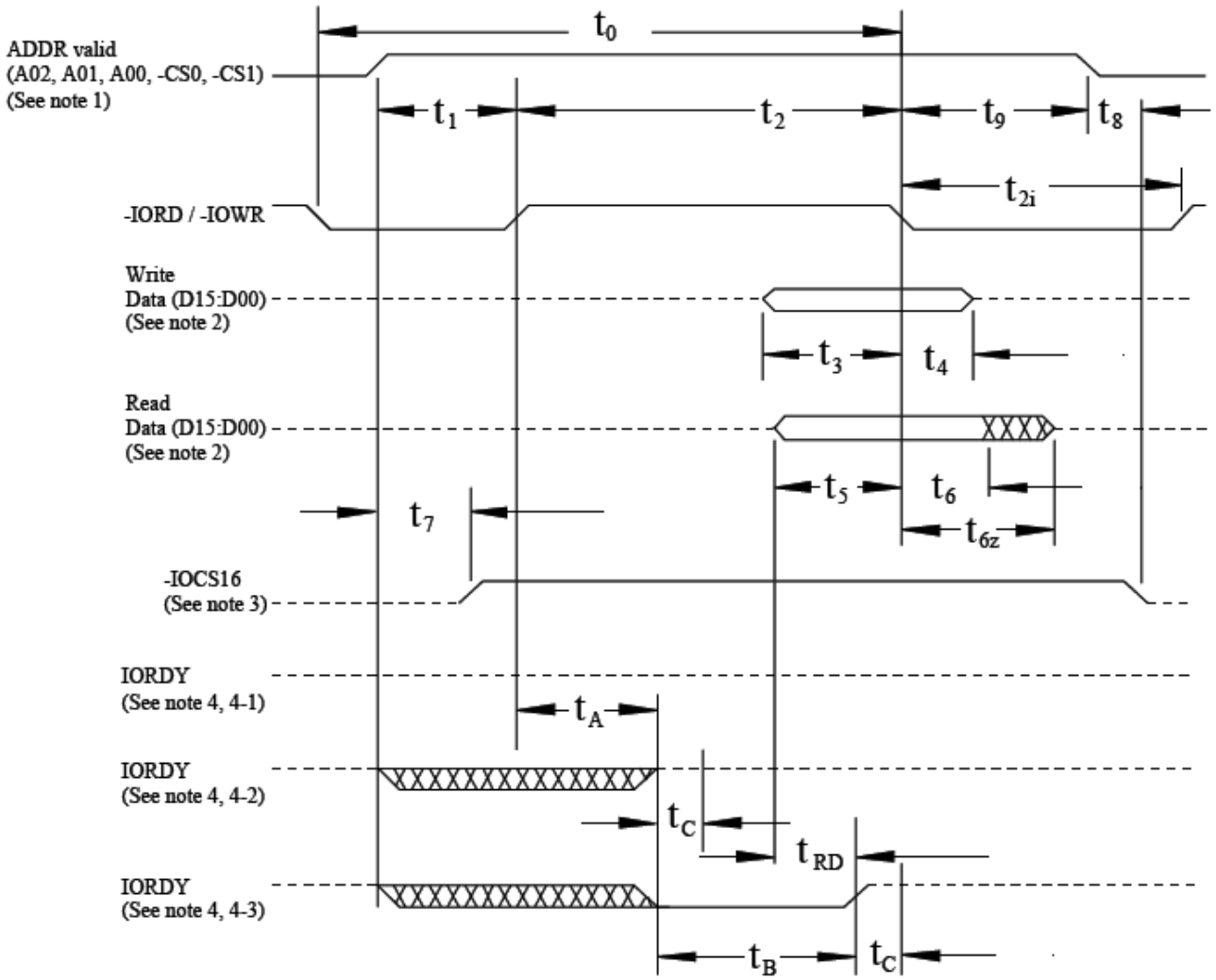
1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

2) This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).

3) The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.

4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.

5) IORDY is not supported in this mode.



Notes:

(1) Device address consists of -CS0, -CS1, and A[02::00]

(2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)

(3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.

(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:

(4-1) Device never negates IORDY: No wait is generated.

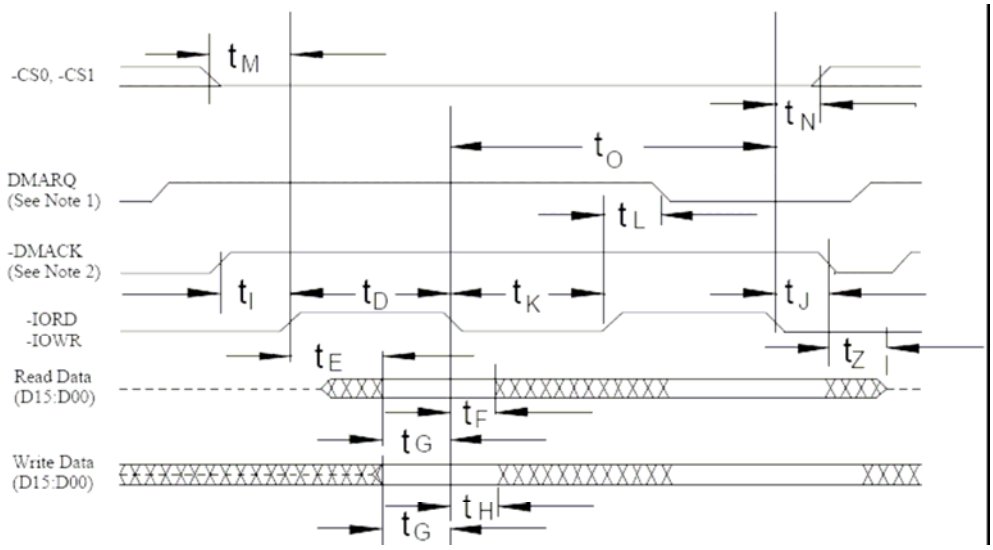
(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.

(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

■ True IDE Multiword DMA Mode Read/Write Timing Specification

The timing diagram for True IDE DMA mode of operation in this section is drawn using the conventions in the ATA-4 specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the -IORD, the -IOWR and the -IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	Note
t_O	Cycle time (min)	480	150	120	100	80	1
t_D	-IORD / -IOWR asserted width (min)	215	80	70	65	55	1
t_E	-IORD data access (max)	150	60	50	50	45	
t_F	-IORD data hold (min)	5	5	5	5	5	
t_G	-IORD/-IOWR data setup (min)	100	30	20	15	10	
t_H	-IOWR data hold (min)	20	15	10	5	5	
t_I	DMACK to –IORD/-IOWR setup (min)	0	0	0	0	0	
t_J	-IORD / -IOWR to -DMACK hold (min)	20	5	5	5	5	
t_{KR}	-IORD negated width (min)	50	50	25	25	20	1
t_{KW}	-IOWR negated width (min)	215	50	25	25	20	1
t_{LR}	-IORD to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35	
t_M	CS(1:0) valid to –IORD / -IOWR	50	30	25	10	5	
t_N	CS(1:0) hold	15	10	10	10	10	
t_Z	-DMACK	20	25	25	25	25	



■ True IDE Ultra DMA Mode Read/Write Timing Specification

Ultra DMA operations can take place in any of the three basic interface modes: PC Card Memory mode, PC Card I/O mode, and True IDE (the original mode to support UDMA). The usage of signals in each of the modes is shown in Table 24:Ultra DMA Signal Usage In Each Interface Mode

UDMA Signal	Type	Pin # (Non UDMA MEM MODE)	PC CARD MEM MODE UDMA	PC CARD IO MODE UDMA	TRUE IDE MODE UDMA
DMARQ	Output	43 (-INPACK)	-DMARQ	-DMARQ	DMARQ
DMACK	Input	44 (-REG)	-DMACK	DMACK	-DMACK
STOP	Input	35 (-IOWR)	STOP 1	STOP 1	STOP 1
HDMARDY(R) HSTROBE(W)	Input	34 (-IORD)	-HDMARDY(R) [1] 2HSTROBE(W) [1, 3, 4]	-HDMARDY(R) [1, 2] HSTROBE(W) [1, 3, 4]	-HDMARDY(R) [1, 2] HSTROBE(W) [1, 3, 4]
DDMARDY(W) DSTROBE(R)	Output	42 (-WAIT)	-DDMARDY(W) [1, 3] DSTROBE(R) [1. 2. 4]	-DDMARDY(W) [1, 3] DSTROBE(R) [1. 2. 4]	-DDMARDY(W) [1, 3] DSTROBE(R) [1. 2. 4]
DATA	Bidir	… (D[15:00])	D[15:00]	D[15:00]	D[15:00]
ADDRESS	Input	… (A[10:00])	A[10:00]	A[10:00]	A[02:00] 5
CSEL	Input	39 (-CSEL)	-CSEL	-CSEL	-CSEL
INTRQ	Output	37 (READY)	READY	-INTRQ	INTRQ
Card Select	Input	7 (-CE1) 31 (-CE2)	-CE1 -CE2	-CE1 -CE2	-CS0 -CS1

Notes:1) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.
2) The UDMA interpretation of this signal is valid only during and Ultra DMA data burst during a DMA Read command.
3) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.
4) The HSTROBE and DSTROBE signals are active on both the rising and the falling edge.
5) Address lines 03 through 10 are not used in True IDE mode.

Several signal lines are redefined to provide different functions during an Ultra DMA data burst. These lines assume their UDMA definitions when:

1 an Ultra DMA mode is selected, and
2 a host issues a READ DMA, or a WRITE DMA command requiring data transfer, and
3 the device asserts (-)DMARQ, and
4 the host asserts (-)DMACK.

These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of -DMACK by the host at the termination of an Ultra DMA data burst.

With the Ultra DMA protocol, the STROBE signal that latches data from D[15:00] is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of D[15:00] and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst.

During an Ultra DMA data burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data.

Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to

select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied. Devices supporting any Ultra DMA mode shall also support all slower Ultra DMA modes.

An Ultra DMA capable device shall retain the previously selected Ultra DMA mode after executing a software reset sequence or the sequence caused by receipt of a DEVICE RESET command if a SET FEATURES disable reverting to defaults command has been issued. The device may revert to a Multiword DMA mode if a SET FEATURES enable reverting to default has been issued. An Ultra DMA capable device shall clear any previously selected Ultra DMA mode and revert to the default non-Ultra DMA modes after executing a power-on or hardware reset.

Both the host and device perform a CRC function during an Ultra DMA data burst. At the end of an Ultra DMA data burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA data bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.

NOTE -If a data transfer is terminated before completion, the assertion of INTRQ should be passed through to the host software driver regardless of whether all data requested by the command has been transferred.

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		UDMA Mode 5		Measure location (see Note 2)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		40		Sender
t_{CYC}	112		73		54		39		25		16.8		Note 3
t_{2CYC}	230		153		115		86		57		38		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		Host
t_{ZFS}	0		0		0		0		0		35		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		Sender
t_{FS}		230		200		170		130		120		90	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	Note 4
t_{MLI}	20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	Host
t_{RFS}		75		70		60		60		60		50	Sender
t_{RP}	160		125		100		100		100		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		Sender

Notes:

1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and –DMARDY transitions are measured at the sender connector.
3) The parameter tCYC shall be measured at the recipient's connector farthest from the sender.
4) The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an

incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5) The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround.

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	6
t_{ZIORDY}	Minimum time before driving IORDY	4, 6
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes: 1) The parameters tUI, tMLI : (Ultra DMA Data-In Burst Device Termination Timing and Ultra DMA Data-In Burst Host Termination Timing), and tLI indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. tUI is an unlimited interlock that has no maximum time value. tMLI is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum.

2) 80-conductor cabling shall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes greater than 2.

3) Timing for tDVS, tDVH, tCVS and tCVH shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

4)For all modes the parameter tZIORDY may be greater than tENV due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

5)The parameters tDS, and tDH for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for tDS and tDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode4 (ns)		UDMA Mode 5 (ns)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	14.7		9.7		6.8		6.8		4.8		2.3	
t_{DHIC}	4.8		4.8		4.8		4.8		4.8		2.8	
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5		6.0	
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0		6.0	
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)											
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)											
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)											
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)											

Notes: 1) All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V.

2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V).

2) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
SRISE	Rising Edge Slew Rate for any signal		1.25	1
SFALL	Falling Edge Slew Rate for any signal		1.25	1

Note: 1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

Card Configuration

The CompactFlash Storage Cards is identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the CompactFlash Storage Card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

■ Multiple Function CompactFlash Storage Cards

Table: CompactFlash Storage Card Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby and UDMA transfer
X	0	0	0	1	0	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	0	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Table: **PC Card Memory Mode UDMA Function**

-CE2	-CE1	-DMARQ -INPACK	-DMACK -REG	STOP -IOW R	-DMARDY -IORD (R)-WAIT (W)	STROBE -WAIT (R)-IORD (W)	DMA CMD	A10-A00	Operation
1	1	1	X	X	X	X	No	XX	Standby
X	X	0	1	X	X	1	YES	XX	Device UDMA Transfer Request (Assert DMARQ)
X	X	0	1	1	X	1	YES	XX	Host Acknowledge Preparation
1	1	0	1	1	1	1	YES	Static	Host Acknowledge Preparation
1	1	0	0	1	1	1	YES	Static	DMA Acknowledge (Stopped)
1	1	0	0	0	0	1	YES	Static	Burst Initiation / Active
1	1	0	0	0	X	/ or \	YES	Static	Burst Transfer
1	1	0	0	0	1	0 or 1	RD	Static	Data In Burst Host Pause
1	1	0	0	0	0	0 or 1	RD	Static	Data In Burst Device Pause
1	1	0	0	0	1	0 or 1	WR	Static	Data Out Burst Device Pause
1	1	0	0	0	0	0 or 1	WR	Static	Data Out Burst Host Pause
1	1	1	0	0	0	0 or 1	RD	Static	Device Initiating BurstTermination
1	1	1	0	1	1	0 or 1	RD	Static	Host Acknowledement of Device Initiated Burst Termination
1	1	0	0	1	0	0 or 1	YES	Static	Host Initiating BurstTermination
1	1	1	0	1	1	0 or 1	YES	Static	Device Acknowledging Host Initiated Burst Termination
1	1	1	0	1	1	/	YES	Static	Device Aligning STROBE to Asserted before CRC Transfer
1	1	1	/	1	1	1	YES	Static	CRC Data Transfer for UDMA Burst
1	1	1	1	1	1	1	YES	Static	Burst Completed

Table: CompactFlash Storage Card Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED REGISTER
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Attribute Memory Function

Attribute memory is a space where CompactFlash Storage Card identification and configuration information are stored, and is limited to 8 bit wide accesses only at even addresses. The card configuration registers are also located here. For CompactFlash Storage Cards, the base address of the Card configuration registers is 200h.

Table: Attribute Memory Function

Function Mode	DMA CMD	-REG	-CE2	-CE1	A10	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	Don't Care	H	H	H	X	X	X	X	X	High Z	High Z
Standby Mode	No	X	H	H	X	X	X	X	X	High Z	High Z
UDMA Operation (see section 4.3.18: Ultra DMA Mode Read/Write Timing Specification)	Yes	L[1]	H	H	X	X	X	H	H	Odd Byte	Even Byte
Read Byte Access CIS ROM (8 bits)	No	L	H	L[2]	L	L	L	L[2]	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	No	L	H	L[2]	L	L	L	H	L[2]	Don't Care	Even Byte
Read Byte Access Configuration CompactFlash Storage (8 bits)	No	L	H	L	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration CompactFlash Storage (8 bits)	No	L	H	L	L	H	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	No	L	L[2]	L[2]	L	L	X	L[2]	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	No	L	L[2]	L[2]	L	L	X	H	L[2]	Don't Care	Even Byte
Read Word Access Configuration CompactFlash Storage (16 bits)	No	L	L[2]	L[2]	L	H	X	L[2]	H	Not Valid	Even Byte
Write Word Access Configuration CompactFlash Storage (16 bits)	No	L	L[2]	L[2]	L	H	X	H	L[2]	Don't Care	Even Byte

■ Configuration Option Register (Base + 00h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the CompactFlash Storage Card or CF+ Card.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Configuration Option Register

SRESET - Soft Reset: setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the CompactFlash Storage Card or CF+ Card in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the CompactFlash Storage Card or CF+ Card in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. For CompactFlash Storage Cards, using the PCMCIA Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

LevlREQ: this bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

Conf5 - Conf0 - Configuration Index: set to zero (0) by reset. It is used to select operation mode of the CompactFlash Storage Card or CF+ Card as shown below.

Note: Conf5 and Conf4 are reserved for CompactFlash Storage cards and shall be written as zero (0). These bits are vendor defined for CF+ Cards.

CompactFlash Storage Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0h-1F7h/3F6h-3F7h
0	0	0	0	1	1	I/O Mapped, 170h-177h/376h-377h

CF+ Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	CF+ Card Mode
0	0	0	0	0	0	Memory Mapped, I/O cycles are ignored
X	X	X	X	X	X	Any non-zero value, vendor defined

■ Card Configuration and Status Register (Base + 02h in Attribute Memory)

The Card Configuration and Status Register contains information about the Card's condition.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	-XE	Audio	PwrDwn	Int	0
Write	0	SigChg	IOis8	-XE	Audio	PwrDwn	0	0

Card Configuration and Status Register

Changed: indicates that one or both of the Pin Replacement register CReady, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the CompactFlash Storage Card or CF+ Card is configured for the I/O interface.

SigChg: this bit is set and reset by the host to enable and disable a state-change "signal" from the Status Register, the Changed bit controls pin 46, the Changed Status signal. If no state change signal is desired, this bit is set to zero (0) and pin 46 (-STSCHG) signal is then held high while the CompactFlash Storage Card or CF+ Card is configured for I/O.

IOis8: the host sets this bit to a one (1) if the CompactFlash Storage Card or CF+ Card is to be configured in an 8 bit I/O Mode. The CompactFlash Storage Card is always configured for both 8 and 16 bit I/O, so this bit is ignored. Some CF+ cards can be configured for either 8 bit I/O mode or 16 bit I/O mode, so CF+ cards may respond to this bit.

-XE: this bit is set and reset by the host to disable and enable Power Level 1 commands in CF+ cards. If the value is 0, Power Level 1 commands are enabled; if it is 1, Power Level 1 commands are disabled. Default value at power on or after reset is 0. The host may read the value of this bit to determine whether Power Level 1 commands are currently enabled. For CompactFlash cards that do not support Power Level 1, this bit has value 0 and is not writeable.

Audio: this bit is set and reset by the host to enable and disable audio information on -SPKR when the CF+ card is configured. This bit should always be zero for CompactFlash Storage cards.

PwrDwn: this bit indicates whether the host requests the CompactFlash Storage Card or CF+ Card to be in the power saving or active mode. When the bit is one (1), the CompactFlash Storage Card or CF+ Card enters a power down mode. When PwrDwn is zero (0), the host is requesting the CompactFlash Storage Card or CF+ Card to enter the active mode. The PCMCIA READY value becomes false (busy) when this bit is changed. READY shall not become true (ready) until the power state requested has been entered. The CompactFlash Storage Card automatically powers down when it is idle and powers back up when it receives a command.

Int: this bit represents the internal state of the interrupt request. This value is available whether or not the I/O interface has been configured. This signal remains true until the condition that caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

■ Pin Replacement Register (Base + 04h in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CReady	CWProt	1	1	RReady	WProt
Write	0	0	CReady	CWProt	0	0	MReady	MWProt

Pin Replacement Register

CReady: this bit is set to one (1) when the bit RReady changes state. This bit can also be written by the host.

CWProt: this bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

RReady: this bit is used to determine the internal state of the READY signal. This bit may be used to determine the state of the READY signal as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask (MReady) for writing the corresponding bit CReady.

WProt: this bit is always zero (0) since the CompactFlash Storage Card or CF+ Card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

MReady: this bit acts as a mask for writing the corresponding bit CReady.

MWProt: this bit when written acts as a mask for writing the corresponding bit CWProt.

Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final "C" Bit	Comments
	"C" Bit	"M" Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

Socket and Copy Register (Base + 06h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register. This register is not required for CF or CF+ Cards.

If present, it is optional for a CF Card to allow setting bit D4 (Drive number) to 1. If two drives are supported, it is intended for use only when two cards are co-located at either the primary or secondary addresses in PCMCIA I/O mode. The availability and capabilities of this register are described in the Card Information Structure of the CF Card.

Hosts shall not depend on the availability of this functionality.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Obsolete[1] (Drive #)	0	0	0	0
Write	0	0	0	Obsolete[1] (Drive #)	X	X	X	X

Socket and Copy Register

Reserved: this bit is reserved for future standardization. This bit shall be set to zero (0) by the software when the register is written.

Obsolete (Drive #): this bit is obsolete and should be written as 0.

If the obsolete functionality is not supported it shall be read as written or shall be read as 0. If the obsolete functionality is supported, the bit shall be read as written. If supported, this bit sets the drive number, which the card matches with the DRV bit of the Drive/Head register when configured in a twin card configuration.

It is recommended that the host always write 0 for the drive number in this register and in the DRV bit of the Drive/Head register for PCMCIA modes of operation.

X: the socket number is ignored by the CompactFlash Storage Card.

I/O Transfer Function

The I/O transfer to or from the CompactFlash Storage can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Storage. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Storage, the system shall generate a pair of 8 bit references to access the word‘s even byte and odd byte. The CompactFlash Storage Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Storage responds. The CompactFlash Storage Card may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table: PCMCIA Mode I/O Function

Function Code	DMA CMD	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	No	X	H	H	X	X	X	High Z	High Z
UDMA Write	Write	H	H	H	X	X	X	Odd Byte	Even Byte
UDMA Read	Read	H	H	H	X	X	X	Odd Byte	Even Byte
Byte Input Access (8 bits)	X	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	X	L L	H H	L L	L H	H H	L L	Don’t Care Don’t Care	Even-Byte Odd-Byte
Word Input Access (16 bits)	X	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	X	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	X	H	X	X	X	L	H	Don’t Care	Don’t Care
I/O Write Inhibit	X	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	X	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	X	L	L	H	X	H	L	Odd-Byte	Don’t Care

Table: PC Card I/O Mode UDMA Function

-CE2	-CE1	-DMARQ -INPACK	DMACK -REG	STOP -IOWR	-DMARDY -IORD (R)-WAIT (W)	STROBE -WAIT (R)-IORD (W)	DMA CMD	A10-A00	Operation
1	1	1	X	X	X	X	No	XX	Standby
X	X	0	0	X	X	1	YES	XX	Device UDMA Transfer Request (Assert DMARQ)
X	X	0	0	1	X	1	YES	XX	Host Acknowledge Preparation
1	1	0	0	1	1	1	YES	Static	Host Acknowledge Preparation
1	1	0	1	1	1	1	YES	Static	DMA Acknowledge (Stopped)
1	1	0	1	0	0	1	YES	Static	Burst Initiation / Active
1	1	0	1	0	X	/ or \	YES	Static	Burst Transfer
1	1	0	1	0	1	0 or 1	RD	Static	Data In Burst Host Pause
1	1	0	1	0	0	0 or 1	RD	Static	Data In Burst Device Pause
1	1	0	1	0	1	0 or 1	WR	Static	Data Out Burst Device Pause
1	1	0	1	0	0	0 or 1	WR	Static	Data Out Burst Host Pause
1	1	1	1	0	0	0 or 1	RD	Static	Device Initiating BurstTermination
1	1	1	1	1	1	0 or 1	RD	Static	Host Acknowledement of Device Initiated Burst Termination
1	1	0	1	1	0	0 or 1	YES	Static	Host Initiating BurstTermination
1	1	1	1	1	1	0 or 1	YES	Static	Device Acknowledging Host Initiated Burst Termination
1	1	1	1	1	1	/	YES	Static	Device Aligning STROBE to Asserted before CRC Transfer
1	1	1	\	1	1	1	YES	Static	CRC Data Transfer for UDMA Burst
1	1	1	0	1	1	1	YES	Static	Burst Completed

Common Memory Transfer Function

The Common Memory transfer to or from the CompactFlash Storage can be either 8 or 16 bits.

Table: Common Memory Function

Function Code	DMA	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	None	X	H	H	X	X	X	High Z	High Z
Byte Read (8 bits)	Don't Care	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write (8 bits)	Don't Care	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Read (16 bits)	Don't Care	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write (16 bits)	Don't Care	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	Don't Care	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	Don't Care	H	L	H	X	H	L	Odd-Byte	Don't Care
Ultra DMA Write	Write	L	H	H	X	H	H	Odd-Byte	Even-Byte
Ultra DMA Read	Read	L	H	H	X	H	H	Odd-Byte	Even-Byte

True IDE Mode I/O Transfer Function

The CompactFlash Storage Card can be configured in a True IDE Mode of operation. The CompactFlash Storage Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. Optionally, CompactFlash Storage Cards may support the following optional detection methods:
1. The card is permitted to monitor the –OE (-ATA SEL) signal at any time(s) and switch to PCMCIA mode upon detecting a high level on the pin.
2. The card is permitted to re-arbitrate the interface mode determination following a transition of the (-)RESET pin.
3. The card is permitted to monitor the –OE (-ATA SEL) signal at any time(s) and switch to True IDE mode upon detection of a continuous low level on pin for an extended period of time.

Table: True IDE Mode I/O Function defines the function of the operations for the True IDE Mode.

Function Code	-CS1	-CS0	A0-A2	-DMACK	-IORD	-IOWR	D15-D8	D7-D0
Invalid Modes	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined In	Undefined In
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined In	Undefined In
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	H	L	H	High Z	Data Out
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte In	Even-Byte In
DMA Data Register Write	H	H	X	L	H	L	Odd-Byte In	Even-Byte In
Ultra DMA Data Register Write	H	H	X	L	See Note 2		Odd-Byte In	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Ultra DMA Data Register Read	H	H	X	L	See Note 3		Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address[1]	L	H	7h	H	L	H	High Z	Data Out

Host Configuration Requirements for Master/Slave or New Timing Modes

The CF Advanced Timing modes include PCMCIA PC Card style I/O modes that are faster than the original 250 ns cycle time. These modes are not supported by the PCMCIA PC Card specification nor CF by cards based on revisions of the CF specification before Revision 3.0. Hosts shall ensure that all cards accessed through a common electrical interface are capable of operation at the desired, faster than 250 ns, I/O mode before configuring the interface for that I/O mode.

Advanced Timing modes are PCMCIA PC Card style I/O modes that are 100 ns or faster, PC Card Memory modes that are 100ns or faster, True IDE PIO Modes 5,6 and Multiword DMA Modes 3,4. These modes are permitted to be used only when a single card is present and the host and card are connected directly, without a cable exceeding 0.15m in length. Consequently, the host shall not configure a card into an Advanced Timing Mode if two cards are sharing I/O lines, as in Master/Slave operation, nor if it is constructed such that a cable exceeding 0.15 meters is required to connect the host to the card.

The load presented to the Host by cards supporting Ultra DMA is more controlled than that presented by other CompactFlash cards. Therefore, the use of a card that does not support Ultra DMA in a Master/Slave arrangement with a Ultra DMA card can affect the critical timing of the Ultra DMA transfers. The host shall not configure a card into Ultra DMA mode when a card not supporting Ultra DMA is also present on the same interface

When the use of two cards on an interface is otherwise permitted, the host may use any mode that is supported by both cards, but to achieve maximum performance it should use its highest performance mode that is also supported by both cards.

Metaformat Overview

The goal of the Metaformat is to describe the requirements and capabilities of the CompactFlash Storage Card as thoroughly as possible. This includes describing the power requirements, IO requirements, memory requirements, manufacturer information and details about the services provided.

Table: Sample Device Info Tuple Information for Extended Speeds

Speed	Attribute Memory Relative Offset	Code	D7	D6	D5	D4	D3	D2	D1	D0	Notes
250	N+0	D9h	Dh = Function Specific				1	1h = 250 nsec			PCMCIA Std
120	N+0	DFh	Dh = Function Specific				1	7h = Extended			CFA Defined
	N+2	12h	0	2h = 1.2				2h = * 100 nsec			
100	N+0	DCh	Dh = Function Specific				1	4h = 100 nsec			PCMCIA
80	N+0	DFh	Dh = Function Specific				1	7h = Extended			CFA Defined
	N+2	79h	0	Fh = 8.0				1h = * 10 nsec			

Note: The value "1" defined for D3 of the N+0 words indicates that no write-protect switch controls writing the ATA registers. The value "0" defined for D7 in the N+2 words indicates that there is not more than a single speed extension byte.

CF-ATA Drive Register Set Definition and Protocol

The CompactFlash Storage Card can be configured as a high performance I/O device through:

a) The standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary) or 170h- 177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).

b) Any system decoded 16 byte I/O block using any available IRQ.

c) Memory space.

The communication to or from the CompactFlash Storage Card is done using the Task File registers, which provide all the necessary registers for control and status information related to the storage medium. The PCMCIA interface connects peripherals to the host using four register mapping methods. Table 39 is a detailed description of these methods:

Standard Configurations			
Config Index	**I/O or Memory**	**Address**	**Description**
0	Memory	0h-Fh, 400h-7FFh	Memory Mapped
1	I/O	XX0h-XXFh	I/O Mapped 16 Contiguous Registers
2	I/O	1F0h-1F7h, 3F6h-3F7h	Primary I/O Mapped
3	I/O	170h-177h, 376h-377h	Secondary I/O Mapped

I/O Primary and Secondary Address Configurations

Table: Primary and Secondary I/O Decoding

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note
0	1F(17)h	0	0	0	0	Even RD Data	Even WR Data	1, 2
0	1F(17)h	0	0	0	1	Error Register	Features	1, 2
0	1F(17)h	0	0	1	0	Sector Count	Sector Count	
0	1F(17)h	0	0	1	1	Sector No.	Sector No.	
0	1F(17)h	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)h	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)h	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)h	0	1	1	1	Status	Command	
0	3F(37)h	0	1	1	0	Alt Status	Device Control	
0	3F(37)h	0	1	1	1	Drive Address	Reserved	

Note: 1) Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers, which lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

2) A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the CompactFlash Storage Card, the registers are accessed in the block of I/O space decoded by the system as follows:

Table: Contiguous I/O Decoding

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card /Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

Memory Mapped Addressing

When the CompactFlash Storage Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as follows:

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1, 2
1	0	X	0	0	0	1	1	Error	Features	1, 2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card /Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

True IDE Mode Addressing

When the CompactFlash Storage Card is configured in the True IDE Mode, the I/O decoding is as follows:

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0	Note
1	0	0	0	0	1	PIO RD Data	PIO WR Data	8 or 16 bit[1]
1	1	X	X	X	0	DMA RD Data	DMA WR Data	16 bit
1	0	0	0	1	1	Error Register	Features	8 bit
1	0	0	1	0	1	Sector Count	Sector Count	8 bit
1	0	0	1	1	1	Sector No.	Sector No.	8 bit
1	0	1	0	0	1	Cylinder Low	Cylinder Low	8 bit
1	0	1	0	1	1	Cylinder High	Cylinder High	8 bit
1	0	1	1	0	1	Select Card/Head	Select Card/Head	8 bit
1	0	1	1	1	1	Status	Command	8 bit
0	1	1	1	0	1	Alt Status	Device Control	8 bit

CF-ATA Registers

The following section describes the hardware registers used by the host software to issue commands to the CompactFlash device. These registers are often collectively referred to as the "task file."

- **Data Register (Address - 1F0h[170h];Offset 0,8,9)**

The Data Register is a 16 bit register, and it is used to transfer data blocks between the CompactFlash Storage Card data buffer and the Host. This register overlaps the Error Register.

Data Register Memory and I/O Modes	-CE2	-CE1	A0	-REG	Offset	Data Bus
Word Data Register	0	0	X	- [1]	0,8,9	D15-D0
Even Data Register	1	0	0	- [1]	0,8	D7-D0
Odd Data Register	1	0	1	- [1]	9	D7-D0
Odd Data Register	0	1	X	- [1]	8,9	D15-D8
Error / Feature Register	1	0	1	- [1]	1, Dh	D7-D0
Error / Feature Register	0	1	X	- [1]	1	D15-D8
Error / Feature Register	0	0	X	- [1]	Dh	D15-D8
Data Register True IDE Mode	**-CS1**	**-CS0**	**A0**	**-DMACK**	**Offset**	**Data Bus**
PIO Word Data Register	1	0	0	1	0	D15-D0
DMA Word Data Register	1	1	X	0	X	D15-D0
PIO Byte Data Register (Selected Using Set Features Command)	1	0	0	1	0	D7-D0

Notes: 1) -REG signal is mode dependent. Signal shall be 0 for I/O mode and 1 for Memory Mode.

Error Register (Address - 1F1h[171h]; Offset 1, 0Dh Read Only)
This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register.

D7	D6	D5	D4	D3	D2	D1	D0
BBK/ICRC	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed in PC Card Modes on data bits D15-D8 during a read operation to offset 0 with -CE2 low and -CE1 high.

Bit 7 (BBK/ICRC): this bit is set when a Bad Block is detected. This bit is also set when an interface CRC error is detected in True IDE Ultra DMA modes of operation.
Bit 6 (UNC): this bit is set when an Uncorrectable Error is encountered.
Bit 5: this bit is 0.
Bit 4 (IDNF): the requested sector ID is in error or cannot be found.
Bit 3: this bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a CompactFlash Storage Card status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error.

- **Feature Register (Address - 1F1h[171h]; Offset 1, 0Dh Write Only)**
  This register provides information regarding features of the CompactFlash Storage Card that the host can utilize. This register is also accessed in PC Card modes on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high.

- **Sector Count Register (Address - 1F2h[172h]; Offset 2)**
  This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash Storage Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

- **Sector Number (LBA 7-0) Register (Address - 1F3h[173h]; Offset 3)**
  This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any CompactFlash Storage Card data access for the subsequent command.

- **6.1.5.5 Cylinder Low (LBA 15-8) Register (Address - 1F4h[174h]; Offset 4)**
  This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

- **Cylinder High (LBA 23-16) Register (Address - 1F5h[175h]; Offset 5)**
  This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

- **Drive/Head (LBA 27-24) Register (Address 1F6h[176h]; Offset 6)**
  The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing.

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7: this bit is specified as 1 for backward compatibility reasons. It is intended that this bit will become obsolete in a future revision of the specification. This bit is ignored by some controllers in some commands.

Bit 6: LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA7-LBA0: Sector Number Register D7-D0.
LBA15-LBA8: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.

Bit 5: this bit is specified as 1 for backward compatibility reasons. It is intended that this bit will become obsolete in a future revisions of the specification. This bit is ignored by some controllers in some commands.

Bit 4 (DRV): DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected. Setting this bit to 1 is obsolete in PCMCIA modes of operation. If the obsolete functionality is support by a CF Storage Card, the CompactFlash Storage Card is set to be Card 0 or 1 using the copy field (Drive #) of the PCMCIA Socket & Copy configuration register.

Bit 3 (HS3): when operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2): when operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1): when operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0): when operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

- **Status & Alternate Status Registers (Address 1F7h[177h]&3F6h[376h]; Offsets 7 & Eh)**

These registers return the CompactFlash Storage Card status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY): the busy bit is set when the CompactFlash Storage Card has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1. During the data transfer of DMA commands, the Card shall not assert DMARQ unless either the BUSY bit, the DRQ bit, or both are set to one.

Bit 6 (RDY): RDY indicates whether the device is capable of performing CompactFlash Storage Card operations. This bit is cleared at power up and remains cleared until the CompactFlash Storage Card is ready to accept a command.

Bit 5 (DWF): This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC): This bit is set when the CompactFlash Storage Card is ready.

Bit 3 (DRQ): The Data Request is set when the CompactFlash Storage Card requires that information be transferred either to or from the host through the Data register. During the data transfer of DMA commands, the Card shall not assert DMARQ unless either the BUSY bit, the DRQ bit, or both are set to one.

Bit 2 (CORR): This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX): This bit is always set to 0.

Bit 0 (ERR): This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is recommended that media access commands (such as Read Sectors and Write Sectors) that end with an error condition should have the address of the first sector in error in the command block registers.

- **Device Control Register (Address - 3F6h[376h]; Offset Eh)**

This register is used to control the CompactFlash Storage Card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X(0)	X(0)	X(0)	X(0)	X(0)	SW Rst	-IEn	0

Bit 7: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0.

Bit 6: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0.

Bit 5: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0.

Bit 4: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0.

Bit 3: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0.

Bit 2 (SW Rst): this bit is set to 1 in order to force the CompactFlash Storage Card to perform an AT Disk controller Soft Reset operation. This does not change the PCMCIA Card Configuration Registers as a hardware Reset does. The Card remains in Reset until this bit is reset to '0.'

Bit 1 (-IEn): the Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the CompactFlash Storage Card are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.

Bit 0: this bit is ignored by the CompactFlash Storage Card.

- **Card (Drive) Address Register (Address 3F7h[377h]; Offset Fh)**

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7.

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7: this bit is unknown.

Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the CompactFlash Storage Card. Following are some possible solutions to this problem for the PCMCIA implementation:

1) Locate the CompactFlash Storage Card at a non-conflicting address, i.e. Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses.

2) Do not install a Floppy and a CompactFlash Storage Card in the system at the same time.

3) Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7h/377h when a CompactFlash Storage Card is installed and conversely to tristate D6-D0 of I/O address 3F7h/377h when a floppy controller is installed.

4) Do not use the CompactFlash Storage Card's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0h-1F7h, 3F6h (or 170h-177h, 176h) to the CompactFlash Storage Card or b) if provided use an additional Primary / Secondary configuration in the CompactFlash Storage Card which does not respond to accesses to I/O locations 3F7h and 377h. With either of these implementations, the host software shall not attempt to use information in the Drive Address Register.

Bit 6 (-WTG): this bit is 0 when a write operation is in progress; otherwise, it is 1.

Bit 5 (-HS3): this bit is the negation of bit 3 in the Drive/Head register.

Bit 4 (-HS2): this bit is the negation of bit 2 in the Drive/Head register.

Bit 3 (-HS1): this bit is the negation of bit 1 in the Drive/Head register.

Bit 2 (-HS0): this bit is the negation of bit 0 in the Drive/Head register.

Bit 1 (-nDS1): this bit is 0 when drive 1 is active and selected.

Bit 0 (-nDS0): this bit is 0 when the drive 0 is active and selected.

CF-ATA Command Set

CF-ATA Command Set summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

	Command	Code	FR	SC	SN	CY	DH	LBA	Status	Note
1	Check Power Mode	E5 or 98h	–	–	–	–	Y	–	Support	
2	Execute Drive Diagnostic	90h	–	–	–	–	Y	–	Support	
3	Erase Sector	C0h	–	Y	Y	Y	Y	Y	Support	
4	Flush Cache	E7h	–	–	–	–	Y	–	NOT Support	#3
5	Format Track	50h	–	Y	–	Y	Y	Y	Support	
6	Identify Device	ECh	–	–	–	–	Y	–	Support	
7	Idle	E3h or 97h	–	Y	–	–	Y	–	Support	
8	Idle Immediate	E1h or 95h	–	–	–	–	Y	–	Support	
9	Initialize Drive Parameters	91h	–	Y	–	–	Y	–	Support	
10	Key Management Structure Read	B9 (Feature 0-127)	Y	Y	Y	Y	Y	–	NOT Support	#1
11	Key Management Read Keying Material	B9 (Feature 80)	Y	Y	Y	Y	Y	–	NOT Support	#1
12	Key Management Change Key Management Value	B9 (Feature 81)	Y	Y	Y	Y	Y	–	NOT Support	#1
13	NOP	00h	–	–	–	–	Y	–	NOT Support	
14	Read Buffer	E4h	–	–	–	–	Y	–	Support	
15	Read DMA	C8h	–	Y	Y	Y	Y	Y	Support	
16	Read Long Sector	22h or 23h	–		Y	Y	Y	Y	NOT Support	#3
17	Read Multiple	C4h	–	Y	Y	Y	Y	Y	Support	
18	Read Sector(s)	20h or 21h	–	Y	Y	Y	Y	Y	Support	
19	Read Verify Sector(s)	40h or 41h	–	Y	Y	Y	Y	Y	Support	
20	Recalibrate	1Xh	–	–	–	–	Y	–	Support	
21	Request Sense	03h	–	–	–	–	Y	–	Support	
22	Security Disable Password	F6h	–	–	–	–	Y	–	Support	#2
23	Security Erase Prepare	F3h	–	–	–	–	Y	–	Support	#2
24	Security Erase Unit	F4h	–	–	–	–	Y	–	Support	#2
25	Security Freeze Lock	F5h	–	–	–	–	Y	–	Support	#2
26	Security Set Password	F1h	–	–	–	–	Y	–	Support	#2
27	Security Unlock	F2h	–	–	–	–	Y	–	Support	#2
28	Seek	7Xh	–	–	Y	Y	Y	Y	Support	

29	Set Feature	EFh	Y	–	–	–	Y	–	Support	
30	Set Multiple Mode	C6h	–	Y	–	–	Y	–	Support	
31	Set Sleep Mode	E6h or 99h	–	–	–	–	Y	–	Support	
32	Standby	E2 or 96h	–	–	–	–	Y	–	Support	
33	Standby Immediate	E0 or 94h	–	–	–	–	Y	–	Support	
34	Translate Sector	87h	–	Y	Y	Y	Y	Y	Support	
35	Wear Level	F5h	–	–	–	–	Y	–	Support	
36	Write Buffer	E8h	–	–	–	–	Y	–	Support	
37	Write DMA	CAh	–	Y	Y	Y	Y	Y	Support	
38	Write Long Sector	32h or 33h	–	–	Y	Y	Y	Y	Not Support	#3
39	Write Multiple	C5h	–	Y	Y	Y	Y	Y	Support	
40	Write Multiple w/o Erase	CDh	–	Y	Y	Y	Y	Y	Support	
41	Write Sector(s)	30h or 31h	–	Y	Y	Y	Y	Y	Support	
42	Write Sector(s) w/o Erase	38h	–	Y	Y	Y	Y	Y	Support	
43	Write Verify	3Ch	–	Y	Y	Y	Y	Y	Support	

#1: This command is optional, depending on the key Management scheme in use.

#2: Use of this command is not recommended by CFA

#3: Use of this command is not recommended.

#4: When the controller gets this command, it will skip this command and return 0x50.

Definitions

FR = Features Register

SC =Sector Count register (00H to FFH, 00H means 256 sectors)

SN = Sector Number register

CY = Cylinder Low/High register

DH = Head No. (0 to 15) of Drive/Head register

LBA = Logic Block Address Mode Support

– = Not used for the command

Y = Used for the command

Check Power Mode - 98h or E5h

If the CompactFlash Storage Card is in, going to, or recovering from the sleep mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.

If the CompactFlash Storage Card is in Idle mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98h or E5h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Execute Drive Diagnostic - 90h

When the diagnostic command is issued in a PCMCIA configuration mode, this command runs only on the CompactFlash Storage Card that is addressed by the Drive/Head register. This is because PCMCIA card interface does not allows for direct inter-drive communication (such as the ATA PDIAG and DASP signals). When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Diagnostic Codes are returned in the Error Register at the end of the command.

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

Erase Sector(s) - C0h

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Flush Cache – E7h

This command causes the card to complete writing data from its cache. The card returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the Compact Flash Storage Card does not support the Flush Cache command, the Compact Flash Storage Card shall return command aborted.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E7h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Format Track - 50h

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the CompactFlash Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash Storage Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Count (LBA mode only)							
Feature (1)	X							

■ Identify Device – Ech

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify Device command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table as below. All reserved bits or words are zero. Hosts should not depend on Obsolete words in Identify Device containing 0. Table 47 specifies each field in the data returned by the Identify Device Command. In Table as below, X indicates a numeric nibble value specific to the card and aaaa indicates an ASCII string specific to the particular drive.

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration - signature for the CompactFlash 0 lash Storage Card
	0XXX	2	General configuration – Bit Significant with ATA-4 definitions.
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0000h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	XXXXh	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0000h	2	Obsolete
21	0000h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	XXXXh	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	XX00h	2	Capabilities
50	0000h	2	Reserved

Word Address	Default Value	Total Bytes	Data Field Type Information
51	0X00h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	000Xh	2	Field Validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	01XXh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0X0Xh	2	Multiword DMA transfer. In PC Card modes this value shall be 0h
64	00XXh	2	Advanced PIO modes supported
65	XXXXh	2	Minimum Multiword DMA transfer cycle time per word. In PC Card modes this value shall be 0h
66	XXXXh	2	Recommended Multiword DMA transfer cycle time. In PC Card modes this value shall be 0h
67	XXXXh	2	Minimum PIO transfer cycle time without flow control
68	XXXXh	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80-81	0000h	4	Reserved – CF cards do not return an ATA version
82-84	XXXXh	6	Features/command sets supported
85-87	XXXXh	6	Features/command sets enabled
88	XXXXh	2	Ultra DMA Mode Supported and Selected
89	XXXXh	2	Time required for Security erase unit completion
90	XXXXh	2	Time required for Enhanced security erase unit completion
91	XXXXh	2	Current Advanced power management value
92-127	0000h	72	Reserved
128	XXXXh	2	Security status
129-159	0000h	64	Vendor unique bytes
160	XXXXh	2	Power requirement description
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported
163	XXXXh	2	CF Advanced True IDE Timing Mode Capability and Setting
164	XXXXh	2	CF Advanced PC Card I/O and Memory Timing Mode Capability
165-167	0000h	6	Reserved for assignment by the CFA
168-255	0000h	158	Reserved

- **Word 0: General Configuration**

  This field indicates the general characteristics of the device. When Word 0 of the Identify drive information is 848Ah then the device is a CompactFlash Storage Card and complies with the CFA specification and CFA command set. It is recommended that PCMCIA modes of operation report only the 848Ah value as they are always intended as removable devices.

  Bits 15-0: CF Standard Configuration Value
  Word 0 is 848Ah. This is the recommended value of Word 0.

  Some operating systems require Bit 6 of Word 0 to be set to 1 (Non-removable device) to use the card as the root storage device. The Card must be the root storage device when a host completely replaces conventional disk storage with a CompactFlash Card in True IDE mode. To support this requirement and provide capability for any future removable media Cards, alternatehandling of Word 0 is permitted.

  Bits 15-0: CF Preferred Alternate Configuration Values
  044Ah: This is the alternate value of Word 0 turns on ATA device and turns off Removable Media and Removable Device while preserving all Retired bits in the word.
  0040h: This is the alternate value of Word 0 turns on ATA device and turns off Removable Media and Removable Device while zeroing all Retired bits in the word

  Bit 15-12: Configuration Flag
  If bits 15:12 are set to 8h then Word 0 shall be 848Ah.
  If bits 15:12 are set to 0h then Bits 11:0 are set using the definitions below and the Card is required to support for the CFA command set and report that in bit 2 of Word 83.
  Bit 15:12 values other than 8h and 0h are prohibited.

  Bits 11-8: Retired
  These bits have retired ATA bit definitions. It is recommended that the value of these bits be either the preferred value of 0h or the value of 4h that preserves the corresponding bits from the 848Ah CF signature value.

  Bit 7: Removable Media Device
  If Bit 7 is set to 1, the Card contains media that can be removed during Card operation.
  If Bit 7 is set to 0, the Card contains nonremovable media.

  Bit 6: Not Removable Controller and/or Device
  Alert! This bit will be considered for obsolescence in a future revision of this standard.
  If Bit 6 is set to 1, the Card is intended to be nonremovable during operation.
  If Bit 6 is set to 0, the Card is intended to be removable during operation.

  Bits 5-0: Retired/Reserved
  Alert! Bit 2 will be considered for definition in a future revision of this standard and shall be 0 at this time.
  Bits 5-1 have retired ATA bit definitions.
  Bit 2 shall be 0.
  Bit 0 is Reserved and shall be 0.
  It is recommended that the value of bits 5-0 be either the preferred value of 00h or the value of 0Ah that preserves the corresponding bits from the 848Ah CF signature value.

- **Word 1: Default Number of Cylinders**

  This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

- **Word 3: Default Number of Heads**

  This field contains the number of translated heads in the default translation mode.

- **Word 6: Default Number of Sectors per Track**

  This field contains the number of sectors per track in the default translation mode.

- **Words 7-8: Number of Sectors per Card**
  This field contains the number of sectors per CompactFlash Storage Card. This double word value is also the first invalid address in LBA translation mode.
- **Words 10-19: Serial Number**
  This field contains the serial number for this CompactFlash Storage Card and is right justified and padded with spaces (20h).
- **Word 22: ECC Count**
  This field defines the number of ECC bytes used on each sector in the Read and Write Long commands. This value shall be set to 0004h.
- **Words 23-26: Firmware Revision**
  This field contains the revision of the firmware for this product.
- **Words 27-46: Model Number**
  This field contains the model number for this product and is left justified and padded with spaces (20h).
- **Word 47: Read/Write Multiple Sector Count**
  Bits 15-8 shall be the recommended value of 80h or the permitted value of 00h. Bits 7-0 of this word define the maximum number of sectors per block that the CompactFlash Storage Card supports for Read/Write Multiple commands.
- **Word 49: Capabilities**
  Bit 13: Standby Timer
  If bit 13 is set to 1 then the Standby timer is supported as defined by the IDLE command
  If bit 13 is set to 0 then the Standby timer operation is defined by the vendor.
  Bit 11: IORDY Supported
  If bit 11 is set to 1 then this CompactFlash Storage Card supports IORDY operation.
  If bit 11 is set to 0 then this CompactFlash Storage Card may support IORDY operation.
  Bit 10: IORDY may be disabled
  Bit 10 shall be set to 0, indicating that IORDY may not be disabled.
  Bit 9: LBA supported
  Bit 9 shall be set to 1, indicating that this CompactFlash Storage Card supports LBA mode addressing. CF devices shall support LBA addressing.
  Bit 8: DMA Supported If bit 8 is set to 1 then Read DMA and Write DMA commands are supported. Bit 8 shall be set to 0. Read/Write DMA commands are not currently permitted on CF cards.
- **PIO Data Transfer Cycle Timing Mode**
  The PIO transfer timing for each CompactFlash Storage Card falls into modes that have unique parametric timing specifications. The value returned in Bits 15-8 shall be 00h for mode 0, 01h for mode 1, or 02h for mode 2. Values 03h through FFh are reserved.
- **Translation Parameters Valid**
  Bit 0 shall be set to 1 indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. If bit 1 of word 53 is set to 1, the values in words 64 through 70 are valid. If this bit is cleared to 0, the values reported in words 64-70 are not valid. Any CompactFlash Storage Card that supports PIO mode 3 or above shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70.
- **Current Number of Cylinders, Heads, Sectors/Track**
  These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.
- **Current Capacity**
  This field contains the product of the current cylinders times heads times sectors.

- **Multiple Sector Setting**
  Bits 15-9 are reserved and shall be set to 0.
  Bit 8 shall be set to 1 indicating that the Multiple Sector Setting is valid.
  Bits 7-0 are the current setting for the number of sectors that shall be transferred per interrupt on Read/Write Multiple commands.

- **Total Sectors Addressable in LBA Mode**
  This field contains the total number of user addressable sectors for the CompactFlash Storage Card in LBA mode only.

- **Multiword DMA transfer**
  Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the CompactFlash Storage Card to indicate the multiword DMA mode which is currently selected. Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected.
  Selection of Multiword DMA modes 3 and above are specific to CompactFlash are reported in word 163, Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.
  Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the CompactFlash Storage Card to indicate the Multiword DMA modes it is capable of supporting.
  Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA modes 2, 1 and 0. Support for Multiword DMA modes 3 and above are specific to CompactFlash are reported in word 163, Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

- **Word 64: Advanced PIO transfer modes supported**
  Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the CompactFlash Storage Card to indicate the advanced PIO modes it is capable of supporting.
  Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the CompactFlash Storage Card supports PIO mode 3. Bit 1, if set to one, indicates that the CompactFlash StorageCard supports PIO mode 4.
  Support for PIO modes 5 and above are specific to CompactFlash are reported in word 163.

- **Word 65: Minimum Multiword DMA transfer cycle time**
  Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the CompactFlash Storage Card guarantees data integrity during the transfer.
  If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all CompactFlash Storage Cards supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field.

- **Recommended Multiword DMA transfer cycle time**
  Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the CompactFlash Storage Card

will need to negate the DMARQ signal during the transfer of a sector.
If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all CompactFlash Storage Cards supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field.

- **Word 67: Minimum PIO transfer cycle time without flow control**
  Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the CompactFlash Storage Card guarantees data integrity during the transfer without utilization of flow control. If this field is supported, Bit 1 of word 53 shall be set to one. Any CompactFlash Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68. If bit 1 of word 53 is set to one because a CompactFlash Storage Card supports a field in words 64-70 other than this field and the CompactFlash Storage Card does not support this field, the CompactFlash Storage Card shall return a value of zero in this field.

- **Word 68: Minimum PIO transfer cycle time with IORDY**
  Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the CompactFlash Storage Card supports while performing data transfers while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. Any CompactFlash Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the CompactFlash Storage Card. If bit 1 of word 53 is set to one because a CompactFlash Storage Card supports a field in words 64-70 other than this field and the CompactFlash Storage Card does not support this field, the CompactFlash Storage Card shall return a value of zero in this field.

- **Words 82-84: Features/command sets supported**
  Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by CompactFlash Storage Cards prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers.

  Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported.
  If bit 1 of word 82 is set to one, the Security Mode feature set is supported.
  Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.
  Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.
  Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.
  If bit 5 of word 82 is set to one, write cache is supported.
  If bit 6 of word 82 is set to one, look-ahead is supported.
  Bit 7 of word 82 shall be set to zero; release interrupt is not supported.
  Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.
  Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.
  Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported.
  Bit 11 of word 82 is obsolete.
  Bit 12 of word 82 shall be set to one; the CompactFlash Storage Card supports the Write Buffer command.
  Bit 13 of word 82 shall be set to one; the CompactFlash Storage Card supports the Read Buffer command.
  Bit 14 of word 82 shall be set to one; the CompactFlash Storage Card supports the NOP command.
  Bit 15 of word 82 is obsolete.

  Bit 0 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Download

Microcode command.
Bit 1 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Read DMA Queued and Write DMA Queued commands.
Bit 2 of word 83 shall be set to one; the CompactFlash Storage Card supports the CFA feature set.
If bit 3 of word 83 is set to one, the CompactFlash Storage Card supports the Advanced Power Management feature set.
Bit 4 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Removable Media Status feature set.

- **Words 85-87: Features/command sets enabled**

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by CompactFlash Storage Cards prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.

Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled.
If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security Set Password command.
Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.
Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.
Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.
If bit 5 of word 85 is set to one, write cache is enabled.
If bit 6 of word 85 is set to one, look-ahead is enabled.
Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.
Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.
Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.
Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.
Bit 11 of word 85 is obsolete.
Bit 12 of word 85 shall be set to one; the CompactFlash Storage Card supports the Write Buffer command.
Bit 13 of word 85 shall be set to one; the CompactFlash Storage Card supports the Read Buffer command.
Bit 14 of word 85 shall be set to one; the CompactFlash Storage Card supports the NOP command.
Bit 15 of word 85 is obsolete.

Bit 0 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Download Microcode command.
Bit 1 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Read DMA Queued and Write DMA Queued commands.
If bit 2 of word 86 shall be set to one, the CompactFlash Storage Card supports the CFA feature set.
If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.
Bit 4 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Removable Media Status feature set.

- **Word 88: Ultra DMA Modes Supported and Selected**

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported.

Bits 15-14: Reserved

Bit 13: 1 = Ultra DMA mode 5 is selected, 0 = Ultra DMA mode 5 is not selected

Bit 12: 1 = Ultra DMA mode 4 is selected, 0 = Ultra DMA mode 4 is not selected
Bit 11: 1 = Ultra DMA mode 3 is selected, 0 = Ultra DMA mode 3 is not selected
Bit 10: 1 = Ultra DMA mode 2 is selected, 0 = Ultra DMA mode 2 is not selected
Bit 9: 1 = Ultra DMA mode 1 is selected, 0 = Ultra DMA mode 1 is not selected
Bit 8: 1 = Ultra DMA mode 0 is selected, 0 = Ultra DMA mode 0 is not selected
Bits 7-6: Reserved
Bit 5: 1 = Ultra DMA mode 5 and below are supported. Bits 0-4 Shall be set to 1.
Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 Shall be set to 1.
Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 Shall be set to 1.
Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 Shall be set to 1.
Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 Shall be set to 1.
Bit 0: 1 = Ultra DMA mode 0 is supported

- **Word 89: Time required for Security erase unit completion**

  Word 89 specifies the time required for the Security Erase Unit command to complete. This command shall be supported on CompactFlash Storage Cards that support security.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

- **Word 90: Time required for Enhanced security erase unit completion**

  Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete. This command shall be supported on CompactFlash Storage Cards that support security.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

- **Word 91: Advanced power management level value**

  Bits 7-0 of word 91 contain the current Advanced Power Management level setting.

- **Word 128: Security Status**

  Bit 8: Security Level
  If set to 1, indicates that security mode is enabled and the security level is maximum.
  If set to 0 and security mode is enabled, indicates that the security level is high.
  Bit 5: Enhanced security erase unit feature supported
  If set to 1, indicates that the Enhanced security erase unit feature set is supported.
  Bit 4: Expire
  If set to 1, indicates that the security count has expired and Security Unlock and Security Erase Unit are command aborted until a power-on reset or hard reset.
  Bit 3: Freeze
  If set to 1, indicates that the security is Frozen.
  Bit 2: Lock
  If set to 1, indicates that the security is locked.
  Bit 1: Enable/Disable
  If set to 1, indicates that the security is enabled.
  If set to 0, indicates that the security is disabled.
  Bit 0: Capability
  If set to 1, indicates that CompactFlash Storage Card supports security mode feature set.
  If set to 0, indicates that CompactFlash Storage Card does not support security mode feature set.

- **Word 160: Power Requirement Description**

  This word is required for CompactFlash Storage Cards that support power mode 1.

  Bit 15: VLD
  If set to 1, indicates that this word contains a valid power requirement description.
  If set to 0, indicates that this word does not contain a power requirement description.
  Bit 14: RSV
  This bit is reserved and shall be 0.
  Bit 13: -XP
  If set to 1, indicates that the CompactFlash Storage Card does not have Power Level 1 commands.
  If set to 0, indicates that the CompactFlash Storage Card has Power Level 1 commands
  Bit 12: -XE
  If set to 1, indicates that Power Level 1 commands are disabled.
  If set to 0, indicates that Power Level 1 commands are enabled.
  Bit 0-11: Maximum current
  This field contains the CompactFlash Storage Card's maximum current in mA.

- **Word 162: Key Management Schemes Supported**

  Bit 0: CPRM support
  If set to 1, the device supports CPRM Scheme (Content Protection for Recordable Media)
  If set to 0, the device does not support CPRM.
  Bits 1-15 are reserved for future additional Key Management schemes.

- **Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings**

  This word describes the capabilities and current settings for CFA defined advanced timing modes using the True IDE interface.
  Notice! The use of True IDE PIO Modes 5 and above or of Multiword DMA Modes 3 and above impose significant restrictions on the implementation of the host:
  Additional Requirements for CF Advanced Timing Modes.
  There are four separate fields defined that describe support and selection of Advanced PIO timing modes and Advanced Multiword DMA timing modes. The older modes are reported in words 63 and 64.
  Word 63: Multiword DMA transfer and 6.2.1.6.19: Word 64: Advanced PIO transfer modes supported.

  Bits 2-0: Advanced True IDE PIO Mode Support Indicates the maximum True IDE PIO mode supported by the card.

Value	Maximum PIO mode timing selected
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

  Bits 5-3: Advanced True IDE Multiword DMA Mode Support Indicates the maximum True IDE Multiword DMA mode supported by the card.

Value	Maximum Multiword DMA timing mode supported
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

Bits 8-6: Advanced True IDE PIO Mode Selected Indicates the current True IDE PIO mode selected on the card.

Value	Current PIO timing mode selected
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

Bits 11-9: Advanced True IDE Multiword DMA Mode Selected Indicates the current True IDE Multiword DMA Mode Selected on the card.

Value	Current Multiword DMA timing mode selected
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

Bits 15-12 are reserved.

- **Word 164: CF Advanced PCMCIA I/O and Memory Timing Modes Capabilities and Settings**

This word describes the capabilities and current settings for CFA defined advanced timing modes using the Memory and PCMCIA I/O interface.

Notice! The use of PCMCIA I/O or Memory modes that are 100ns or faster impose significant restrictions on the implementation of the host:
Additional Requirements for CF Advanced Timing Modes.

Bits 2-0: Maximum Advanced PCMCIA I/O Mode Support Indicates the maximum I/O timing mode supported by the card.

Value	Maximum PCMCIA IO timing mode Supported
0	255ns Cycle PCMCIA I/O Mode
1	120ns Cycle PCMCIA I/O Mode
2	100ns Cycle PCMCIA I/O Mode
3	80ns Cycle PCMCIA I/O Mode
4-7	Reserved

Bits 5-3: Maximum Memory timing mode supported
Indicates the Maximum Memory timing mode supported by the card.

Value	Maximum Memory timing mode Supported
0	250ns Cycle Memory Mode
1	120ns Cycle Memory Mode
2	100ns Cycle Memory Mode
3	80ns Cycle Memory Mode
4-7	Reserved

Bits 8-6: Maximum PC Card I/O UDMA timing mode supported Indicates the Maximum PC Card I/O UDMA timing mode supported by the card when bit 15 is set.

Value	Maximum PC Card I/O UDMA timing mode Supported
0	PC Card I/O UDMA mode 0 supported
1	PC Card I/O UDMA mode 1 supported
2	PC Card I/O UDMA mode 2 supported
3	PC Card I/O UDMA mode 3 supported
4	PC Card I/O UDMA mode 4 supported
5	PC Card I/O UDMA mode 5 supported
6	Reserved
7	Reserved

Bits 11-9: Maximum PC Card Memory UDMA timing mode supported Indicates the Maximum PC Card Memory UDMA timing mode supported by the card when bit 15 is set.

Value	Maximum PC Card Memory UDMA timing mode Supported
0	PC Card Memory UDMA mode 0 supported
1	PC Card Memory UDMA mode 1 supported
2	PC Card Memory UDMA mode 2 supported
3	PC Card Memory UDMA mode 3 supported
4	PC Card Memory UDMA mode 4 supported
5	PC Card Memory UDMA mode 5 supported
6	Reserved
7	Reserved

Bits 14-12: PC Card Memory or I/O UDMA timing mode selectedIndicates the PC Card Memory or I/O UDMA timing mode selected by the card.

Value	PC Card Memory or I/O UDMA timing mode Selected
0	PC Card I/O UDMA mode 0 selected
1	PC Card I/O UDMA mode 1 selected
2	PC Card I/O UDMA mode 2 selected
3	PC Card I/O UDMA mode 3 selected
4	PC Card I/O UDMA mode 4 selected
5	PC Card I/O UDMA mode 5 selected
6	Reserved
7	Reserved

Bit 15: PC Card Memory and IO Modes Supported

This bit, when set, indicates that the PC Card UDMA support values in bits 11-6 are valid. When this bit is cleared, PC Card Memory and IO Modes are not supported by the device.

Idle - 97h or E3h

This command causes the CompactFlash Storage Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97h or E3h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

Idle Immediate - 95h or E1h

This command causes the CompactFlash Storage Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95h or E1h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Initialize Drive Parameters - 91h

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91h							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

NOP - 00h

This command always fails with the CompactFlash Storage Card returning command aborted.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	00h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Read Buffer - E4h

The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Read DMA – C8h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C8h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Read Long Sector - 22h or 23h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22h or 23h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

- **Read Multiple - C4h**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

- **Read Sector(s) - 20h or 21h**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20h or 21h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

- **Read Verify Sector(s) - 40h or 41h**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40h or 41h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

- **Recalibrate - 1Xh**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1Xh							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Request Sense - 03h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03h							
C/D/H (6)	1	X	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The extended error code is returned to the host in the Error Register.

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed
22h	Power Level 1 Disabled

Seek - 7Xh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7Xh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Set Features – EFh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

Feature Supported

Feature	Operation
01h	Enable 8 bit data transfers.
02h	Enable Write Cache.
03h	Set transfer mode based on value in Sector Count register.
05h	Enable Advanced Power Management.
09h	Enable Extended Power operations. ***(Alert: It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.)***
0Ah	Enable Power Level 1 commands.
44h	Product specific ECC bytes apply on Read/Write Long commands.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69h	NOP - Accepted for backward compatibility.
81h	Disable 8 bit data transfer.
82h	Disable Write Cache.
85h	Disable Advanced Power Management.
89h	Disable Extended Power operations. ***(Alert: It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.)***
8Ah	Disable Power Level 1 commands.
96h	NOP - Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
AAh	Enable Read Look Ahead.
BBh	4 bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers shall occur on the low order D[7:0] data bus and the -IOIS16 signal shall not be asserted for data register accesses. The host shall not enable this feature for DMA transfers.

Features 02h and 82h allow the host to enable or disable write cache in CompactFlash Storage Cards that

implement write cache. When the subcommand disable write cache is issued, the CompactFlash Storage Card shall initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03h allows the host to select the PIO or Multiword DMA transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode shall be selected at all times. For Cards which support DMA, one Multiword DMA mode shall be selected at all times. The host may change the selected modes by the Set Features command.

■ Set Multiple Mode - C6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

■ Set Sleep Mode- 99h or E6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99h or E6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

■ Standby - 96h or E2h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	96h or E2h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Standby Immediate - 94h or E0h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94h or E0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Translate Sector - 87h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Translate Sector Information

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MSB (04) - LSB (06)
07h-12h	Reserved
13h	Erased Flag (FFh) = Erased; 00h = Not Erased
14h – 17h	Reserved
18h-1Ah	Hot Count MSB (18) - LSB (1A) [1]
1Bh-1FFh	Reserved

Wear Level - F5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5h							
C/D/H (6)	X	X	X	Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Completion Status							
Feature (1)	X							

Write Buffer - E8h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Write DMA – CAh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CAh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Long Sector - 32h or 33h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32h or 33h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Write Multiple Command - C5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5h							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Multiple without Erase – CDh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDh							
C/D/H (6)	X1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Sector(s) - 30h or 31h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30h or 31h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Sector(s) without Erase - 38h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Write Verify - 3Ch

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3Ch							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

■ Error Posting

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Check Power Mode				V		V	V	V		V
Execute Drive Diagnostic[1]						V		V		V
Erase Sector(s)	V		V	V	V	V	V	V		V
Flush Cache				V		V	V	V		V
Format Track			V	V	V	V	V	V		V
Identify Device				V		V	V	V		V
Idle				V		V	V	V		V
Idle Immediate				V		V	V	V		V
Initialize Drive Parameters						V		V		V
Key Management Structure Read		V	V	V		V		V		V
Key Management Read Keying Material		V	V	V		V		V		V
Key Management Change Key Management Value		V		V		V	V	V		V
NOP				V		V	V			V
Read Buffer				V		V	V	V		V
Read DMA	V	V	V	V	V	V	V	V	V	V
Read Multiple	V	V	V	V	V	V	V	V	V	V
Read Long Sector	V		V	V	V	V	V	V		V
Read Sector(s)	V	V	V	V	V	V	V	V	V	V
Read Verify Sectors	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request Sense				V		V		V		V
Security Disable Password				V		V	V	V		V
Security Erase Prepare				V		V	V	V		V
Security Erase Unit				V		V	V	V		V
Security Freeze Lock				V		V	V	V		V
Security Set Password				V		V	V	V		V
Security Unlock				V		V	V	V		V
Seek			V	V		V	V	V		V
Set Features				V		V	V	V		V

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Set Multiple Mode				V		V	V	V		V
Set Sleep Mode				V		V	V	V		V
Stand By				V		V	V	V		V
Stand By Immediate				V		V	V	V		V
Translate Sector	V		V	V	V	V	V	V		V
Wear Level	V	V	V	V	V	V	V	V		V
Write Buffer				V		V	V	V		V
Write DMA	V		V	V	V	V	V	V		V
Write Long Sector	V		V	V	V	V	V	V		V
Write Multiple	V		V	V	V	V	V	V		V
Write Multiple w/o Erase	V		V	V	V	V	V	V		V
Write Sector(s)	V		V	V	V	V	V	V		V
Write Sector(s) w/o Erase	V		V	V	V	V	V	V		V
Write Verify	V		V	V	V	V	V	V		V
Invalid Command Code				V		V	V	V		V

Error and Status Register summarizes the valid status and error value for all the CF-ATA Command set.

C.H.S. Table

Capacity	C	H	S
4GB	7899	16	63
8GB	15798	16	63
16GB	33149	15	63

SMART Command Set

- **SMART Command Set**

SMART Feature Register Values			
D0h	Read Data	D4h	Execute OFF-LINE Immediate
D1h	Read Attribute Threshold	D8h	Enable SMART Operations
D2h	Enable/Disable Autosave	D9h	Disable SMART Operations
D3h	Save Attribute Values	DAh	Return Status

1. If reserved size is below the Threshold, the status can be read from Cylinder register by Return Status command (DAh).

- **SMART Data Structure**

BYTE	F / V	Decription
0-1	X	Revision code
2-361	X	Vendor specific
362	V	Off line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	**F**	**Date Code**
396	**V**	**Number of MU in device (0~n)**
397+(n*6)	**V**	**MU number**
398+(n*6)	**V**	**MU data block**
400+(n*6)	**V**	**MU spare block**
401+(n*6)	**V**	**Init. Bad block**
402+(n*6)	**V**	**Last Defect Bad block (Newest state)**
511	V	Data structure checksum

F=the content of the byte is fixed and does not change.

V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.

X=the content of the byte is vendor specific and may be fixed or variable.

R=the content of the byte is reserved and shall be zero.

* 4 Byte value : [MSB] [2] [1] [LSB]

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