

# 74HC73

Dual JK flip-flop with reset; negative-edge trigger

Rev. 03 — 12 November 2004

Product data sheet

## 1. General description

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The 74HC73 is a high-speed Si-gate CMOS device and is pin compatible with low-power Schottky TTL (LSTTL). The 74HC73 is specified in compliance with JEDEC standard no. 7A.

The 74HC is a dual negative-edge triggered JK flip-flop featuring individual J, K, clock ( $\overline{nCP}$ ) and reset ( $\overline{nR}$ ) inputs; also complementary  $nQ$  and  $n\overline{Q}$  outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ( $\overline{nR}$ ) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the  $nQ$  output LOW and the  $n\overline{Q}$  output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## 2. Features

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- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+80\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

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### 3. Quick reference data

**Table 1: Quick reference data**

$GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f = 6\text{ ns}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHL}$ , $t_{PLH}$	propagation delay	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-		-	
	$n\overline{CP}$ to $nQ$		-	16	-	ns
	$n\overline{CP}$ to $n\overline{Q}$		-	16	-	ns
	$n\overline{R}$ to $nQ$ , $n\overline{Q}$		-	15	-	ns
$f_{max}$	maximum clock frequency	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	77	-	MHz
$C_I$	input capacitance		-	3.5	-	pF
$C_{PD}$	power dissipation capacitance per flip-flop	$V_I = GND$ to $V_{CC}$	[1]	30	-	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 4. Ordering information

**Table 2: Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74HC73N	-40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HC73D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC73DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HC73PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

5. Functional diagram

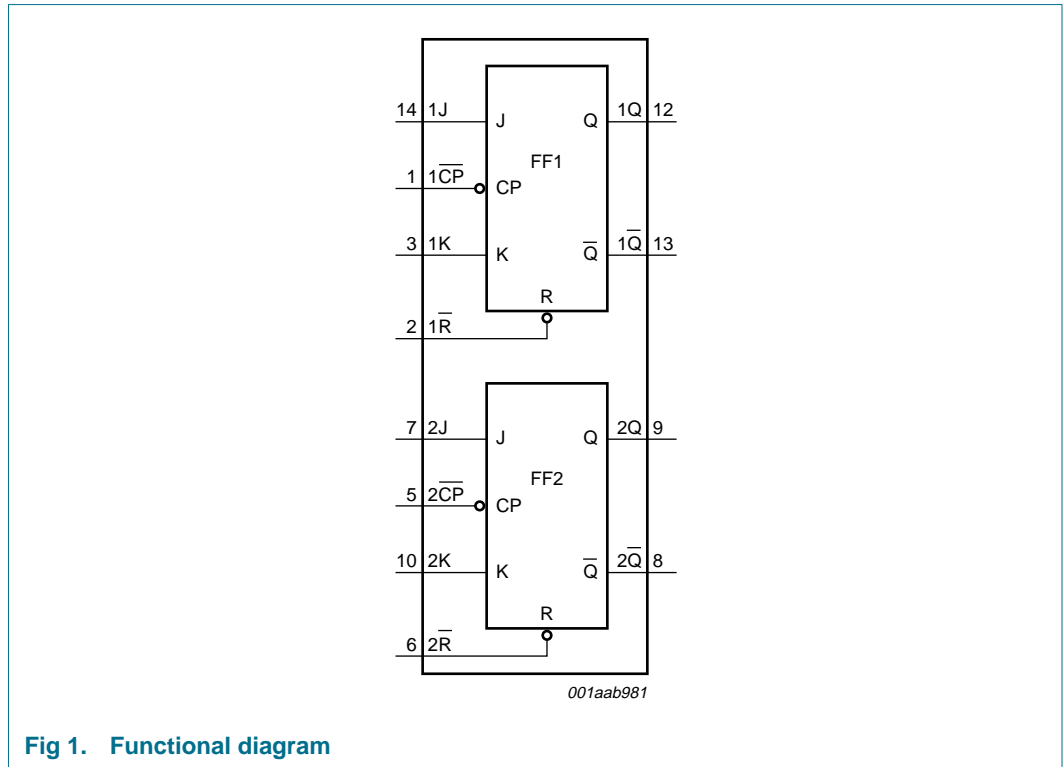


Fig 1. Functional diagram

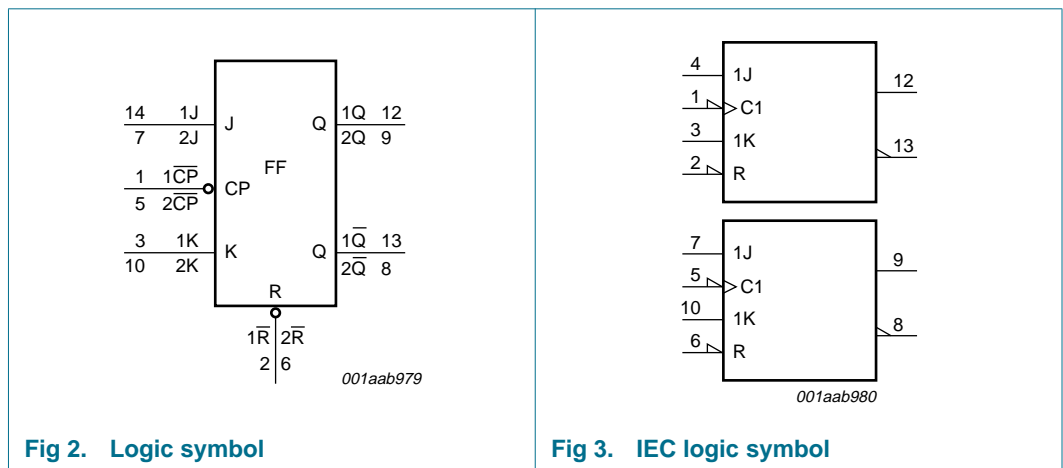
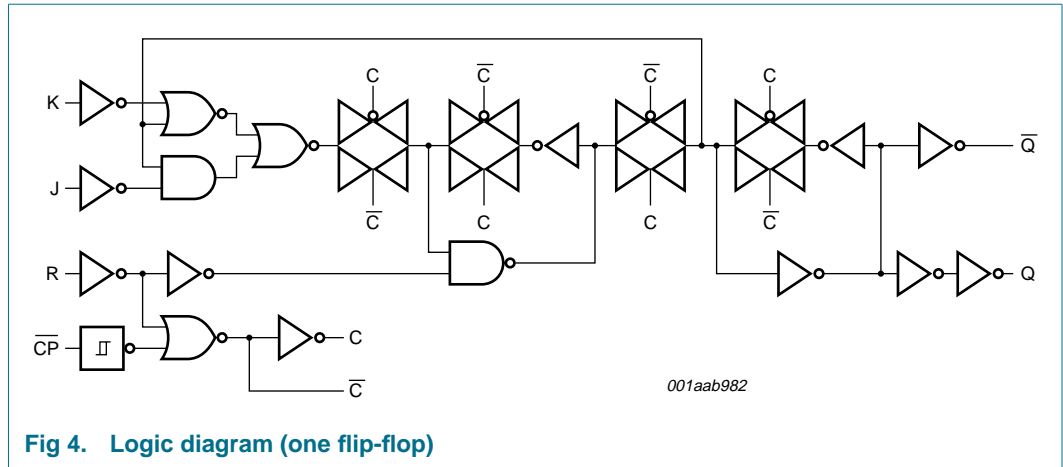


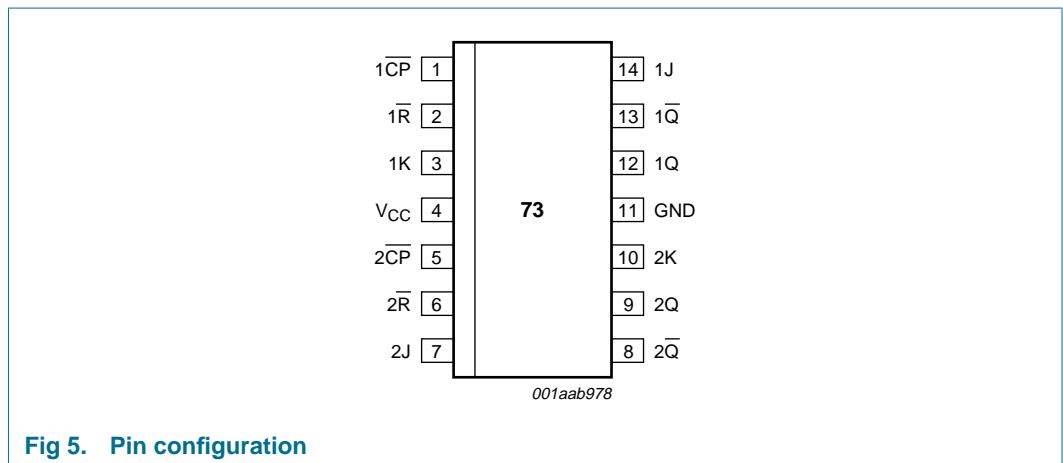
Fig 2. Logic symbol

Fig 3. IEC logic symbol



## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1CP	1	clock input for flip-flop 1 (HIGH-to-LOW, edge-triggered)
1R	2	asynchronous reset input for flip-flop 1 (active LOW)
1K	3	synchronous K input for flip-flop 1
V <sub>CC</sub>	4	positive supply voltage
2CP	5	clock input for flip-flop 2 (HIGH-to-LOW, edge-triggered)
2R	6	asynchronous reset input for flip-flop 2 (active LOW)
2J	7	synchronous J input for flip-flop 2
2Q	8	complement flip-flop 2 output
2Q	9	true flip-flop 2 output
2K	10	synchronous K input for flip-flop 2

Table 3: Pin description ...continued

Symbol	Pin	Description
GND	11	ground (0 V)
1Q	12	true flip-flop 1 output
1 $\bar{Q}$	13	complement flip-flop 1 output
1J	14	synchronous J input for flip-flop 1

## 7. Functional description

### 7.1 Function table

Table 4: Function table [1]

Input				Output		Operating mode
n $\bar{R}$	n $\bar{CP}$	nJ	nK	nQ	n $\bar{Q}$	
L	X	X	X	L	H	asynchronous reset
H	↓	h	h	$\bar{q}$	q	toggle
		l	h	L	H	load 0 (reset)
		h	l	H	L	load 1 (set)
		l	l	q	$\bar{q}$	hold (no change)

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition;  
 q = state of referenced output one set-up time prior to the HIGH-to-LOW CP transition;  
 X = don't care;  
 ↓ = HIGH-to-LOW CP transition.

## 8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
$I_{OK}$	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
$I_O$	output source or sink current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	±50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation				
	DIP14 package		[1]	-	750 mW
	SO14, SSOP14 and TSSOP14 packages		[2]	-	500 mW

[1] Above 70 °C:  $P_{tot}$  derates linearly with 12 mW/K.

[2] Above 70 °C:  $P_{tot}$  derates linearly with 8 mW/K.

## 9. Recommended operating conditions

**Table 6: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$t_r, t_f$	input rise and fall times except for nCP	$V_{CC} = 2.0\text{ V}$	-	-	1000	ns
		$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	-	-	400	ns
$T_{amb}$	ambient temperature		-40	-	+125	°C

## 10. Static characteristics

**Table 7: Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25\text{ °C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	6.0	-	V
		$I_O = -4\text{ mA}; V_{CC} = 4.5\text{ V}$	3.98	4.32	-	V
	$I_O = -5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	5.48	5.81	-	V	
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	-	0	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.15	0.26	V
	$I_O = 5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	-	0.16	0.26	V	
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	$\pm 0.1$	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}; V_{CC} = 6.0\text{ V}$	-	-	4.0	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	pF

**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 4.5 V	3.84	-	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.34	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 4.5 V	-	-	0.33	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	-	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	40.0	μA

**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40\text{ °C to }+125\text{ °C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	-	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	-	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	-	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	-	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 4.5\text{ V}$	3.7	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	-	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.4	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$
		$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}; V_{CC} = 6.0\text{ V}$	-	-	80.0	$\mu\text{A}$



## 11. Dynamic characteristics

**Table 8: Dynamic characteristics**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$ ; see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b><math>T_{\text{amb}} = 25\text{ °C}</math></b>							
$t_{\text{PHL}}, t_{\text{PLH}}$	propagation delay $\overline{nCP}$ to $nQ$	see <a href="#">Figure 6</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	-	52	160	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	-	19	32	ns	
		$V_{\text{CC}} = 6.0\text{ V}$	-	15	27	ns	
	propagation delay $\overline{nCP}$ to $n\overline{Q}$	see <a href="#">Figure 6</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	-	52	160	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	-	19	32	ns	
		$V_{\text{CC}} = 6.0\text{ V}$	-	15	27	ns	
	propagation delay $n\overline{R}$ to $nQ, n\overline{Q}$	see <a href="#">Figure 7</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	-	50	145	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	-	18	29	ns	
		$V_{\text{CC}} = 6.0\text{ V}$	-	14	25	ns	
$t_{\text{THL}}, t_{\text{TLH}}$	output transition time	see <a href="#">Figure 6</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	-	19	75	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	-	7	15	ns	
		$V_{\text{CC}} = 6.0\text{ V}$	-	6	13	ns	
$t_{\text{W}}$	$n\overline{CP}$ clock pulse width HIGH or LOW	see <a href="#">Figure 6</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	80	22	-	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	16	8	-	ns	
	$n\overline{R}$ reset pulse width HIGH or LOW	see <a href="#">Figure 7</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	80	22	-	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	16	8	-	ns	
	$t_{\text{rem}}$	removal time $n\overline{R}$ to $n\overline{CP}$	see <a href="#">Figure 7</a>				
			$V_{\text{CC}} = 2.0\text{ V}$	80	22	-	ns
			$V_{\text{CC}} = 4.5\text{ V}$	16	8	-	ns
	$t_{\text{su}}$	set-up time $nJ, nK$ to $n\overline{CP}$	see <a href="#">Figure 6</a>				
$V_{\text{CC}} = 2.0\text{ V}$			80	22	-	ns	
$V_{\text{CC}} = 4.5\text{ V}$			16	8	-	ns	
$V_{\text{CC}} = 6.0\text{ V}$			14	6	-	ns	

**Table 8: Dynamic characteristics ...continued**  
 $GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$ ; see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_h$	hold time nJ, nK to nCP	see <a href="#">Figure 6</a>					
		$V_{CC} = 2.0\text{ V}$	3	-8	-	ns	
		$V_{CC} = 4.5\text{ V}$	3	-3	-	ns	
		$V_{CC} = 6.0\text{ V}$	3	-2	-	ns	
$f_{max}$	maximum clock frequency	see <a href="#">Figure 6</a>					
		$V_{CC} = 2.0\text{ V}$	6.0	23	-	MHz	
		$V_{CC} = 4.5\text{ V}$	30	70	-	MHz	
		$V_{CC} = 6.0\text{ V}$	35	83	-	MHz	
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	77	-	MHz	
$C_{PD}$	power dissipation capacitance per flip-flop	$V_I = GND$ to $V_{CC}$	[1] -	30	-	pF	
<b><math>T_{amb} = -40\text{ °C to }+85\text{ °C}</math></b>							
$t_{PHL}, t_{PLH}$	propagation delay nCP to nQ	see <a href="#">Figure 6</a>					
		$V_{CC} = 2.0\text{ V}$	-	-	200	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	40	ns	
	propagation delay nCP to nQ	$V_{CC} = 6.0\text{ V}$	-	-	34	ns	
		see <a href="#">Figure 6</a>					
		$V_{CC} = 2.0\text{ V}$	-	-	200	ns	
	propagation delay nCP to nQ	$V_{CC} = 4.5\text{ V}$	-	-	40	ns	
		$V_{CC} = 6.0\text{ V}$	-	-	34	ns	
		propagation delay nR to nQ, nQ	see <a href="#">Figure 7</a>				
	$V_{CC} = 2.0\text{ V}$		-	-	180	ns	
	$V_{CC} = 4.5\text{ V}$		-	-	36	ns	
	propagation delay nR to nQ, nQ	$V_{CC} = 6.0\text{ V}$	-	-	31	ns	
$t_{THL}, t_{TLH}$		output transition time	see <a href="#">Figure 6</a>				
			$V_{CC} = 2.0\text{ V}$	-	-	95	ns
	$V_{CC} = 4.5\text{ V}$		-	-	19	ns	
	$V_{CC} = 6.0\text{ V}$		-	-	16	ns	
$t_w$	nCP clock pulse width HIGH or LOW	see <a href="#">Figure 6</a>					
		$V_{CC} = 2.0\text{ V}$	100	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	20	-	-	ns	
	nR reset pulse width HIGH or LOW	$V_{CC} = 6.0\text{ V}$	17	-	-	ns	
		see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0\text{ V}$	100	-	-	ns	
	nR reset pulse width HIGH or LOW	$V_{CC} = 4.5\text{ V}$	20	-	-	ns	
		$V_{CC} = 6.0\text{ V}$	17	-	-	ns	
		$t_{rem}$	removal time nR to nCP	see <a href="#">Figure 7</a>			
	$V_{CC} = 2.0\text{ V}$			100	-	-	ns
	$V_{CC} = 4.5\text{ V}$			20	-	-	ns
	$V_{CC} = 6.0\text{ V}$			17	-	-	ns

**Table 8: Dynamic characteristics ...continued**  
 $GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$ ; see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_{su}$	set-up time nJ, nK to $\overline{nCP}$	see <a href="#">Figure 6</a>					
		$V_{CC} = 2.0\text{ V}$	100	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	20	-	-	ns	
		$V_{CC} = 6.0\text{ V}$	17	-	-	ns	
$t_h$	hold time nJ, nK to $\overline{nCP}$	see <a href="#">Figure 6</a>					
		$V_{CC} = 2.0\text{ V}$	3	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	3	-	-	ns	
		$V_{CC} = 6.0\text{ V}$	3	-	-	ns	
$f_{max}$	maximum clock frequency	see <a href="#">Figure 6</a>					
		$V_{CC} = 2.0\text{ V}$	4.8	-	-	MHz	
		$V_{CC} = 4.5\text{ V}$	24	-	-	MHz	
		$V_{CC} = 6.0\text{ V}$	28	-	-	MHz	
<b><math>T_{amb} = -40\text{ °C to }+125\text{ °C}</math></b>							
$t_{PHL}, t_{PLH}$	propagation delay $\overline{nCP}$ to nQ	see <a href="#">Figure 6</a>					
		$V_{CC} = 2.0\text{ V}$	-	-	240	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	48	ns	
	propagation delay $\overline{nCP}$ to $\overline{nQ}$	see <a href="#">Figure 6</a>					
		$V_{CC} = 2.0\text{ V}$	-	-	240	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	48	ns	
	propagation delay $\overline{nR}$ to nQ, $\overline{nQ}$	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0\text{ V}$	-	-	220	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	44	ns	
	$t_{THL}, t_{TLH}$	output transition time	see <a href="#">Figure 6</a>				
			$V_{CC} = 2.0\text{ V}$	-	-	110	ns
			$V_{CC} = 4.5\text{ V}$	-	-	22	ns
$t_w$	$\overline{nCP}$ clock pulse width HIGH or LOW	see <a href="#">Figure 6</a>					
		$V_{CC} = 2.0\text{ V}$	120	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	24	-	-	ns	
	$\overline{nR}$ reset pulse width HIGH or LOW	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0\text{ V}$	120	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	24	-	-	ns	
	$V_{CC} = 6.0\text{ V}$	20	-	-	ns		

**Table 8: Dynamic characteristics ...continued**  
*GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF; see [Figure 8](#).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{rem}$	removal time $n\bar{R}$ to $n\bar{CP}$	see <a href="#">Figure 7</a>				
		$V_{CC} = 2.0$ V	120	-	-	ns
		$V_{CC} = 4.5$ V	24	-	-	ns
		$V_{CC} = 6.0$ V	20	-	-	ns
$t_{su}$	set-up time $nJ, nK$ to $n\bar{CP}$	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	120	-	-	ns
		$V_{CC} = 4.5$ V	24	-	-	ns
		$V_{CC} = 6.0$ V	20	-	-	ns
$t_h$	hold time $nJ, nK$ to $n\bar{CP}$	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	3	-	-	ns
		$V_{CC} = 4.5$ V	3	-	-	ns
		$V_{CC} = 6.0$ V	3	-	-	ns
$f_{max}$	maximum clock frequency	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.0$ V	4.0	-	-	MHz
		$V_{CC} = 4.5$ V	20	-	-	MHz
		$V_{CC} = 6.0$ V	24	-	-	MHz

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

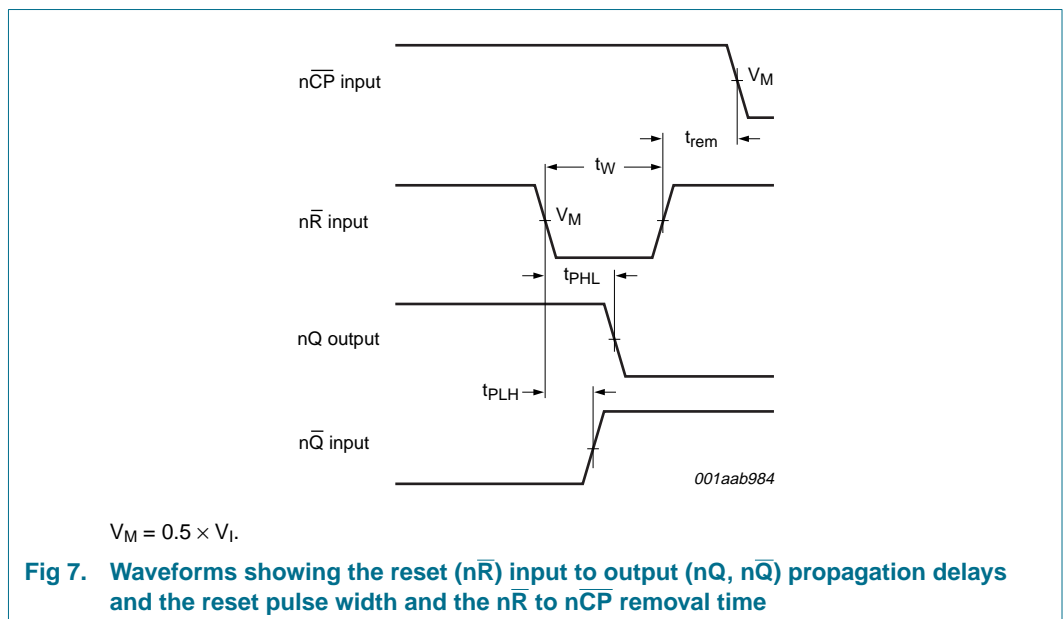
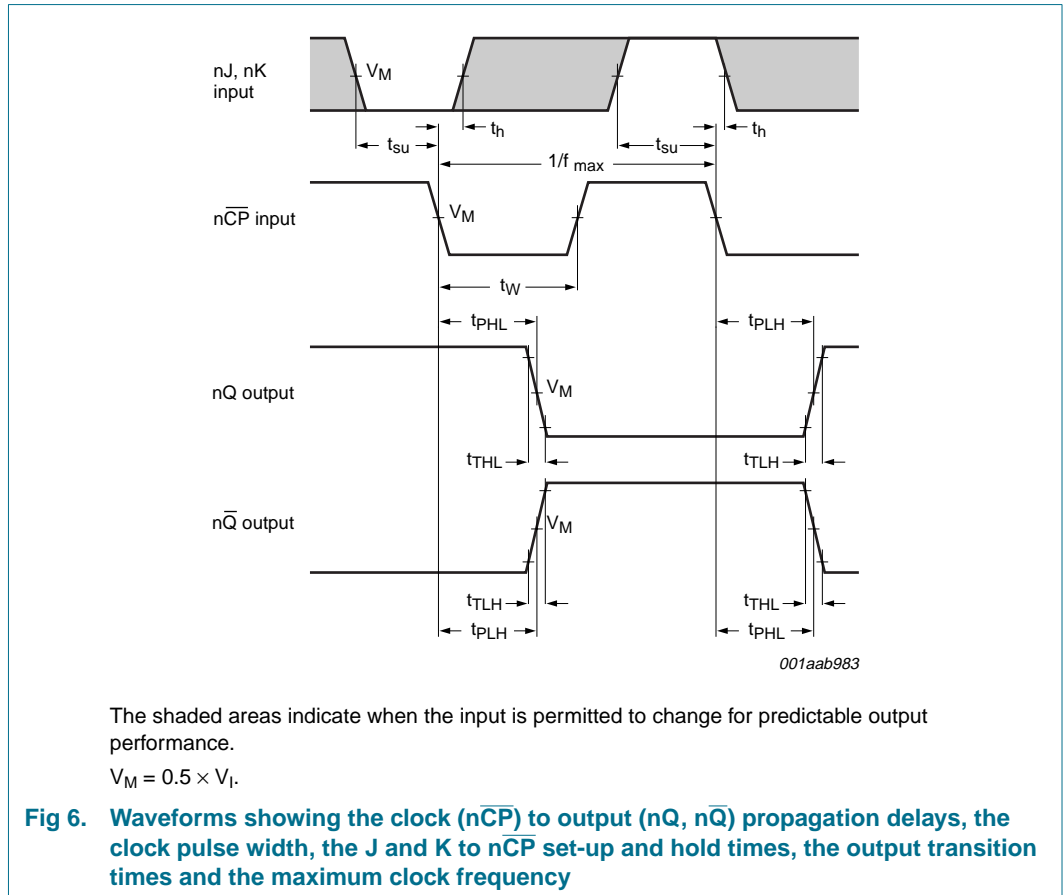
$C_L$  = output load capacitance in pF;

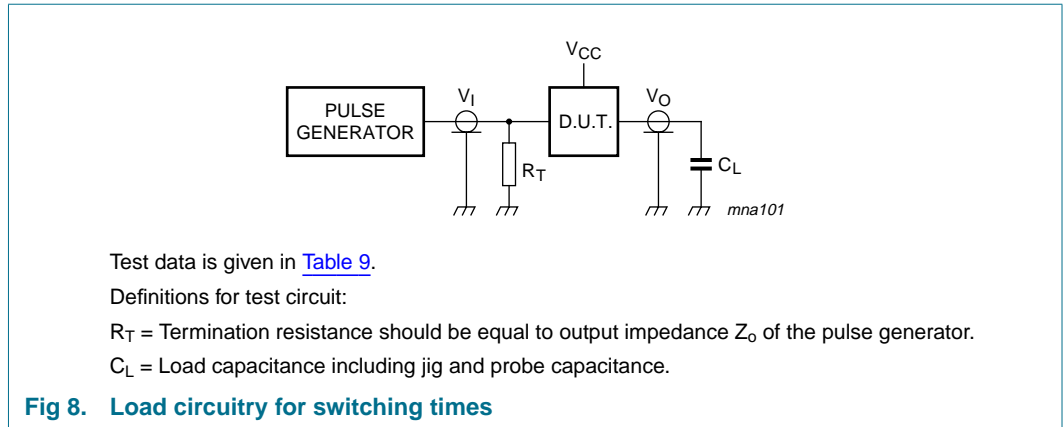
$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

12. Waveforms





**Table 9: Test data**

Supply	Input		Load
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$
2.0 V	$V_{CC}$	6 ns	50 pF
4.5 V	$V_{CC}$	6 ns	50 pF
6.0 V	$V_{CC}$	6 ns	50 pF
5.0 V	$V_{CC}$	6 ns	15 pF

13. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

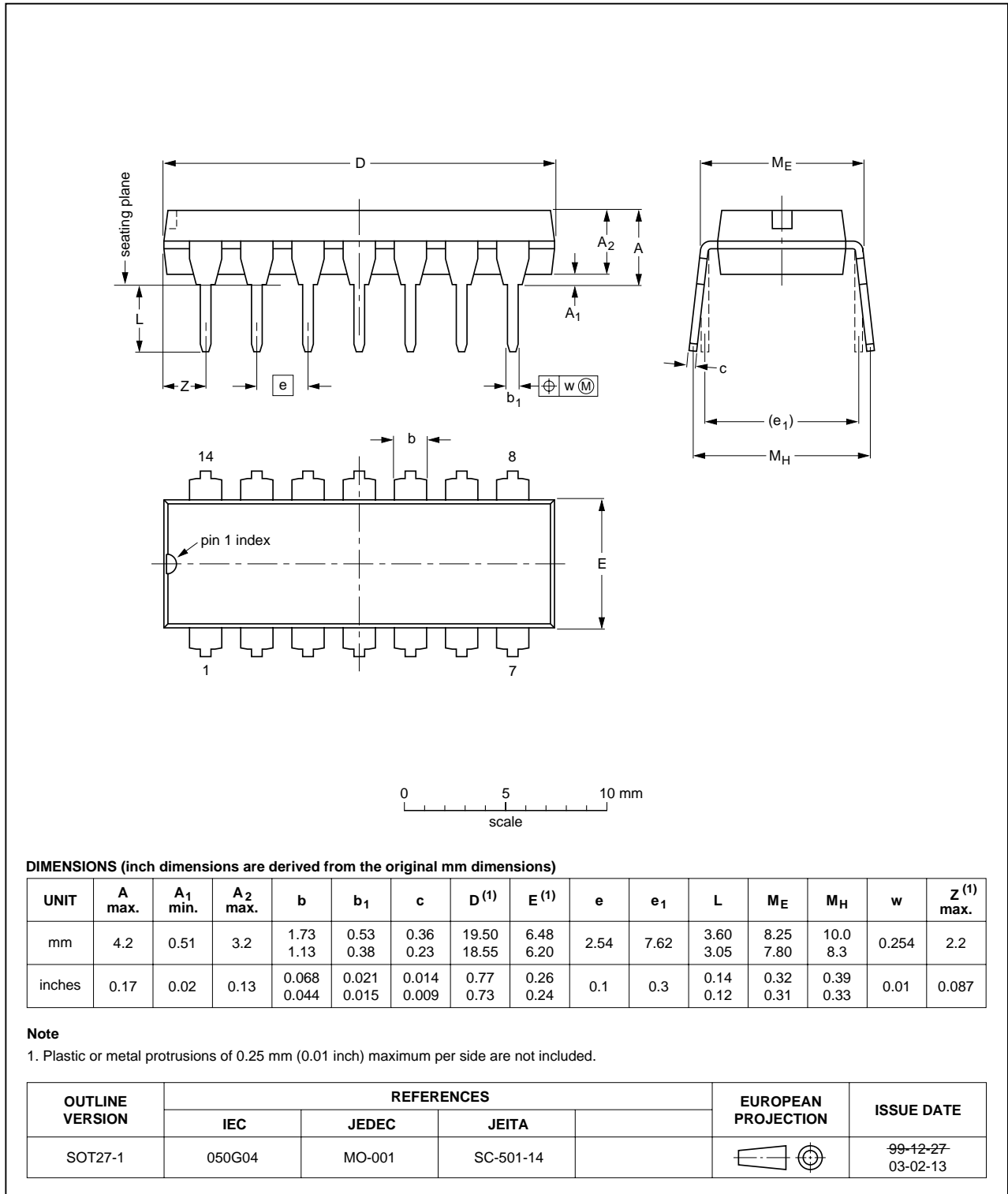


Fig 9. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

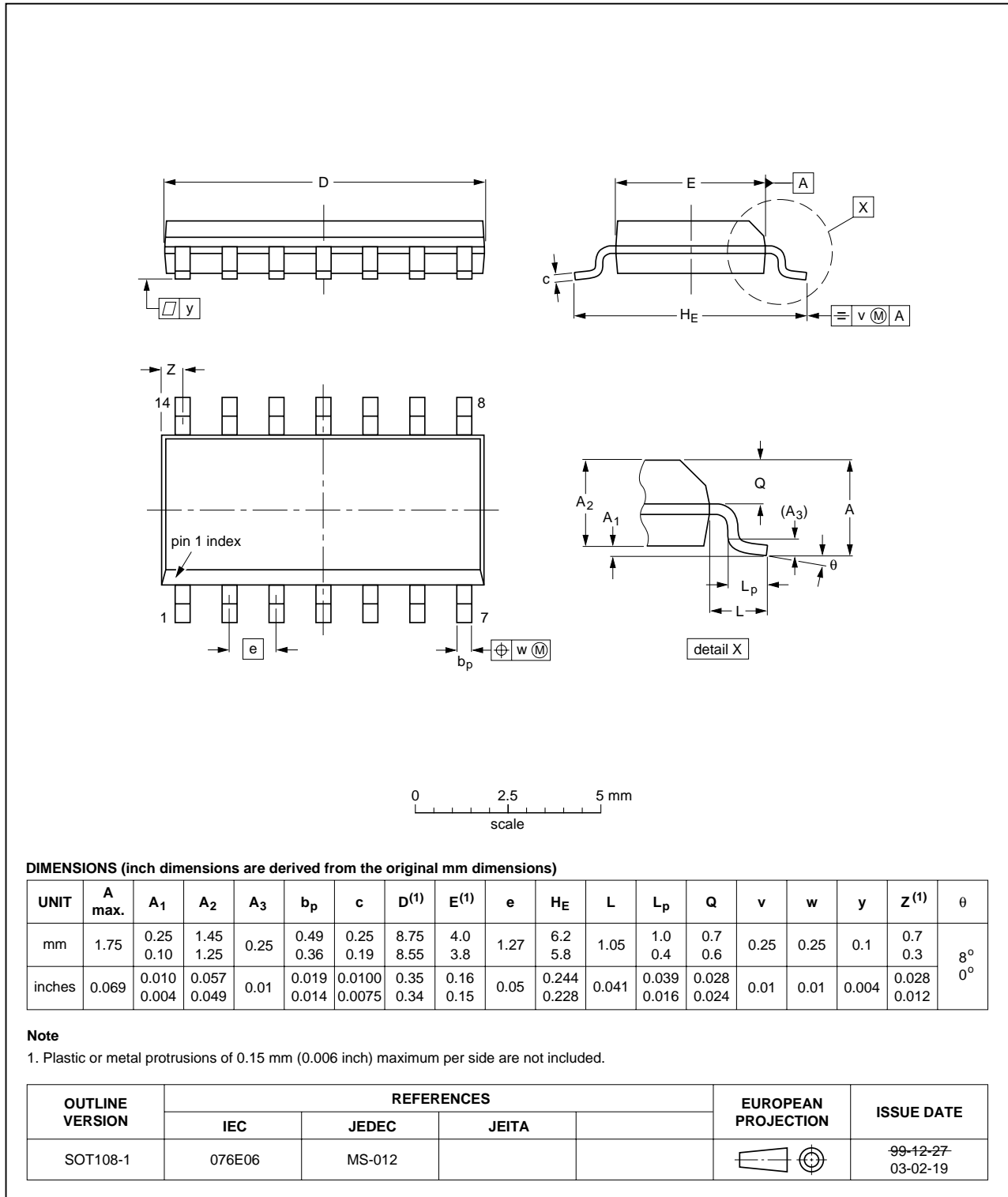


Fig 10. Package outline SOT108-1 (SO14)



SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

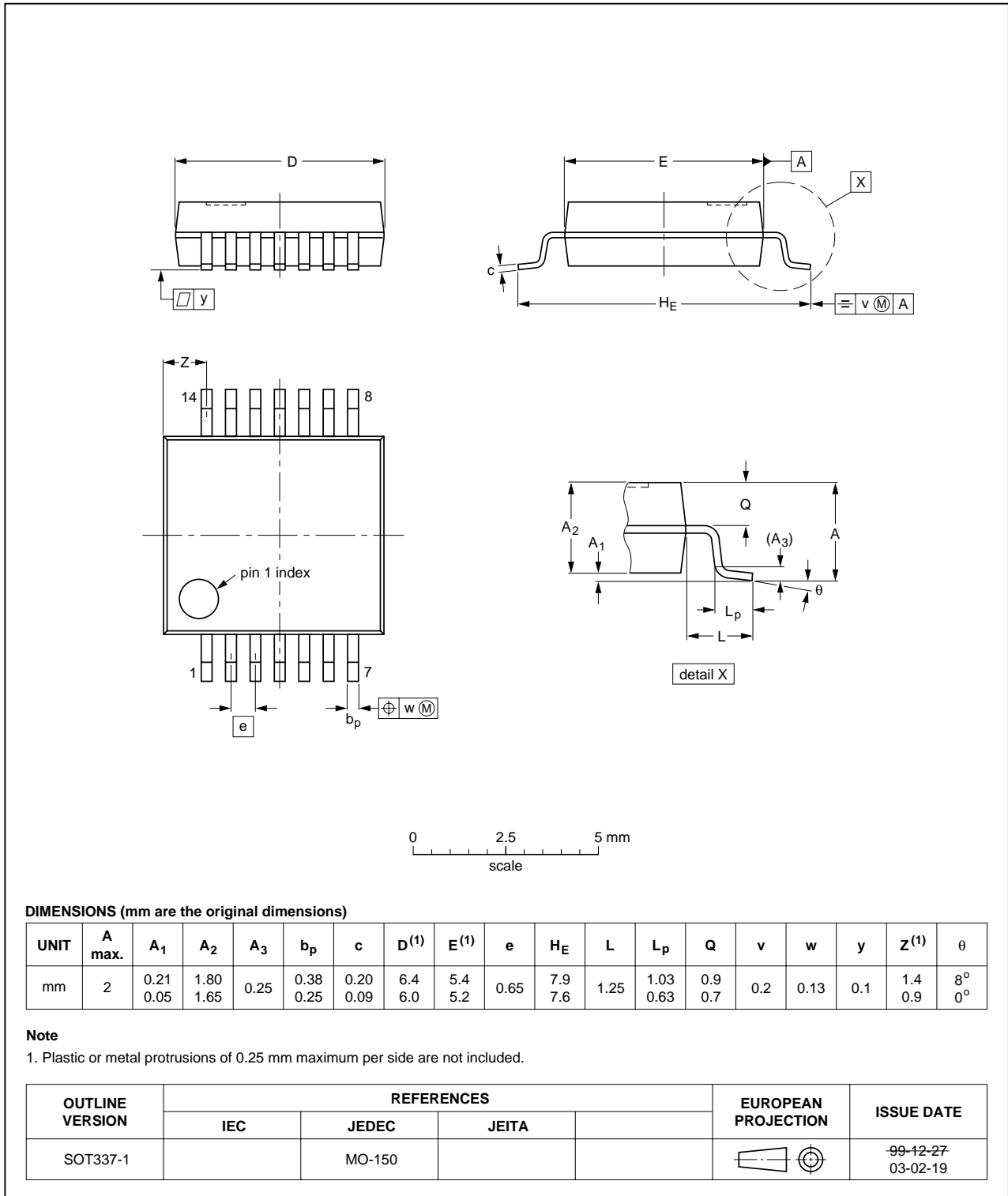


Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

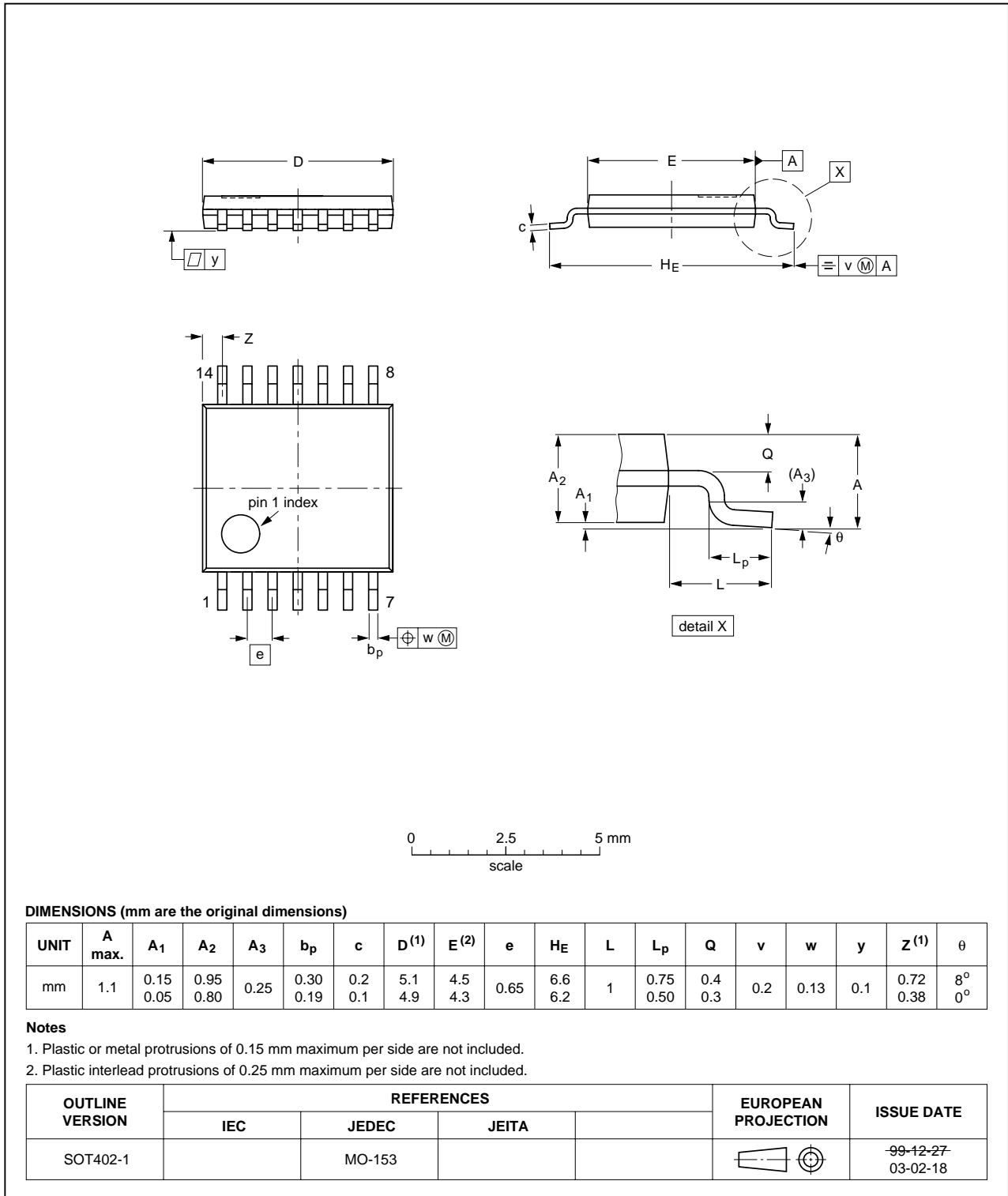


Fig 12. Package outline SOT402-1 (TSSOP14)

## 14. Revision history

**Table 10: Revision history**

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC73_3	20041112	Product data sheet	-	9397 750 13815	74HC_HCT73_CNV_2
Modifications:					
					<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors.</li><li>• Removed type number 74HCT73.</li><li>• Inserted family specification.</li></ul>
74HC_HCT73_CNV_2	19970911	Product specification	-	-	74HC_HCT73_1
74HC_HCT73_1	19901201	Product specification	-	-	-

## 15. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 16. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## 18. Contact information

For additional information, please visit: <http://www.semiconductors.philips.com>

For sales office addresses, send an email to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com)

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Date of release: 12 November 2004  
Document number: 9397 750 13815

Published in The Netherlands

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