125 MHz AMPLIFIER AND DIVIDER-BY-32/33

The silicon monolithic integrated circuit SAA1059 is designed as a programmable-ratio divide-by-32/33 prescaler. It is intended for use in digital radio tuning systems and frequency counters in radio applications with an input frequency range from 0,5 to 125 MHz. The high-frequency inputs are differential inputs of a preamplifier for handling a.m. as well as f.m. oscillator signals. One output set provides complementary ECL levels by emitter followers and a second output buffer set is intended to drive MOS circuits by open collectors.

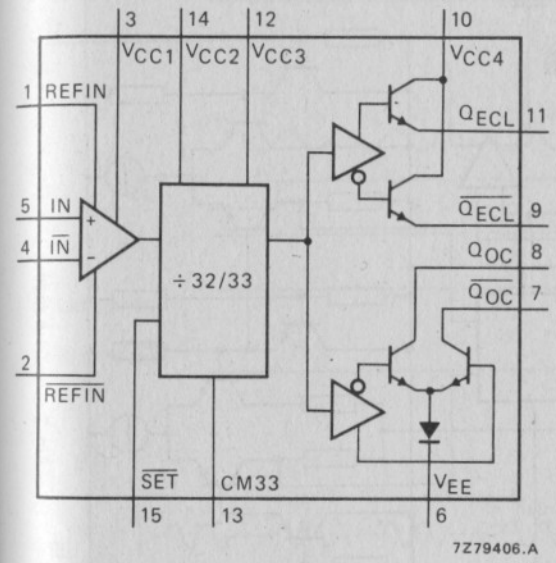


Fig. 1 Block diagram.

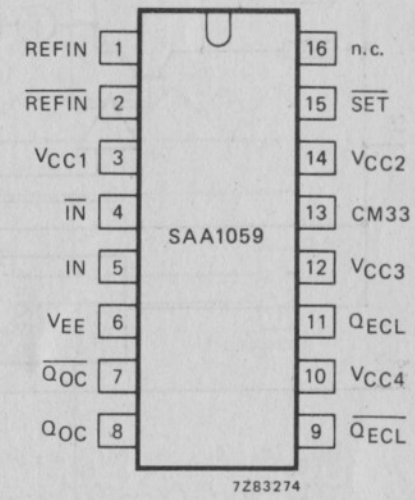


Fig. 2 Pin diagram.
V_{CC2} = 5 V (see Fig. 6)
V_{EE} = 0 V (ground)
Pin 16 preferably connected to V_{EE}

QUICK REFERENCE DATA

Supply voltage	V_B	max.	14	V
	V_{CC2}	typ.	5 ± 10%	V
Input frequency range	f_i		0,5 to 125	MHz
Input voltage range				
f = 0,5 to 30 MHz	$V_{i(rms)}$		5 to 100	mV
f = 30 to 125 MHz	$V_{i(rms)}$		10 to 100	mV
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	typ.	760	mW

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

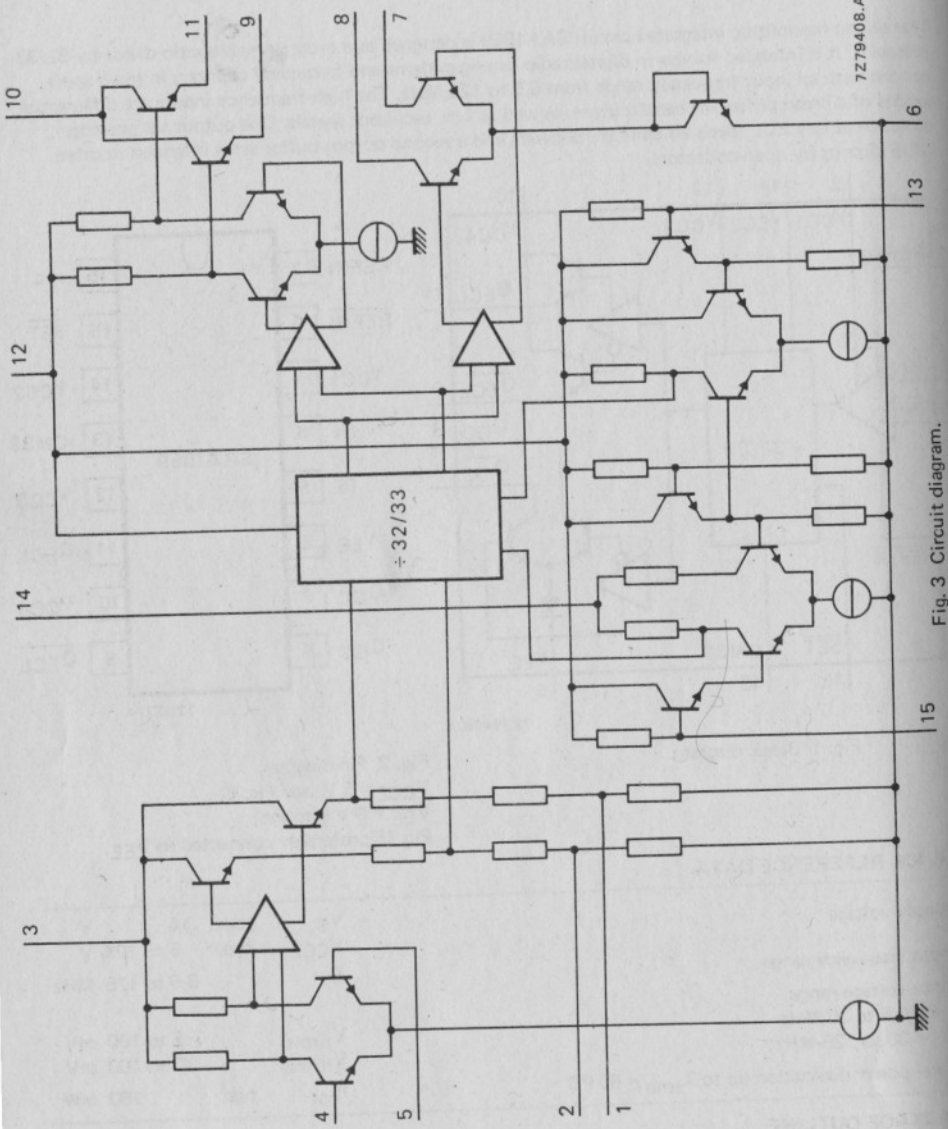
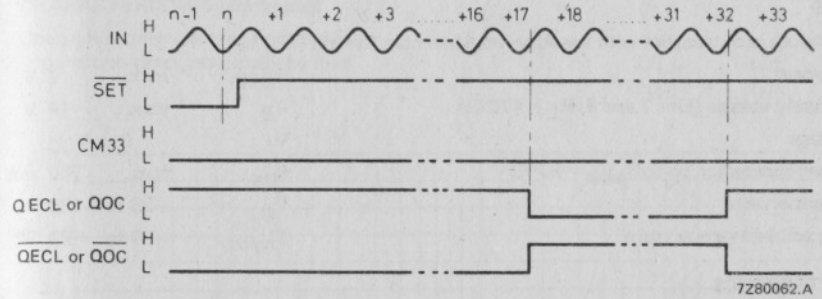
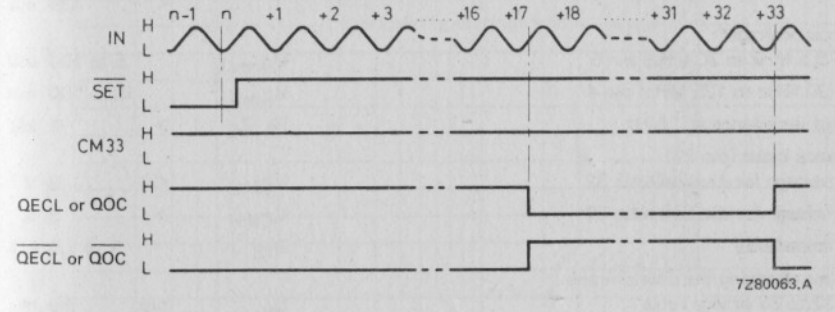


Fig. 3 Circuit diagram.





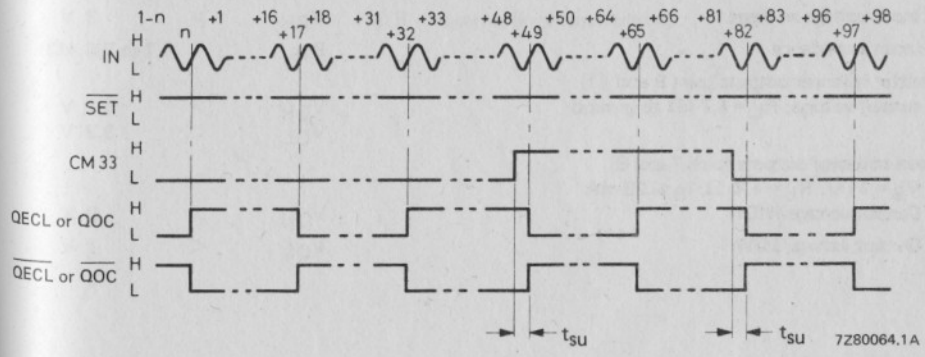


Fig. 4 Timing diagrams of programmable frequency dividing.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC2}	max.	7 V
Output supply voltage (pins 7 and 8, R_L = 470 Ω)	V_B	max.	14 V
Input voltage	V_I	0 to V_{CC}	
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	760 mW
Storage temperature	T_{stg}	−25 to + 125	°C
Operating ambient temperature	T_{amb}	−20 to + 80	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC} = 5 V; V_B = 9 V; T_{amb} = 25 °C; unless otherwise specified.

Supply current ($I_3 + I_{10} + I_{12} + I_{14}$)*	I_{CC}	typ.	110 mA
		<	135 mA
Count input voltage*			
A.M. (0,5 MHz to 30 MHz) pin 5	$V_{i(rms)}$	5 to 100	mV
F.M. (30 MHz to 125 MHz) pin 4	$V_{i(rms)}$	10 to 100	mV
A.C. input impedance at 1 MHz	Z_4, Z_5	>	1 kΩ
Count mode input (pin 13)			
input voltage for division-ratio 32	V_{CML}	<	2 V
input voltage for division-ratio 33	V_{CMH}	>	3 V
input impedance	Z_{13}	1 to 1,5	kΩ
Set-up time changing the division-ratio from 32 to 33 or vice versa	t_{su}	typ.	50 ns
Reset (pin 15)			
input voltage reset	V_{RL}	<	2 V
input voltage no reset	V_{RH}	>	3 V
input impedance	Z_{15}	1,7 to 2,6	kΩ
Emitter follower outputs (pins 9 and 11)			
output voltage; R_L = 4,7 kΩ to ground	V_{OH}	>	3,7 V
	V_{OL}	<	3,3 V
Open collector outputs (pins 7 and 8)			
V_B = 11 V; R_L = 470 Ω; $I_B \leqslant$ 20 mA			
Output voltage HIGH	V_{OH}	>	9 V
Output voltage LOW	V_{OL}	<	2 V

* See Fig. 6.

SAA1059

CHARACTERISTICS (continued)

Open collector outputs (pins 7 and 8) transition times, no capacitive load

	t_{TLH}	typ.	15 ns
	t_{THL}	typ.	12 ns

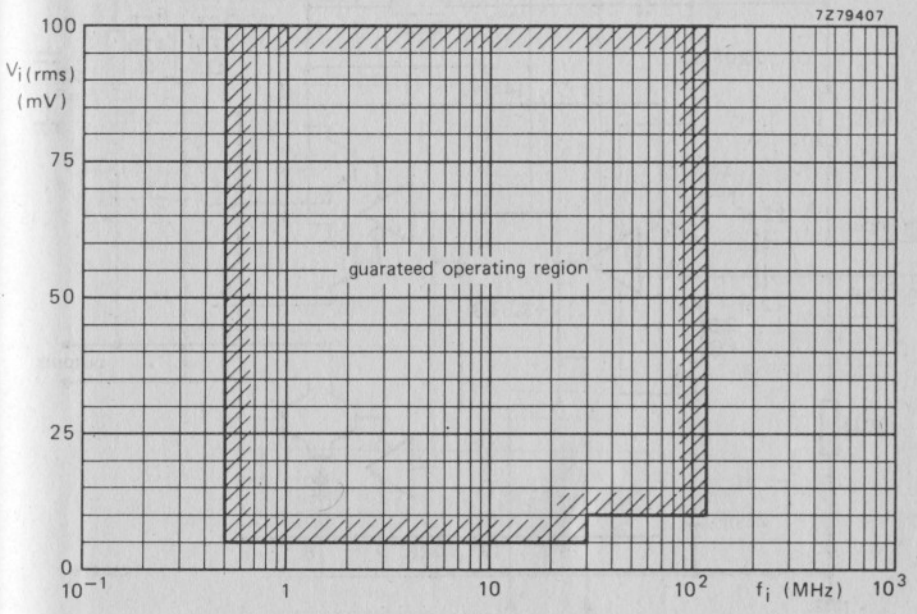


Fig. 5 Triggering level requirements.

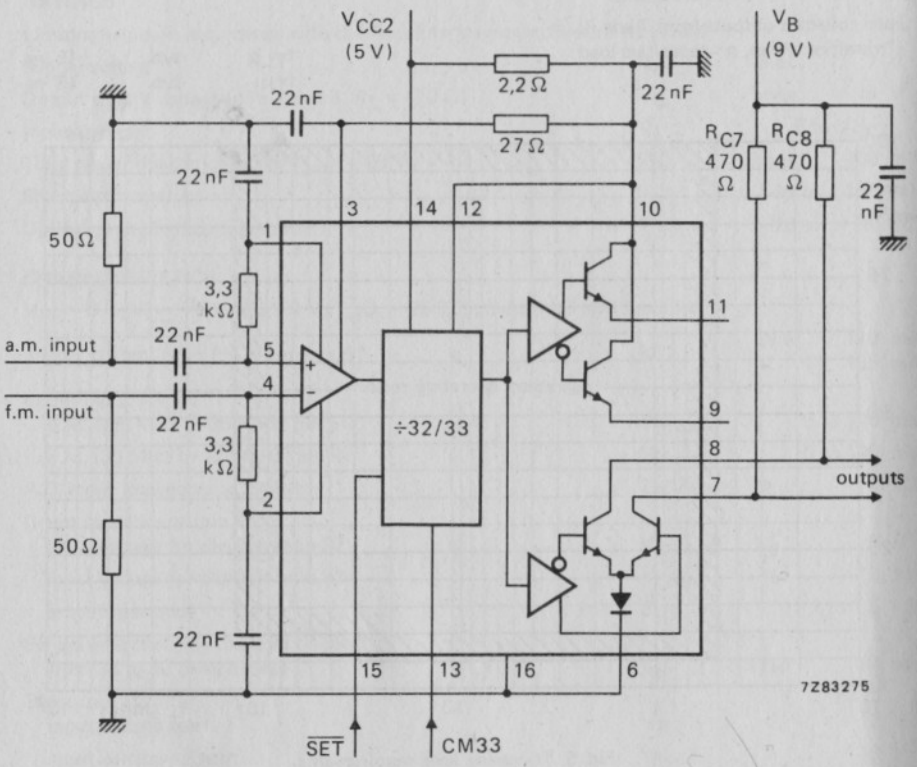
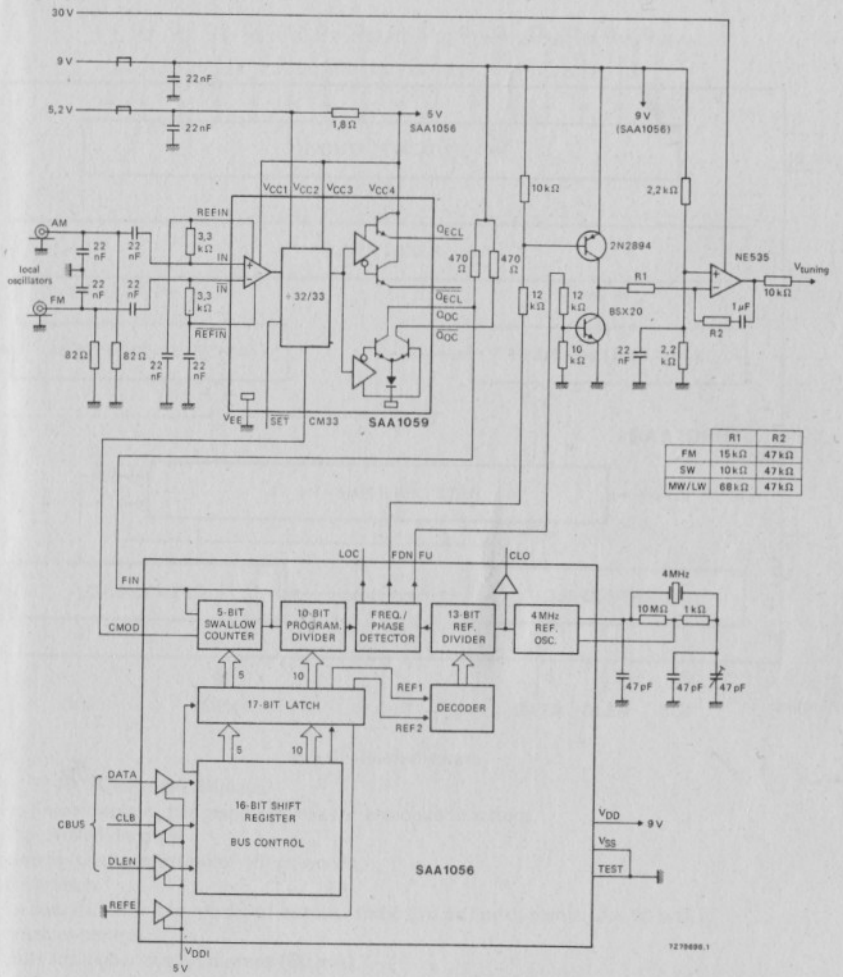


Fig. 6 Test circuit.

APPLICATION INFORMATION



	R1	R2
FM	15 kΩ	47 kΩ
SW	10 kΩ	47 kΩ
MW/LW	68 kΩ	47 kΩ

Fig. 7 A practical digital frequency synthesizer.