

## 3.3 V Dual LVTTTL to Differential LVPECL Translator

### FEATURES

- 450 ps (typ) Propagation Delay
- Operating Range:  $V_{CC}$  3.0 V to 3.8 with  $GND = 0$  V
- <50 ps (max) Output to Output Skew
- Built-in Temperature Compensation
- Drop in Compatible to MC100LVELT22

### APPLICATIONS

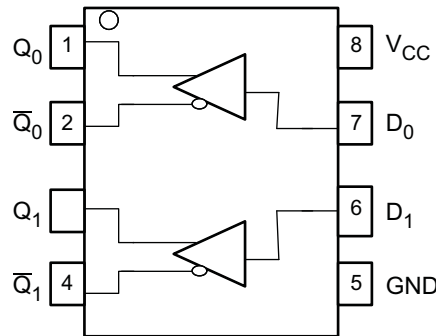
- Data and Clock Transmission Over Backplane
- Signaling Level Conversion for Clock or Data

### DESCRIPTION

The SN65ELT22 is a dual LVTTTL to differential LVPECL translator buffer. It operates on +3V supply and ground only. The output is driven default high when the inputs are left floating or unused. The low output skew makes the device the ideal solution for clock or data signal translation.

The SN65LVELT22 is housed in an industry standard SOIC-8 package and is also available in TSSOP-8 package option.

### PINOUT ASSIGNMENT



**Table 1. Pin Description**

| PIN                                        | FUNCTION         |
|--------------------------------------------|------------------|
| $D_0, D_1$                                 | TTL inputs       |
| $Q_0, \overline{Q}_0, Q_1, \overline{Q}_1$ | PECL/ECL outputs |
| $V_{CC}$                                   | Positive supply  |
| GND                                        | Ground           |

### ORDERING INFORMATION<sup>(1)</sup>

| PART NUMBER    | PART MARKING | PACKAGE    | LEAD FINISH |
|----------------|--------------|------------|-------------|
| SN65LVELT22D   | SN65LVELT22  | SOIC       | NiPdAu      |
| SN65LVELT22DGK | SN65LVELT22  | SOIC-TSSOP | NiPdAu      |

(1) Leadless device options not initially available. Contact TI sales representative for further details.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|                                             |                    | VALUE      | UNIT |
|---------------------------------------------|--------------------|------------|------|
| Absolute PECL mode supply voltage, $V_{CC}$ | $GND = 0\text{ V}$ | 6          | V    |
| $V_{IN}$ input voltage                      | $V_I \leq V_{CC}$  | 6          | V    |
| Output current                              | Continuous         | 50         | mA   |
|                                             | Surge              | 100        |      |
| Operating temperature range                 |                    | –40 to 85  | °C   |
| Storage temperature range                   |                    | –65 to 150 | °C   |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## POWER DISSIPATION RATINGS

| PACKAGE    | CIRCUIT BOARD MODEL | POWER RATING<br>$T_A < 25^\circ\text{C}$<br>(mW) | THERMAL RESISTANCE,<br>JUNCTION TO AMBIENT<br>NO AIRFLOW | DERATING FACTOR<br>$T_A > 25^\circ\text{C}$<br>(mW/°C) | POWER RATING<br>$T_A = 85^\circ\text{C}$<br>(mW) |
|------------|---------------------|--------------------------------------------------|----------------------------------------------------------|--------------------------------------------------------|--------------------------------------------------|
| SOIC       | Low-K               | 719                                              | 139                                                      | 7                                                      | 288                                              |
|            | High-K              | 840                                              | 119                                                      | 8                                                      | 336                                              |
| SOIC-TSSOP | Low-K               | 469                                              | 213                                                      | 5                                                      | 188                                              |
|            | High-K              | 527                                              | 189                                                      | 5                                                      | 211                                              |

## THERMAL CHARACTERISTICS

|               | PARAMETER                            | PACKAGE    | VALUE | UNIT |
|---------------|--------------------------------------|------------|-------|------|
| $\theta_{JB}$ | Junction-to Board Thermal Resistance | SOIC       | 79    | °C/W |
|               |                                      | SOIC-TSSOP | 120   |      |
| $\theta_{JC}$ | Junction-to Case Thermal Resistance  | SOIC       | 98    | °C/W |
|               |                                      | SOIC-TSSOP | 74    |      |

## KEY ATTRIBUTES

| CHARACTERISTICS                                     | VALUE                 |
|-----------------------------------------------------|-----------------------|
| Moisture sensitivity level                          | Level 1               |
| Flammability rating (Oxygen Index: 28 to 34)        | UL 94 V-0 at 0.125 in |
| ESD-HBM                                             | 4 kV                  |
| ESD-machine model                                   | 200 V                 |
| ESD-charge device model                             | 2 kV                  |
| Meets or exceeds JEDEC Spec EIA/JESD78 latchup test |                       |

**PECL DC CHARACTERISTICS<sup>(1)</sup> ( $V_{CC} = 3.3\text{ V}$ ,  $GND = 0.0\text{ V}$ <sup>(2)</sup>)**

| CHARACTERISTICS |                                    | –40°C |      |      | 25°C |      |      | 85°C |      |      | UNIT |
|-----------------|------------------------------------|-------|------|------|------|------|------|------|------|------|------|
|                 |                                    | MIN   | TYP  | MAX  | MIN  | TYP  | MAX  | MIN  | TYP  | MAX  |      |
| $I_{CC}$        | Power Supply Current               |       | 23   | 33   |      | 25   | 33   |      | 26   | 33   | mA   |
| $V_{OH}$        | Output HIGH Voltage <sup>(3)</sup> | 2275  | 2317 | 2420 | 2275 | 2331 | 2420 | 2275 | 2343 | 2420 | mV   |
| $V_{OL}$        | Output LOW Voltage <sup>(3)</sup>  | 1490  | 1558 | 1680 | 1490 | 1556 | 1680 | 1490 | 1555 | 1680 | mV   |

- (1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input parameters vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $\pm 0.15\text{ V}$
- (3) Outputs are terminated through a 50- $\Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .

**TTL DC CHARACTERISTICS<sup>(1)</sup> ( $V_{CC} = 3.3\text{ V}$ ;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ )**

| CHARACTERISTIC |                           | CONDITION                |  | MIN | TYP | MAX  | UNIT          |
|----------------|---------------------------|--------------------------|--|-----|-----|------|---------------|
| $I_{IH}$       | Input HIGH current        | $V_{IN} = 2.7\text{ V}$  |  |     |     | 20   | $\mu\text{A}$ |
| $I_{IHH}$      | Input HIGH current max    | $V_{IN} = V_{CC}$        |  |     |     | 100  | $\mu\text{A}$ |
| $I_{IL}$       | Input LOW current         | $V_{IN} = 0.5\text{ V}$  |  |     |     | –0.2 | mA            |
| $V_{IK}$       | Input clamp diode voltage | $I_{IN} = -18\text{ mA}$ |  |     |     | –1.2 | V             |
| $V_{IH}$       | Input HIGH voltage        |                          |  | 2.0 |     |      | V             |
| $V_{IL}$       | Input LOW voltage         |                          |  |     |     | 0.8  | V             |

- (1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**AC CHARACTERISTICS<sup>(1)</sup> ( $V_{CC} = 3.3\text{ V}$ ;  $GND = 0.0\text{ V}$ )**

| CHARACTERISTIC    |                                                                       | –40°C |      |     | 25°C |      |     | 85°C |      |     | UNIT |
|-------------------|-----------------------------------------------------------------------|-------|------|-----|------|------|-----|------|------|-----|------|
|                   |                                                                       | MIN   | TYP  | MAX | MIN  | TYP  | MAX | MIN  | TYP  | MAX |      |
| $f_{MAX}$         | Max switching frequency <sup>(2)</sup> , see <a href="#">Figure 5</a> |       | 1750 |     |      | 1750 |     |      | 1700 |     | MHz  |
| $t_{PLH}/t_{PHL}$ | Propagation delay to output at 1.5V, see <a href="#">Figure 4</a>     | 200   | 425  | 550 | 200  | 445  | 550 | 200  | 460  | 550 | ps   |
| $t_{SKEW}$        | Within – device skew <sup>(3)</sup>                                   |       | 20   | 50  |      | 20   | 50  |      | 20   | 50  | ps   |
|                   | Device-to-device skew <sup>(4)</sup>                                  |       | 30   | 100 |      | 30   | 100 |      | 30   | 100 |      |
| $t_{JITTER}$      | Random clock jitter (RMS)                                             |       | 0.5  | 1.0 |      | 0.5  | 1.0 |      | 0.5  | 1.0 | ps   |
| $t_r/t_f$         | Output rise/fall times Q (20%–80%)                                    | 300   |      | 500 | 300  |      | 500 | 300  |      | 500 | ps   |

- (1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Maximum switching frequency measured at output amplitude of 300 mV<sub>pp</sub>.
- (3) This is measured between outputs under the identical transitions and conditions on any one device.
- (4) Device-Device Skew is defined as identical transitions at identical  $V_{CC}$  levels.

## Typical Termination for Output Driver

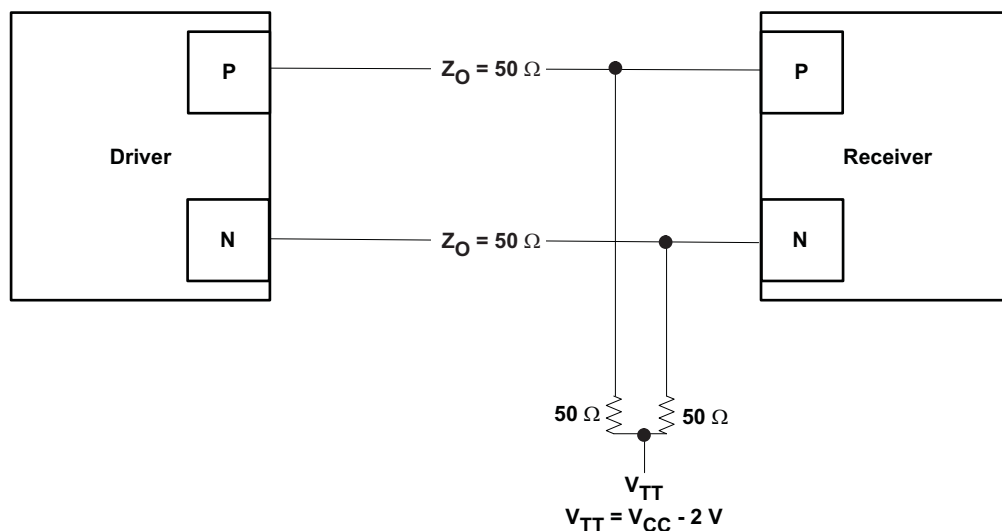


Figure 1. Termination for Output Driver

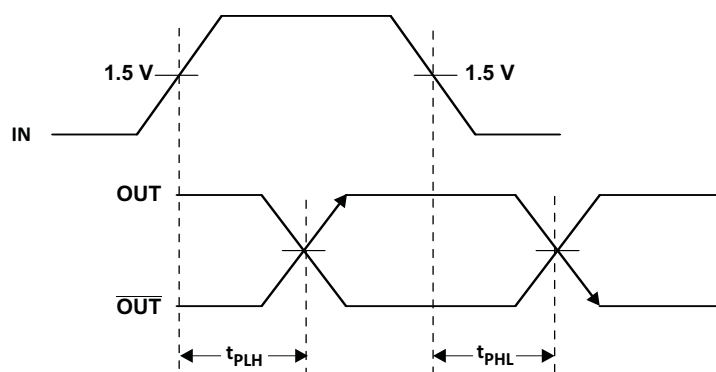


Figure 2. Output Propagation Delay

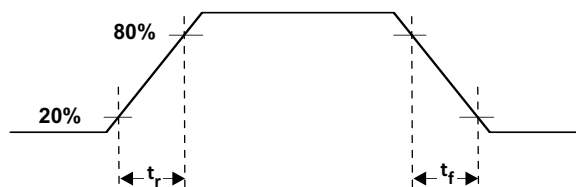
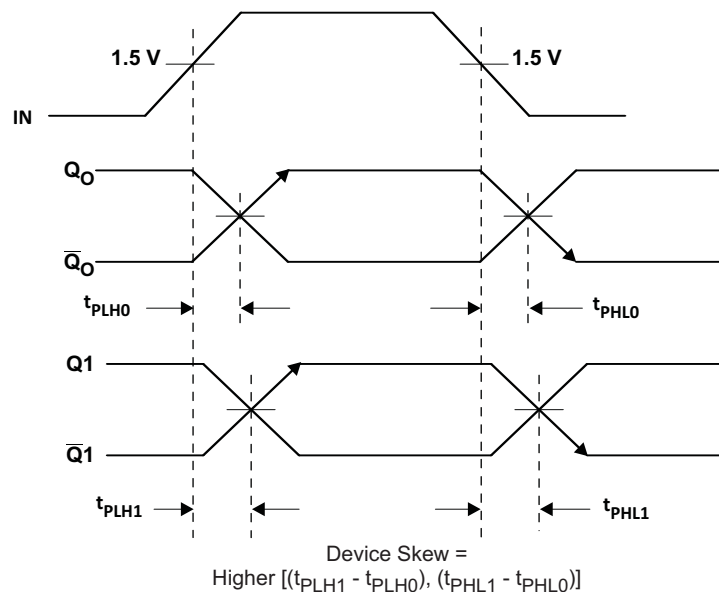
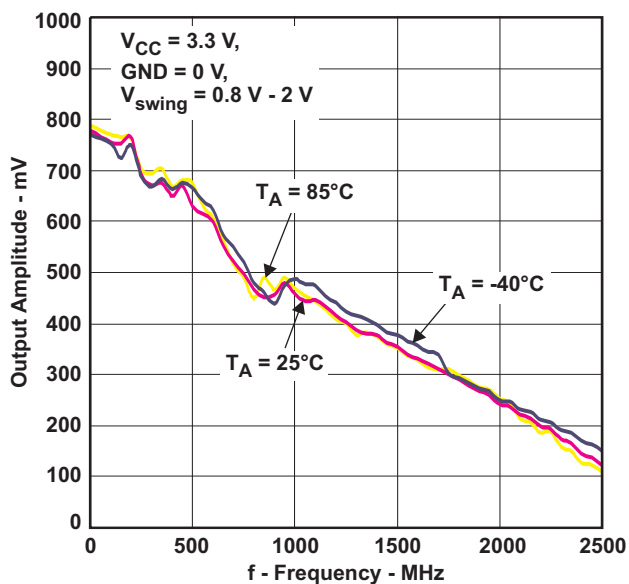


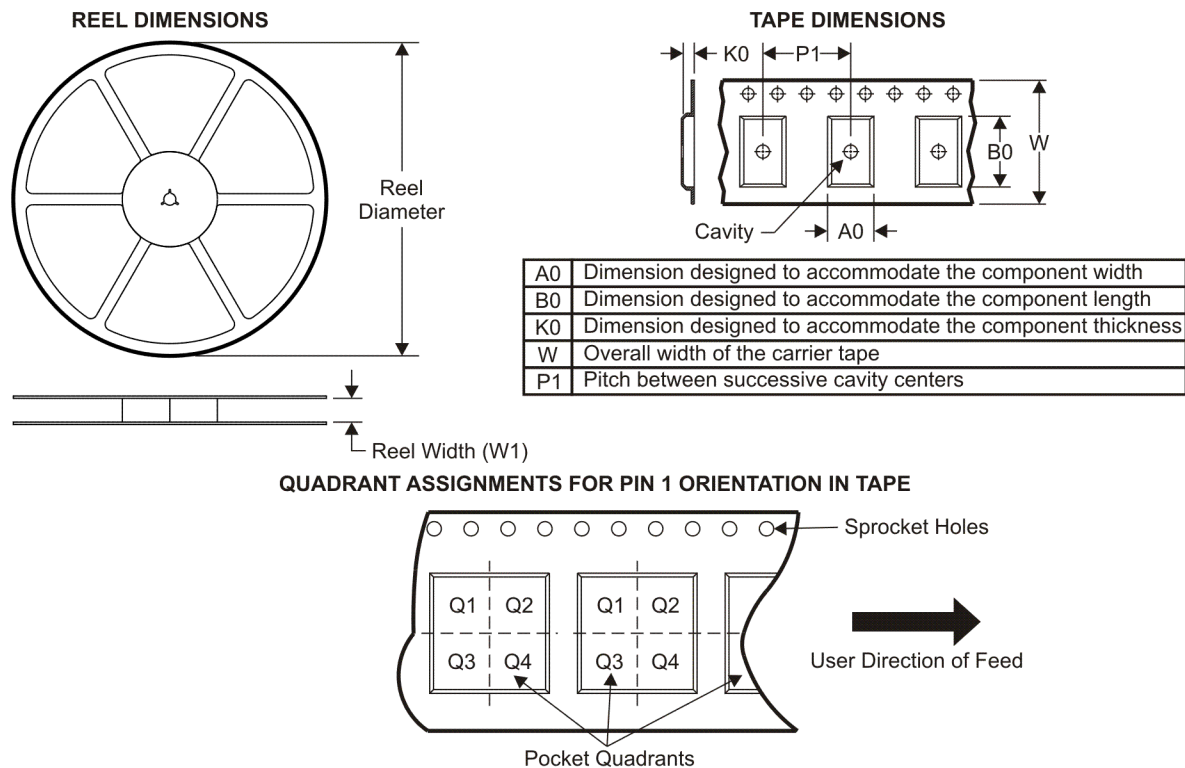
Figure 3. Output Rise and Fall Times



**Figure 4. Device Skew**



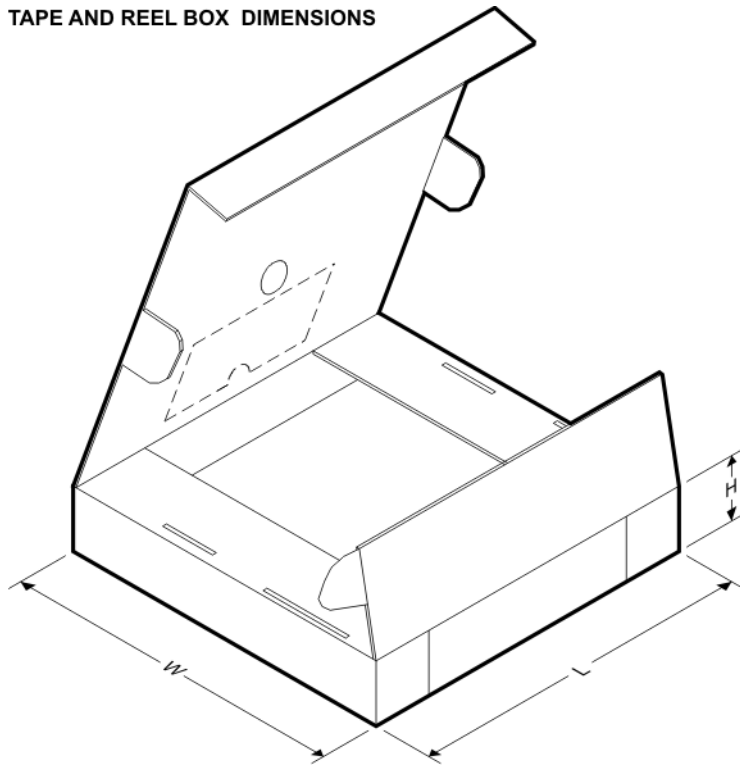
**Figure 5. Output Amplitude vs. Frequency**

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LVELT22DGKR | MSOP         | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| SN65LVELT22DR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

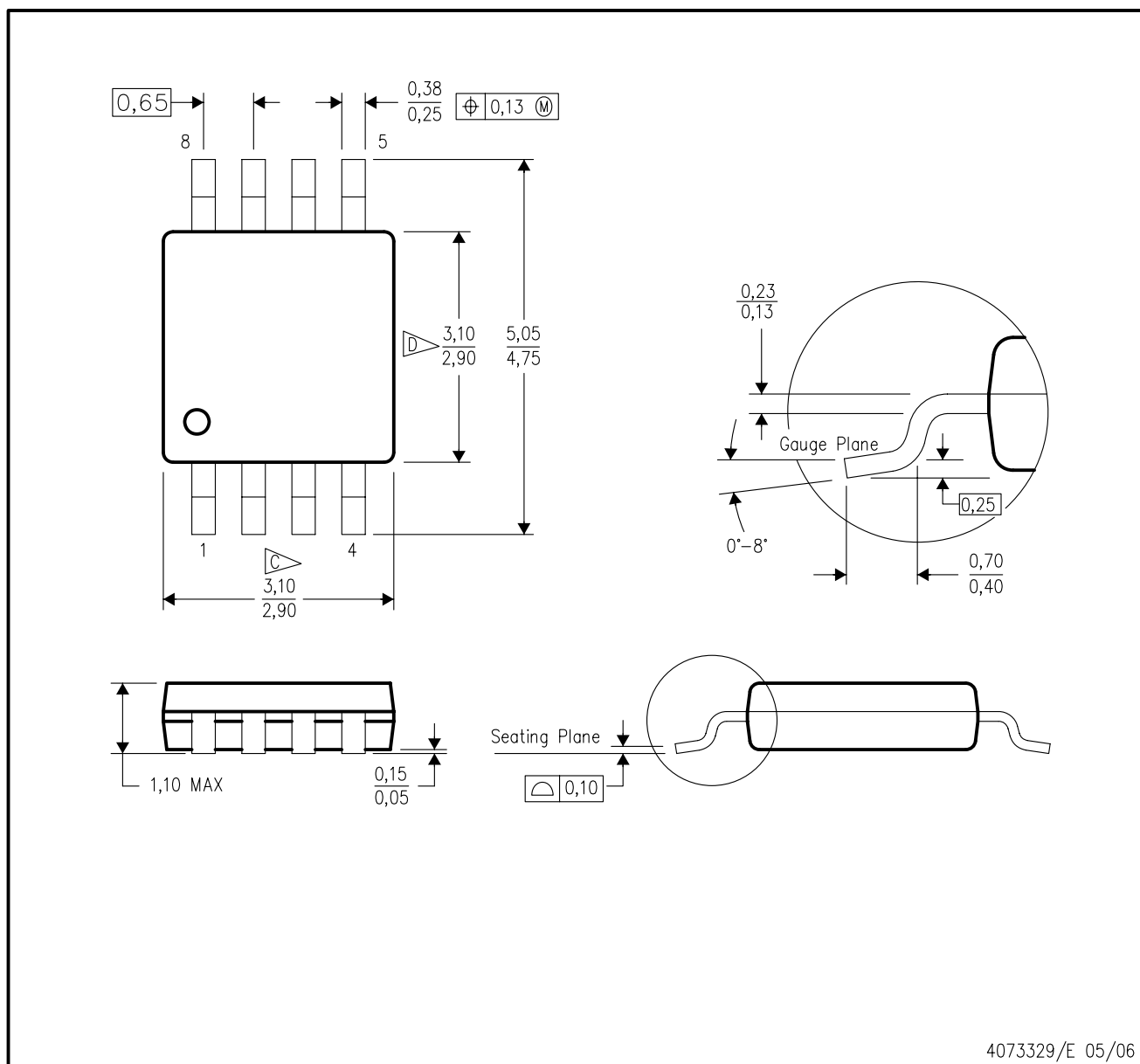


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LVELT22DGKR | MSOP         | DGK             | 8    | 2500 | 346.0       | 346.0      | 29.0        |
| SN65LVELT22DR   | SOIC         | D               | 8    | 2500 | 346.0       | 346.0      | 29.0        |

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



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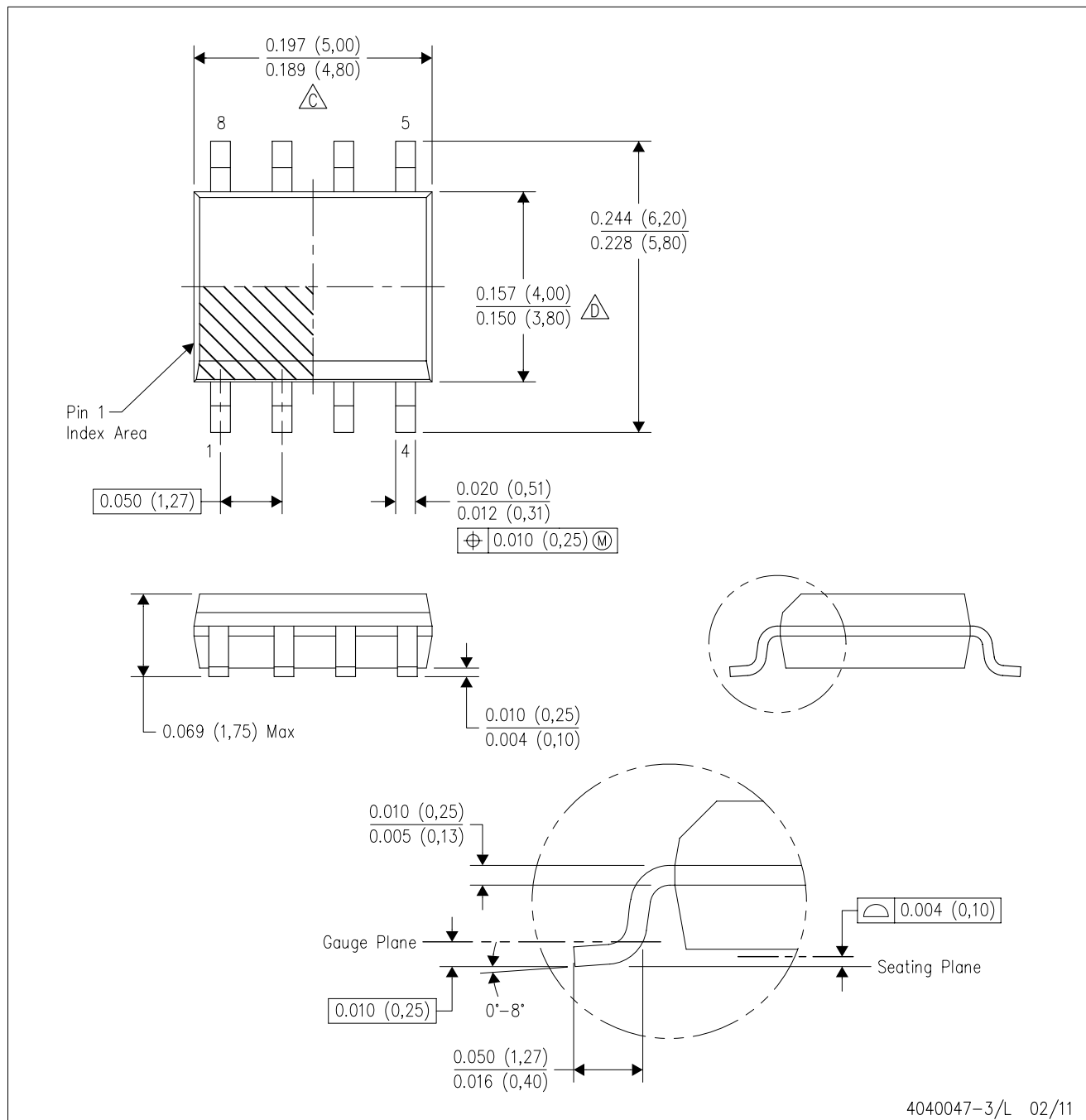
## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



D (R-PDSO-G8)

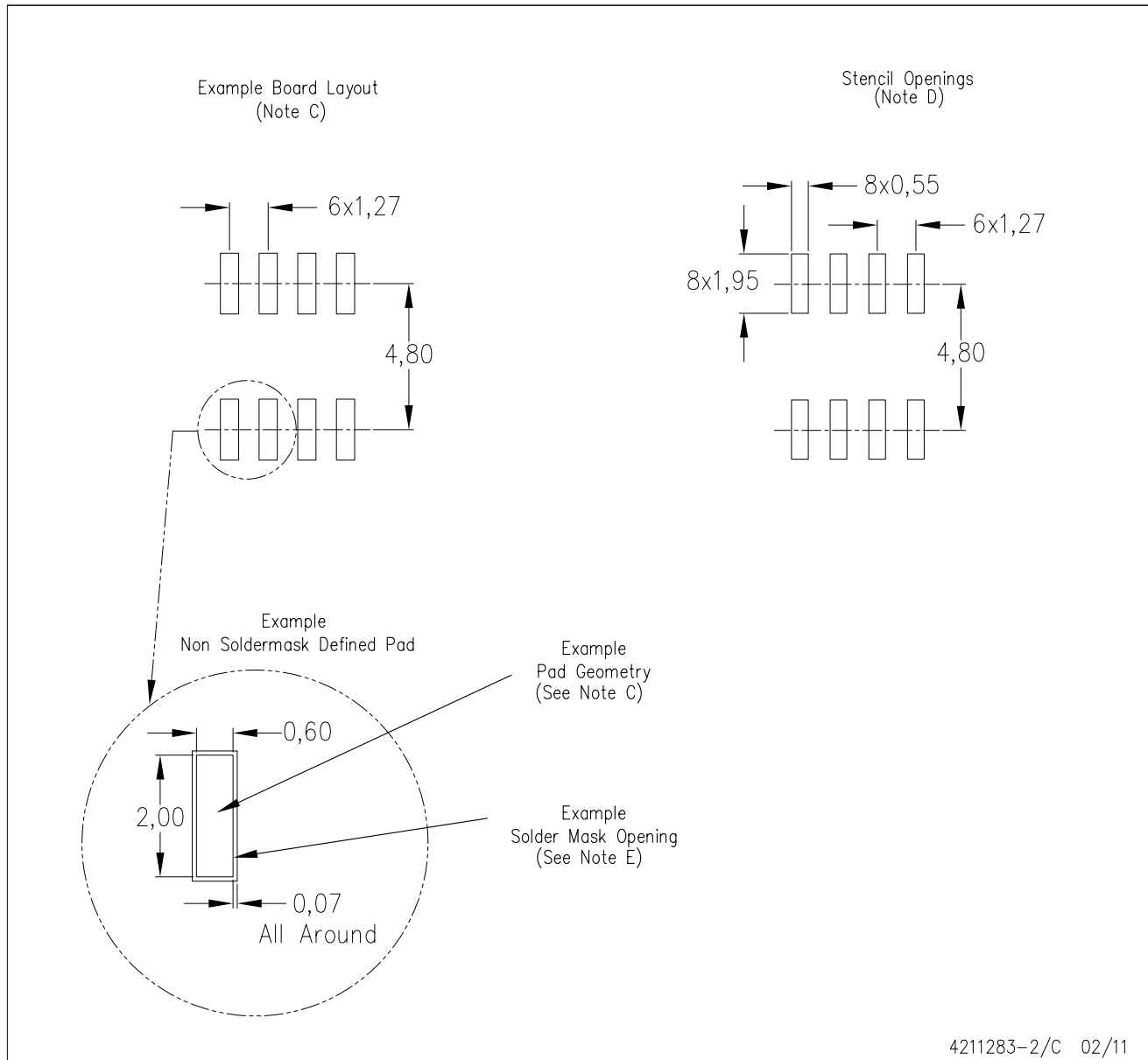
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/C 02/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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### Applications

|                               |                                                                                          |
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