# Product Change Notification - SYST-08FZMW895

**Date:**

09 May 2019

**Product Category:**

Memory

**Affected CPNs:**

**Notification subject:**

Data Sheet - 24AA02/24LC02B/24FC02 Data Sheet

**Notification text:**

SYST-08FZMW895

Microchip has released a new DeviceDoc for the 24AA02/24LC02B/24FC02 Data Sheet of devices. If you are using one of these devices please read the document located at 24AA02/24LC02B/24FC02 Data Sheet.

**Notification Status:** Final

**Description of Change:** 1) Corrected Part Marking for UDFN package. 2) . Added note about exposed pad on the TDFN and UDFN packages.

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Manufacturability

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 09 May 2019

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

**Attachment(s):**

24AA02/24LC02B/24FC02 Data Sheet

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

24AA02/SN
24AA02/P
24AA02/ST
24AA02-I/MS
24AA02H-I/MS
24AA02-I/SN
24AA02H-I/SN
24AA02-I/P
24AA02H-I/P
24AA02-I/ST
24AA02H-I/ST
24AA02T/SN
24AA02T-I/MNY
24AA02HT-I/MNY
24AA02T-I/MS
24AA02HT-I/MS
24AA02T-I/MC
24AA02T-I/LT
24AA02HT-I/LT
24AA02T-I/SN
24AA02HT-I/SN
24AA02T-I/ST
24AA02HT-I/ST
24AA02T-I/OT
24AA02HT-I/OT
24AA02/SNRVC
24AA02/PRVC
24AA02/STRVC
24AA02-I/SNRVC
24AA02-I/PRVC
24AA02-I/STRVC
24AA02T/SNRVC
24AA02T/STRVC
24AA02T-I/SNRVC
24AA02T-I/STRVC
24AA02T-I/SN15KV03
24AA02/SNB79
24AA02-E/WM16KB21
24AA02-I/S16K
24AA02SC-I/S16K
24AA02-I/WF0716K
24AA02-I/WF16K
24AA02SC-I/WF16K
24AA02-I/W0716K
24AA02-I/WNBG16K
24AA02-I/W16K

24AA02SC-I/W16K
24AA02-I/WMNBG16K
24AA02-I/MSB31
24AA02T-I/MSB31
24AA02T-I/OT103
24AA02T-I/OT16KVAO
24AA02E64-E/W16K
24AA02E48-E/SN
24AA02E64-E/SN
24AA02H-I/S0816K
24AA02H-I/S16K
24AA02E48-I/SN
24AA02E64-I/SN
24AA02UID-I/SN
24AA02UID-I/P
24AA02E48T-I/SN
24AA02E64T-I/SN
24AA02UIDT-I/SN
24AA02E48T-I/OT
24AA02E64T-I/OT
24AA02UIDT-I/OT
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24AA025-I/MC
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24AA025-I/SN
24AA024-I/P
24AA025-I/P
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24AA025-I/ST
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24AA025T-I/MS
24AA024T-I/MC
24AA025T-I/MC
24AA024T-I/SN
24AA025T-I/SN
24AA024T-I/ST
24AA025T-I/ST
24AA025T-I/OT

24AA025E48-E/SN
24AA025E64-E/SN
24AA024H-I/MS
24AA024H-I/SN
24AA025E48-I/SN
24AA025E64-I/SN
24AA025UID-I/SN
24AA024H-I/P
24AA025UID-I/P
24AA024H-I/ST
24AA024HT-I/MNY
24AA024HT-I/MS
24AA024HT-I/SN
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24AA025E64T-I/SN
24AA025UIDT-I/SN
24AA024HT-I/ST
24AA025E48T-I/OT
24AA025E64T-I/OT
24AA025UIDT-I/OT
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24AA025E64T-E/SN
24AA025E48T-E/OT
24AA025E64T-E/OT
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24LC02BH-E/MS
24LC02B-E/SN
24LC02BH-E/SN
24LC02B-E/P
24LC02BH-E/P
24LC02B-E/ST
24LC02BH-E/ST
24LC02B-I/MS
24LC02BH-I/MS
24LC02B-I/SN
24LC02BH-I/SN
24LC02B-I/P
24LC02BH-I/P
24LC02B-I/ST
24LC02BH-I/ST
24LC02BT/SN
24LC02BT/ST
24LC02BT-I/MNY
24LC02BHT-I/MNY
24LC02BT-I/MS
24LC02BHT-I/MS

24LC02BT-I/MC
24LC02BT-I/LT
24LC02BHT-I/LT
24LC02BT-I/SN
24LC02BHT-I/SN
24LC02BT-I/ST
24LC02BHT-I/ST
24LC02BT-I/OT
24LC02BHT-I/OT
24LC02BT-E/MNY
24LC02BHT-E/MNY
24LC02BT-E/MS
24LC02BHT-E/MS
24LC02BT-E/MC
24LC02BT-E/LT
24LC02BHT-E/LT
24LC02BT-E/SN
24LC02BHT-E/SN
24LC02BT-E/ST
24LC02BHT-E/ST
24LC02BT-E/OT
24LC02BHT-E/OT
24LC02B/SNRVC
24LC02B/PRVC
24LC02B/PROCRVC
24LC02B/STRVC
24LC02B-E/SNRVC
24LC02B-E/PRVC
24LC02B-E/STRVC
24LC02B-I/SNRVC
24LC02B-I/PRVC
24LC02B-I/STRVC
24LC02BT/SNRVC
24LC02BT/SNROCRVC
24LC02BT/STRVC
24LC02BT-I/SNRVC
24LC02BT-I/SNROCRVC
24LC02BT-I/SNVAO
24LC02BT-I/STRVC
24LC02BT-E/SNRVC
24LC02BT-E/STRVC
24LC02B/S15K
24LC02B-I/S15K
24LC02B-I/STA31
24LC02BT/SNA31
24LC02BT/SN15KVAO
24LC02BT-I/SN15KVAO
24LC02BT-I/STA31
24LC02BT-E/SN15KV01

24LC02BT-E/SN15KV04
24LC02B-E/SN16KVAO
24LC02B-I/WF0816K
24LC02B-I/WF16K6
24LC02B-I/SNA32
24LC02B-I/PREL
24LC02BT-I/MC16KVAO
24LC02BT-I/SN104
24LC02BT-I/SNA32
24LC02BT-I/SN16KV02
24LC02BT-I/SN16KVAO
24LC02BT-I/OT105
24LC02BT-I/OT16K106
24LC02BT-I/OT16K107
24LC02BT-I/OT16K108
24LC02BT-I/OTA31
24LC02BT-I/OT16KV04
24LC02BT-E/SN16K109
24LC02BT-E/SN16KV03
24LC02BT-E/SN16KV07
24LC02BT-E/SN16KVAO
24LC02BT-E/ST16KV05
24LC02BT-E/ST16KVAO
24LC02BT-E/OT16KV06
24LC02BT-E/OT16KVAO
24LC02BH-I/SN100
24FC02-E/MS
24FC02-E/SN
24FC02-E/P
24FC02-E/ST
24FC02-I/MS
24FC02-I/SN
24FC02-I/P
24FC02-I/ST
24FC02T-I/MS
24FC02T-I/SN
24FC02T-I/ST
24FC02T-I/OT
24FC02T-I/MUY
24FC02T-E/MS
24FC02T-E/SN
24FC02T-E/ST
24FC02T-E/OT
24FC02T-E/MUY

# 24AA02/24LC02B/24FC02

## 2K I²C Serial EEPROM

### Device Selection Table

| Part Number | Vcc Range | Max. Clock Frequency | Temp. Ranges | Available Packages |
|---|---|---|---|---|
| 24AA02 | 1.7V-5.5V | 400 kHz(1) | I | P, SN, MS, ST, MC, LT, MNY, OT |
| 24LC02B | 2.5V-5.5V | 400 kHz | I, E | P, SN, MS, ST, MC, LT, MNY, OT |
| 24FC02 | 1.7V-5.5V | 1 MHz | I, E | P, SN, MS, ST, MUY, OT |

**Note 1:** 100 kHz for VCC < 2.5V

### Features

- Single Supply with Operation down to 1.7V for 24AA02 and 24FC02 Devices, 2.5V for 24LC02B Devices
- Low-Power CMOS Technology:
  - Read current 1 mA, maximum
  - Standby current 1 µA, maximum (I-temp.)
- 2-Wire Serial Interface, I²C Compatible
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz, 400 kHz and 1 MHz Compatibility
- Page Write Time: 5 ms, Maximum
- Self-Timed Erase/Write Cycle
- 8-Byte Page Write Buffer
- Hardware Write-Protect
- ESD Protection >4,000V
- More than 1 Million Erase/Write Cycles
- Data Retention >200 Years
- Factory Programming Available
- RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- Automotive AEC-Q100 Qualified

### Packages

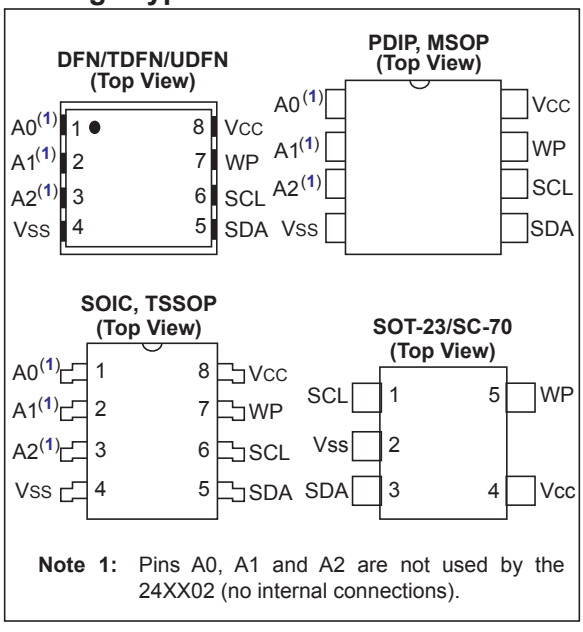
- 8-Lead DFN, 8-Lead MSOP, 8-Lead PDIP, 8-Lead SOIC, 8-Lead TDFN, 8-Lead TSSOP, 8-Lead UDFN, 5-Lead SOT-23 and 5-Lead SC-70

### Description

The Microchip Technology Inc. 24XX02(1) is a 2-Kbit Electrically Erasable PROM. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Its low-voltage design permits operation down to 1.7V with standby and active currents of only 1 µA and 1 mA, respectively. The 24XX02 also has a page write capability for up to 8 bytes of data.

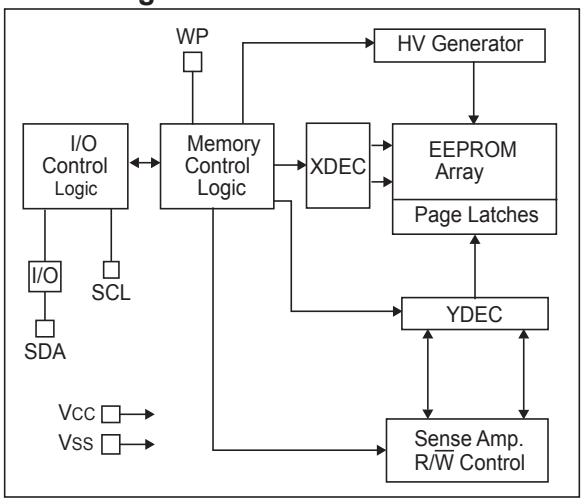
**Note 1:** 24XX02 is used in this document as a generic part number for the 24AA02/24LC02B/24FC02 devices.

### Package Types




**Note 1:** Pins A0, A1 and A2 are not used by the 24XX02 (no internal connections).

## Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.3V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied .....-40°C to +125°C

ESD protection on all pins ..... ≥4 kV

**† NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

| **DC CHARACTERISTICS** | | | Industrial (I): TA = -40°C to +85°C, VCC = +1.7V to +5.5V<br>Extended (E): TA = -40°C to +125°C, VCC = +2.5V to +5.5V (24LC02B)<br>Extended (E): TA = -40°C to +125°C, VCC = +1.7V to +5.5V (24FC02) | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| D1 | VIH | High-Level Input Voltage | 0.7 VCC | — | — | V | |
| D2 | VIL | Low-Level Input Voltage | — | — | 0.3 VCC | V | |
| D3 | VHYS | Hysteresis of Schmitt Trigger Inputs | 0.05 VCC | — | — | V | **Note** |
| D4 | VOL | Low-Level Output Voltage | — | — | 0.40 | V | IOL = 3.0 mA, VCC = 2.5V |
| D5 | ILI | Input Leakage Current | — | — | ±1 | µA | VIN = VSS or VCC |
| D6 | ILO | Output Leakage Current | — | — | ±1 | µA | VOUT = VSS or VCC |
| D7 | CIN, COUT | Pin Capacitance (all inputs/outputs) | — | — | 10 | pF | VCC = 5.0V (**Note**)<br>TA = 25°C, FCLK = 1 MHz |
| D8 | ICCWRITE | Operating Current | — | — | 3 | mA | VCC = 5.5V, SCL = 400 kHz |
| D9 | ICCREAD | | — | — | 1 | mA | VCC = 5.5V, SCL = 400 kHz |
| D10 | ICCS | Standby Current | — | — | 1 | µA | SDA = SCL = VCC<br>WP = VSS, I-Temp. |
| | | | — | — | 3 | µA | SDA = SCL = VCC<br>WP = VSS, E-Temp. (**24FC02**) |
| | | | — | — | 5 | µA | SDA = SCL = VCC<br>WP = VSS, E-Temp. (**24LC02B**) |

**Note:** This parameter is periodically sampled and not 100% tested.

**TABLE 1-2: AC CHARACTERISTICS**

| AC CHARACTERISTICS | | | Industrial (I): $T_A$ = -40°C to +85°C, $V_{CC}$ = +1.7V to +5.5V<br>Extended (E): $T_A$ = -40°C to +125°C, $V_{CC}$ = +2.5V to +5.5V (24LC02B)<br>Extended (E): $T_A$ = -40°C to +125°C, $V_{CC}$ = +1.7V to +5.5V (24FC02) | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| 1 | $F_{CLK}$ | Clock Frequency | — | — | 400 | kHz | 2.5V ≤ $V_{CC}$ ≤ 5.5V |
| | | | — | — | 100 | kHz | 1.7V ≤ $V_{CC}$ < 2.5V (**24AA02**) |
| | | | — | — | 1000 | kHz | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) |
| 2 | $T_{HIGH}$ | Clock High Time | 600 | — | — | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V |
| | | | 4000 | — | — | ns | 1.7V ≤ $V_{CC}$ < 2.5V (**24AA02**) |
| | | | 260 | — | — | ns | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) |
| 3 | $T_{LOW}$ | Clock Low Time | 1300 | — | — | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V |
| | | | 4700 | — | — | ns | 1.7V ≤ $V_{CC}$ < 2.5V (**24AA02**) |
| | | | 500 | — | — | ns | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) |
| 4 | $T_R$ | SDA and SCL Rise Time | — | — | 300 | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V (**Note 1**) |
| | | | — | — | 1000 | ns | 1.7V ≤ $V_{CC}$ < 2.5V (**24AA02**) (**Note 1**) |
| | | | — | — | 1000 | ns | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) (**Note 1**) |
| 5 | $T_F$ | SDA and SCL Fall Time | — | — | 300 | ns | **Note 1** |
| 6 | $T_{HD:STA}$ | Start Condition Hold Time | 600 | — | — | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V |
| | | | 4000 | — | — | ns | 1.7V ≤ $V_{CC}$ < 2.5V (**24AA02**) |
| | | | 250 | — | — | ns | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) |
| 7 | $T_{SU:STA}$ | Start Condition Setup Time | 600 | — | — | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V |
| | | | 4700 | — | — | ns | 1.7V ≤ $V_{CC}$ < 2.5V (**24AA02**) |
| | | | 250 | — | — | ns | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) |
| 8 | $T_{HD:DAT}$ | Data Input Hold Time | 0 | — | — | ns | **Note 2** |
| 9 | $T_{SU:DAT}$ | Data Input Setup Time | 100 | — | — | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V |
| | | | 250 | — | — | ns | 1.7V ≤ $V_{CC}$ < 2.5V (**24AA02**) |
| | | | 50 | — | — | ns | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) |
| 10 | $T_{SU:STO}$ | Stop Condition Setup Time | 600 | — | — | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V |
| | | | 4000 | — | — | ns | 1.7V ≤ $V_{CC}$ < 2.5V (**24AA02**) |
| | | | 250 | — | — | ns | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) |
| 11 | $T_{SU:WP}$ | WP Setup Time | 0 | — | — | ns | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) |
| 12 | $T_{HD:WP}$ | WP Hold Time | 1000 | — | — | ns | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) |
| 13 | $T_{AA}$ | Output Valid from Clock | — | — | 900 | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V (**Note 2**) |
| | | | — | — | 3500 | ns | 1.7V ≤ $V_{CC}$ < 2.5V (**24AA02**) (**Note 2**) |
| | | | — | — | 450 | ns | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) (**Note 2**) |

**Note 1:** Characterized but not 100% tested.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**3:** $C_B$ = total capacitance of one bus line in pF.

**4:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's website at www.microchip.com.

**TABLE 1-2: AC CHARACTERISTICS**

| AC CHARACTERISTICS (Continued) | | | Industrial (I): $T_A$ = -40°C to +85°C, $V_{CC}$ = +1.7V to +5.5V<br>Extended (E): $T_A$ = -40°C to +125°C, $V_{CC}$ = +2.5V to +5.5V (24LC02B)<br>Extended (E): $T_A$ = -40°C to +125°C, $V_{CC}$ = +1.7V to +5.5V (24FC02) | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| 14 | $T_{BUF}$ | Bus Free Time: The time the bus must be free before a new transmission can start | 1300 | — | — | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V |
| | | | 4700 | — | — | ns | 1.7V ≤ $V_{CC}$ < 2.5V (**24AA02**) |
| | | | 500 | — | — | ns | 1.7V ≤ $V_{CC}$ ≤ 5.5V (**24FC02**) |
| 15 | $T_{OF}$ | Output Fall Time from $V_{IH}$ Minimum to $V_{IL}$ Maximum | 20+0.1$C_B$ | — | 250 | ns | 2.5V ≤ $V_{CC}$ ≤ 5.5V (**24LC02B**) (**Notes 1** and **3**) |
| | | | — | — | 250 | ns | 1.7V ≤ $V_{CC}$ < 2.5V (**24AA02**) (**Note 1**) |
| 16 | $T_{SP}$ | Input Filter Spike Suppression (SDA and SCL pins) | — | — | 50 | ns | **Note 1** |
| 17 | $T_{WC}$ | Write Cycle Time (byte or page) | — | — | 5 | ms | |
| 18 | | Endurance | 1,000,000 | — | — | cycles | 25°C, 5.5V, Page Mode (**Note 4**) |

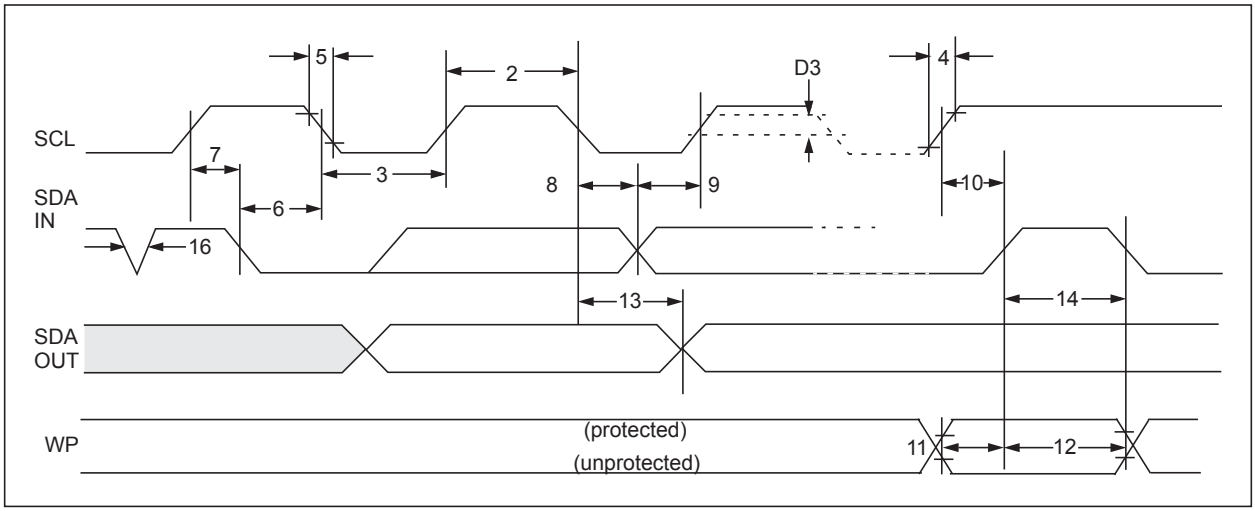
**Note 1:** Characterized but not 100% tested.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**3:** $C_B$ = total capacitance of one bus line in pF.

**4:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's website at www.microchip.com.

**FIGURE 1-1: BUS TIMING DATA**



## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Name | DFN | MSOP | PDIP | SC-70 | SOIC | SOT-23 | TDFN(1) | TSSOP | UDFN(1) | Description |
|---|---|---|---|---|---|---|---|---|---|---|
| A0 | 1 | 1 | 1 | — | 1 | — | 1 | 1 | 1 | Not Connected |
| A1 | 2 | 2 | 2 | — | 2 | — | 2 | 2 | 2 | Not Connected |
| A2 | 3 | 3 | 3 | — | 3 | — | 3 | 3 | 3 | Not Connected |
| VSS | 4 | 4 | 4 | 2 | 4 | 2 | 4 | 4 | 4 | Ground |
| SDA | 5 | 5 | 5 | 3 | 5 | 3 | 5 | 5 | 5 | Serial Address/Data I/O |
| SCL | 6 | 6 | 6 | 1 | 6 | 1 | 6 | 6 | 6 | Serial Clock |
| WP | 7 | 7 | 7 | 5 | 7 | 5 | 7 | 7 | 7 | Write-Protect Input |
| VCC | 8 | 8 | 8 | 4 | 8 | 4 | 8 | 8 | 8 | Power Supply |

**Note 1:** The exposed pad on the TDFN/UDFN package can be connected to VSS or left floating.

### 2.1 A0, A1, A2

The A0, A1 and A2 pins are not used by the 24XX02. They may be left floating or tied to either VSS or VCC.

### 2.2 Serial Address/Data Input/Output (SDA)

The SDA input is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating Start and Stop conditions.

### 2.3 Serial Clock (SCL)

The SCL input is used to synchronize the data transfer to and from the device.

### 2.4 Write-Protect (WP)

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory 00-FF).

If tied to VCC, write operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

## 3.0 FUNCTIONAL DESCRIPTION

The 24XX02 supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while defining a device receiving data as a receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX02 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

## 4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

### 4.1 Bus Not Busy (A)

Both data and clock lines remain high.

### 4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

### 4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

### 4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between the Start and Stop conditions is determined by the master device and is, theoretically, unlimited (although only the last eight will be stored when doing a write operation). When an overwrite does occur, it will replace data based on the first-in first-out (FIFO) principle.

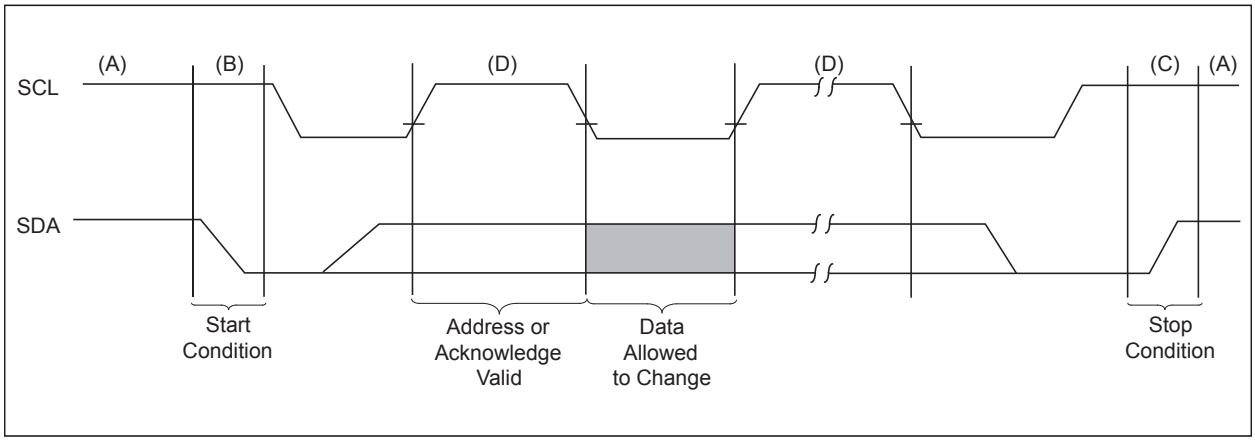
### 4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

| **Note:** | The 24XX02 does not generate any Acknowledge bits if an internal programming cycle is in progress. |
|---|---|

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX02) will leave the data line high to enable the master to generate the Stop condition.

**FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS**



## 5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the master device. The control byte consists of a four-bit control code. For the 24XX02, this is set as '1010' binary for read and write operations. The next three bits of the control byte are "don't cares" for the 24XX02. The combination of the 4-bit control code and the next three bits are called the slave address.

The last bit of the control byte is the Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit and it defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. Following the Start condition, the 24XX02 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving a valid slave address and the R/$\overline{\text{W}}$ bit, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{\text{W}}$ bit, the 24XX02 will select a read or write operation.

The next byte received defines the address of the first data byte within the selected block (Figure 5-2). The word address byte uses all eight bits.

| Operation | Control Code | Block Select | R/$\overline{\text{W}}$ |
|---|---|---|---|
| Read | 1010 | Block Address | 1 |
| Write | 1010 | Block Address | 0 |

**FIGURE 5-1: CONTROL BYTE ALLOCATION**

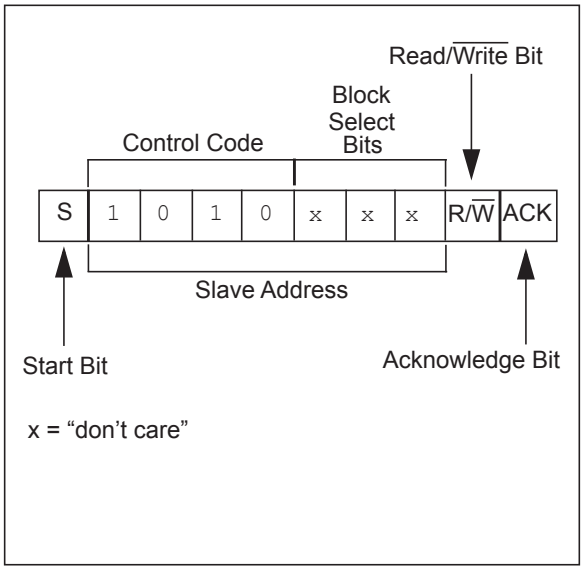
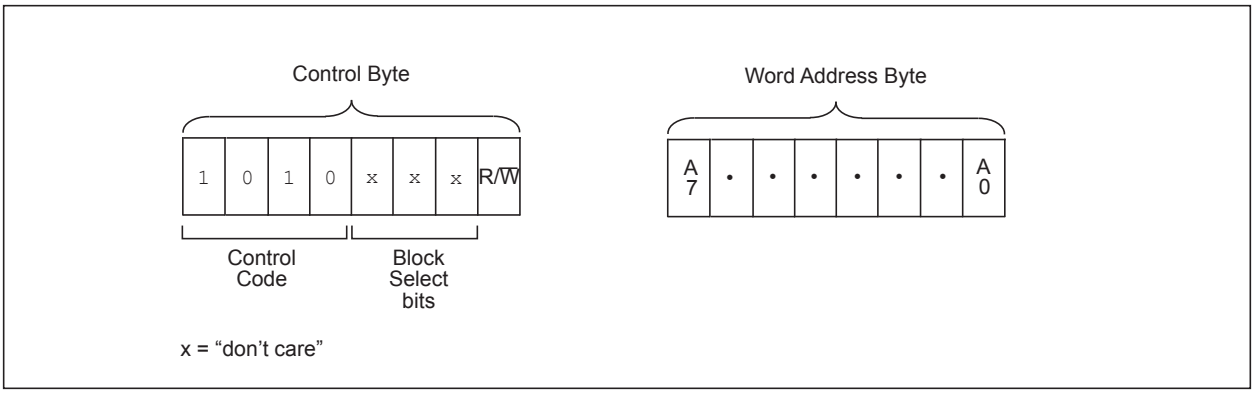



**FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS**



## 6.0 WRITE OPERATION

### 6.1 Byte Write

Following the Start condition from the master, the device code (4 bits), the block address (3 bits, “don’t cares”) and the R/$\overline{W}$ bit, which is a logic-low, is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the Address Pointer of the 24XX02. After receiving another Acknowledge signal from the 24XX02, the master device will transmit the data word to be written into the addressed memory location. The 24XX02 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and, during this time, the 24XX02 will not generate Acknowledge signals (Figure 6-1).

### 6.2 Page Write

The write control byte, word address and first data byte are transmitted to the 24XX02 in the same way as in a byte write. However, instead of generating a Stop condition, the master transmits up to eight data bytes to the 24XX02, which are temporarily stored in the on-chip page buffer and will be written into the memory once the master has transmitted a Stop condition. Upon receipt of each word, the three lower-order Address Pointer bits, which form the byte counter, are internally incremented by one. The higher-order five bits of the word address remain constant. If the master should transmit more than eight words prior to generating the Stop condition, the Address Pointer will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2).

| | |
|---|---|
| **Note:** | Page write operations are limited to writing bytes within a single physical page **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘page size’) and end at addresses that are integer multiples of page size – 1. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary. |

### 6.3 Write Protection

The WP pin allows the user to write-protect the entire array (00-FF) when the pin is tied to VCC. If tied to VSS, the write protection is disabled.

**FIGURE 6-1: BYTE WRITE**

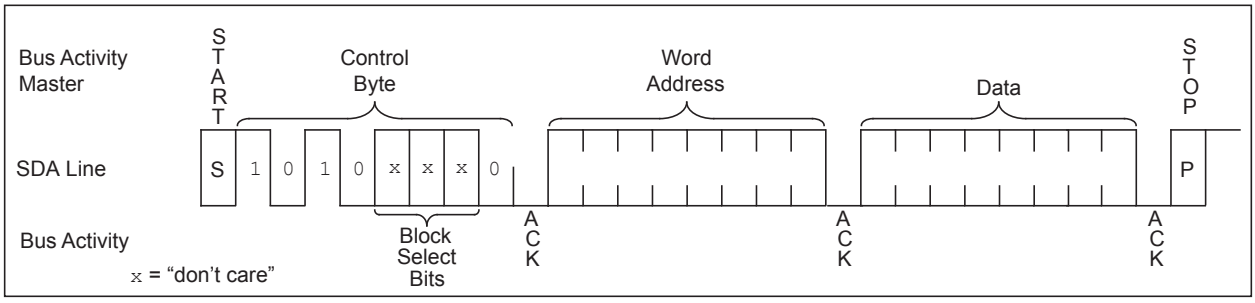
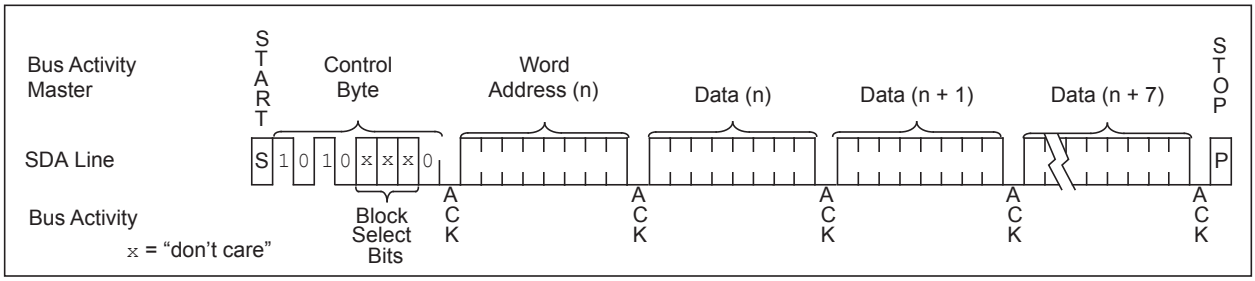


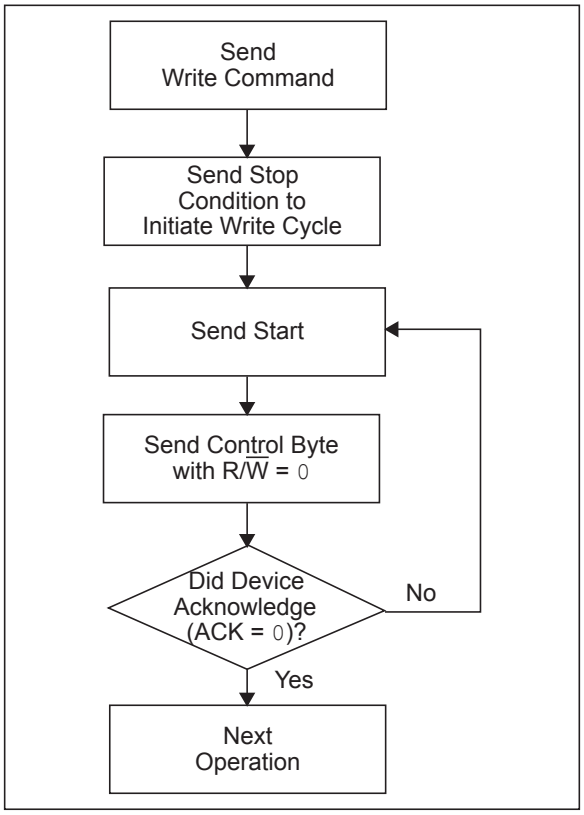
**FIGURE 6-2: PAGE WRITE**



## 7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write command has been issued from the master, the device initiates the internally-timed write cycle. ACK polling can then be initiated immediately. This involves the master sending a Start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, no ACK will be returned. If the cycle is complete, the device will return the ACK and the master can then proceed with the next read or write operation. See Figure 7-1 for a flow diagram of this operation.

**FIGURE 7-1: ACKNOWLEDGE POLLING FLOW**



## 8.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

### 8.1 Current Address Read

The 24XX02 contains an Address Pointer that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to '1', the 24XX02 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24XX02 discontinues transmission (Figure 8-1).

### 8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24XX02 as part of a write operation. Once the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a '1'. The 24XX02 will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24XX02 discontinues transmission (Figure 8-2).

### 8.3 Sequential Read

Sequential reads are initiated in the same way as a random read, except that once the 24XX02 transmits the first data byte, the master issues an acknowledge (as opposed to a Stop condition in a random read). This directs the 24XX02 to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24XX02 contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation.

### 8.4 Noise Protection

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

**FIGURE 8-1: CURRENT ADDRESS READ**

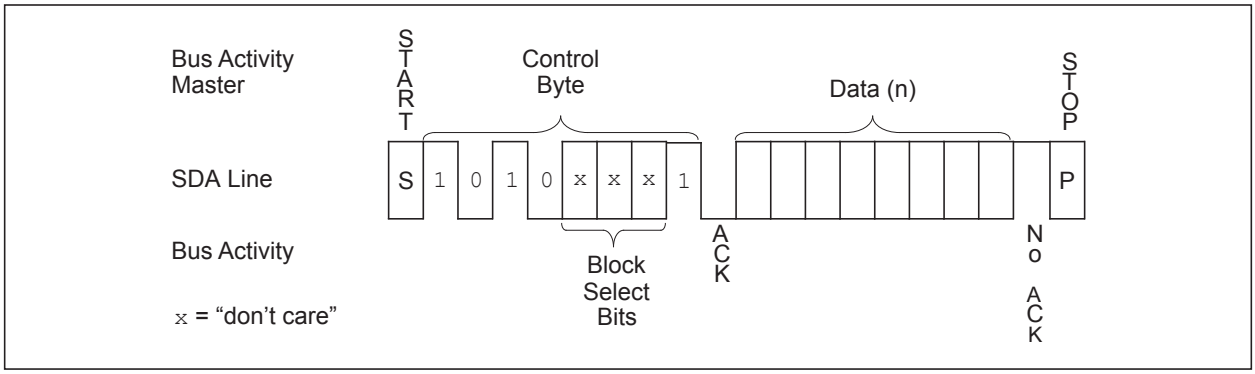


**FIGURE 8-2: RANDOM READ**

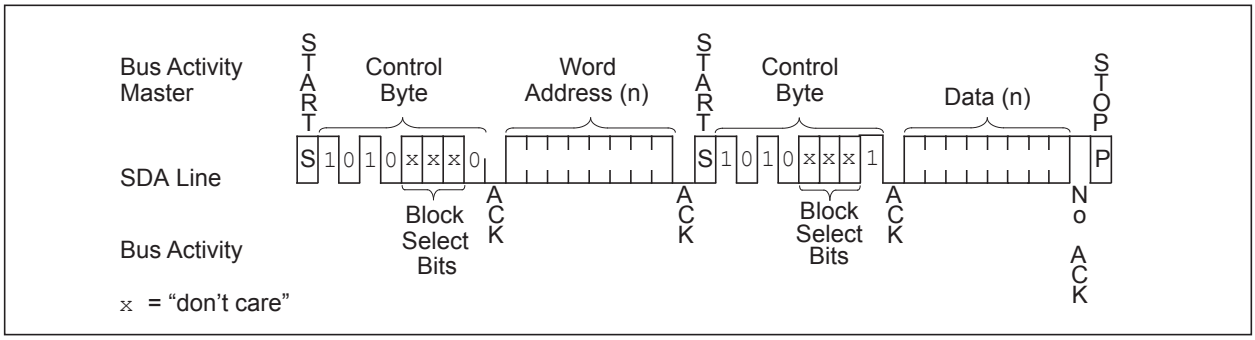
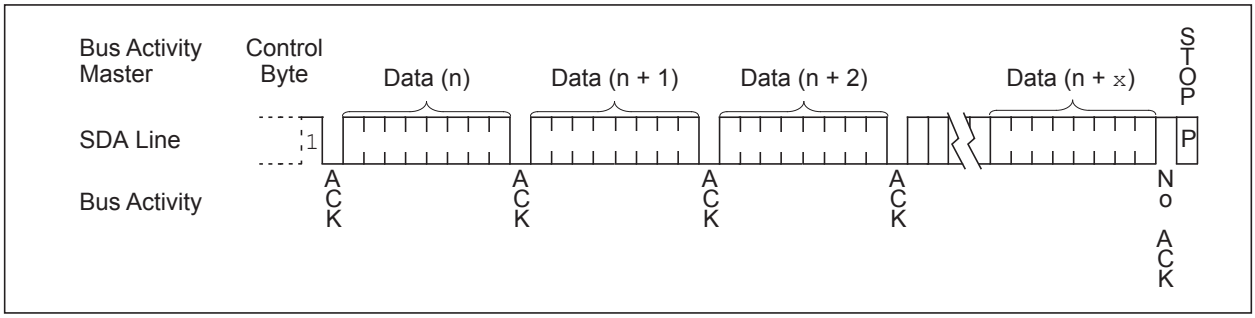



**FIGURE 8-3: SEQUENTIAL READ**

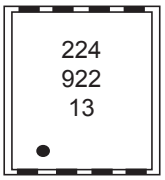


## 9.0 PACKAGING INFORMATION

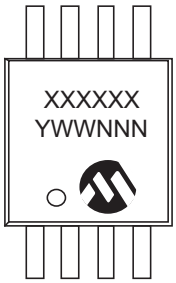
### 9.1 Package Marking Information*

8-Lead 2x3 DFN


Example

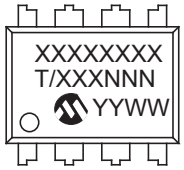



8-Lead MSOP

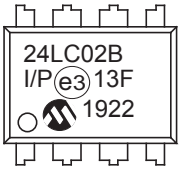



Example

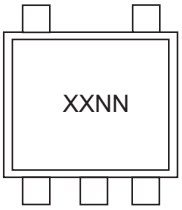

8-Lead PDIP (300 mil)



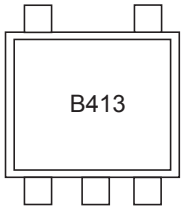

Example



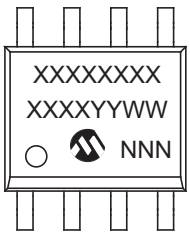

5-Lead SC-70



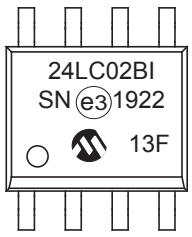

Example



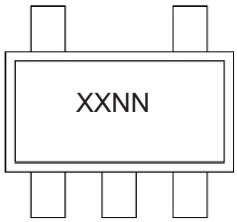

8-Lead SOIC (3.90 mm)



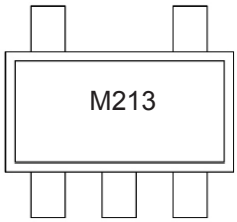

Example



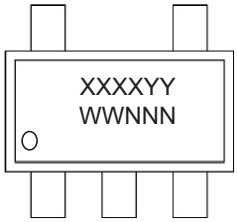
5-Lead SOT-23 (**1-Line Marking**)



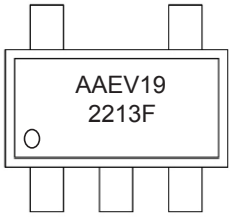

Example




5-Lead SOT-23 (**2-Line Marking**)

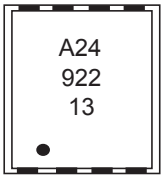



Example

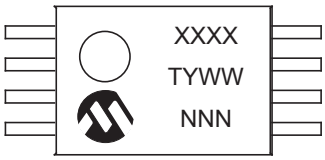



8-Lead 2x3 TDFN

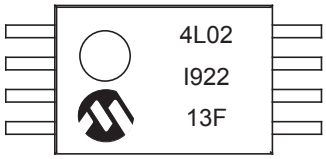

Example



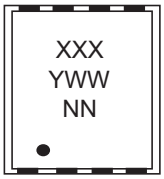

8-Lead TSSOP



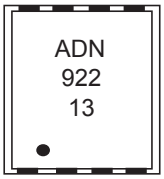

Example




8-Lead 2x3 UDFN




Example



| Part Number | 1st Line Marking Codes | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TSSOP | MSOP | UDFN | SOT-23 | | DFN | | TDFN | | SC-70 | |
| | | | | I-Temp. | E-Temp. | I-Temp. | E-Temp. | I-Temp. | E-Temp. | I-Temp. | E-Temp. |
| 24AA02 | 4A02 | 4A02T(1) | — | B2NN(2,3) | — | 221 | — | A21 | — | B5NN(2) | — |
| 24LC02B | 4L02 | 4L2BT(1) | — | M2NN(2,3) | N2NN(2,3) | 224 | 225 | A24 | A25 | B4NN(2) | B6NN(2) |
| 24FC02 | AADQ | 24FC02 | ADN | AAEVYY(4) | AAEVYY(4) | — | — | — | — | — | — |

**Note 1:** T = Temperature grade (I, E)

**2:** NN = Alphanumeric traceability code

**3:** These parts use the 1-line SOT-23 marking format

**4:** These parts use the 2-line SOT-23 marking format

| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | JEDEC® designator for Matte Tin (Sn) |

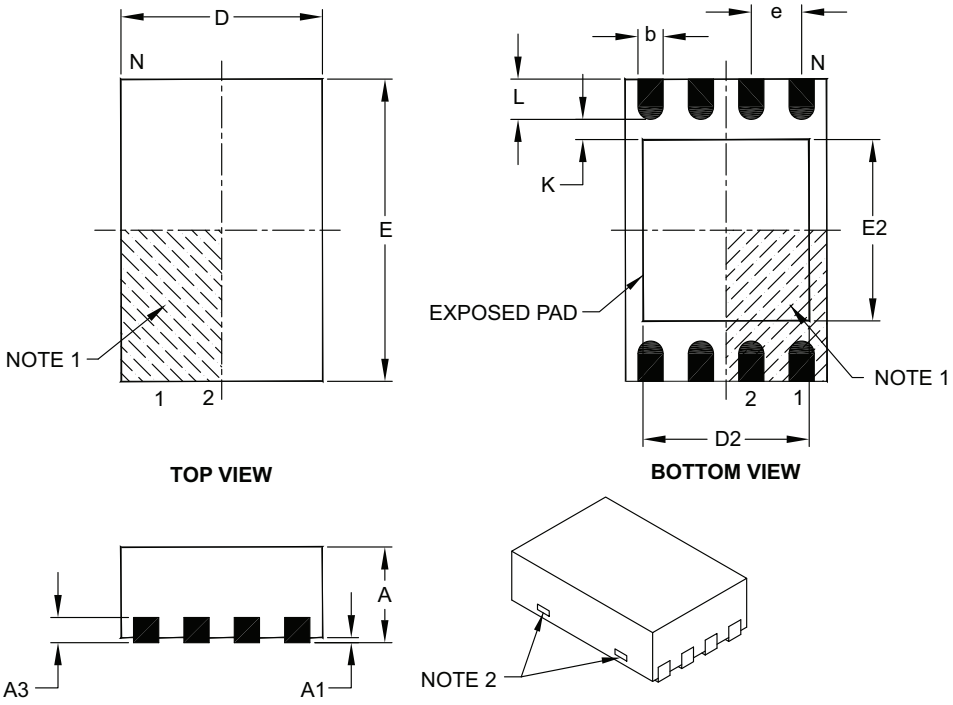
***** Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

**Note:** For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

### 8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.30 | – | 1.55 |
| Exposed Pad Width | E2 | 1.50 | – | 1.75 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

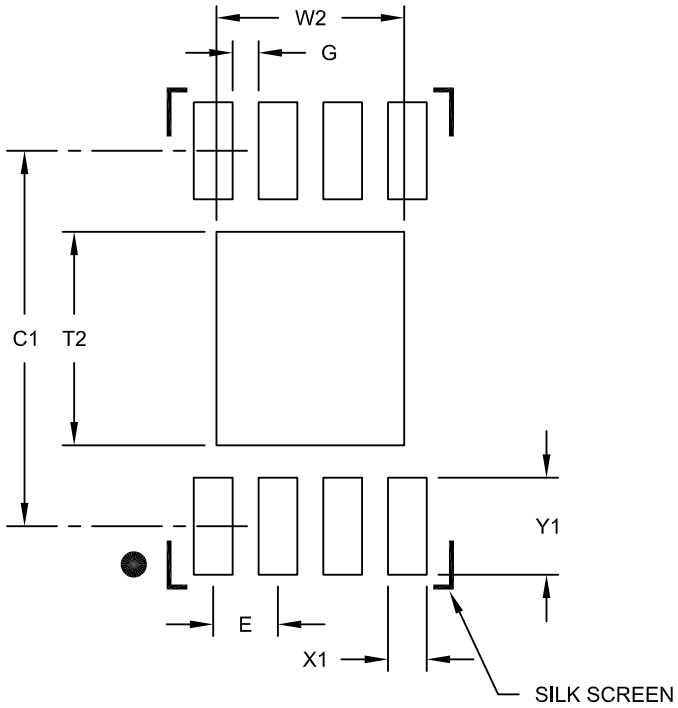
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Optional Center Pad Width | W2 | | | 1.45 |
| Optional Center Pad Length | T2 | | | 1.75 |
| Contact Pad Spacing | C1 | | 2.90 | |
| Contact Pad Width (X8) | X1 | | | 0.30 |
| Contact Pad Length (X8) | Y1 | | | 0.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

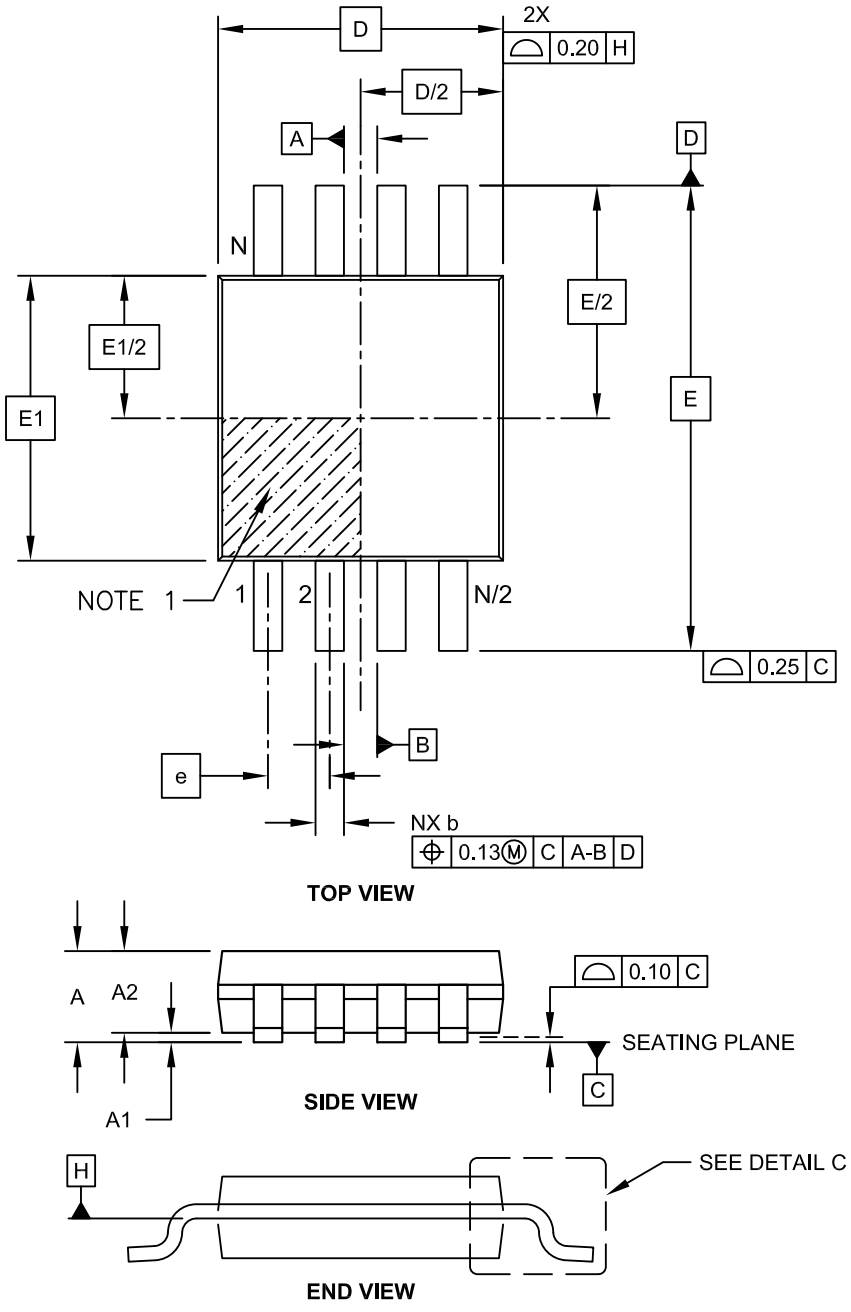
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123B

### 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

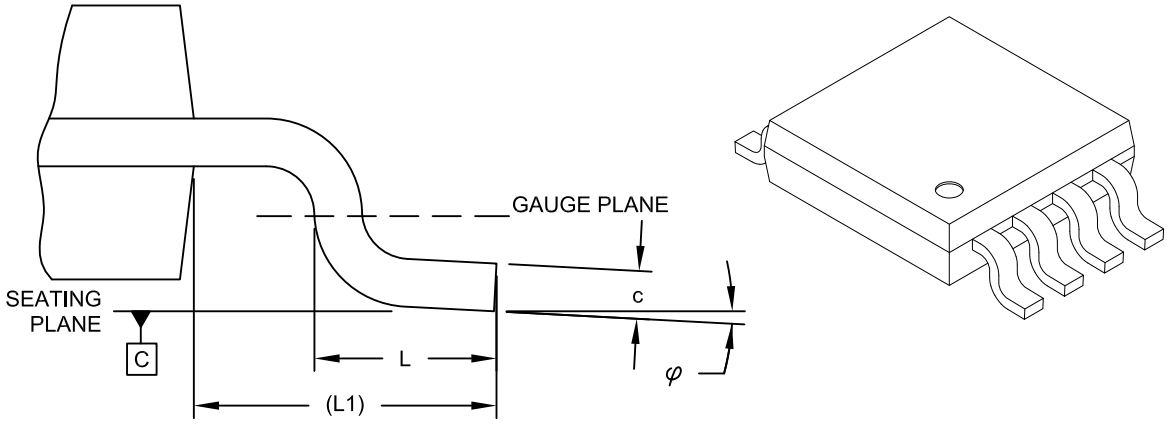
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-111C Sheet 1 of 2

## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**DETAIL C**

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | - | - | 1.10 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | 0.00 | - | 0.15 |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Overall Length | D | | 3.00 BSC | |
| Foot Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.08 | - | 0.23 |
| Lead Width | b | 0.22 | - | 0.40 |

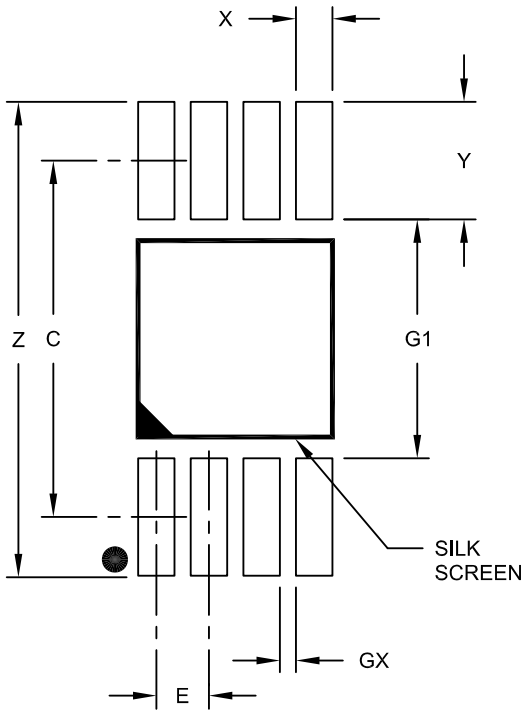
**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Contact Pad Spacing | C | | 4.40 | |
| Overall Width | Z | | | 5.85 |
| Contact Pad Width (X8) | X1 | | | 0.45 |
| Contact Pad Length (X8) | Y1 | | | 1.45 |
| Distance Between Pads | G1 | 2.95 | | |
| Distance Between Pads | GX | 0.20 | | |

Notes:

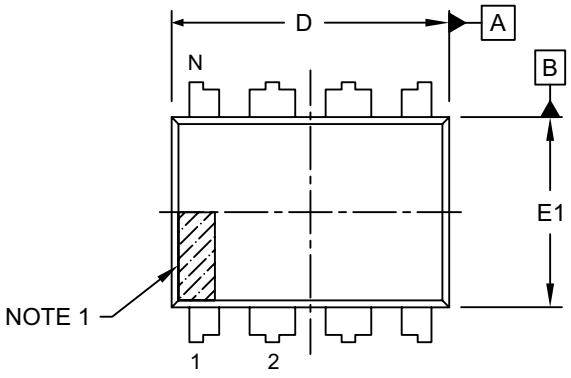
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

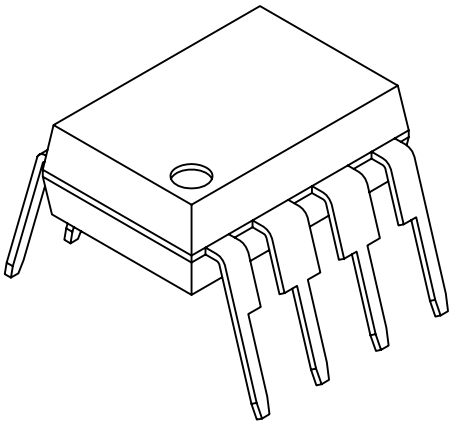
Microchip Technology Drawing No. C04-2111A

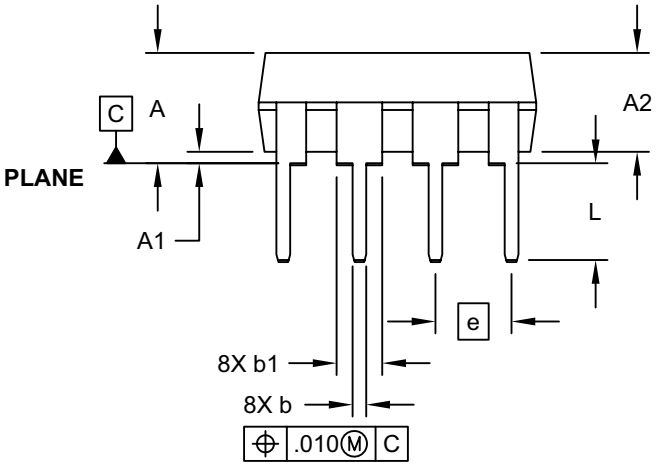
### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

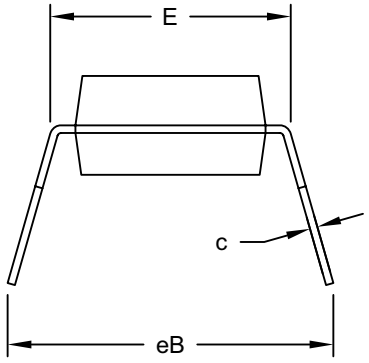



TOP VIEW






SIDE VIEW

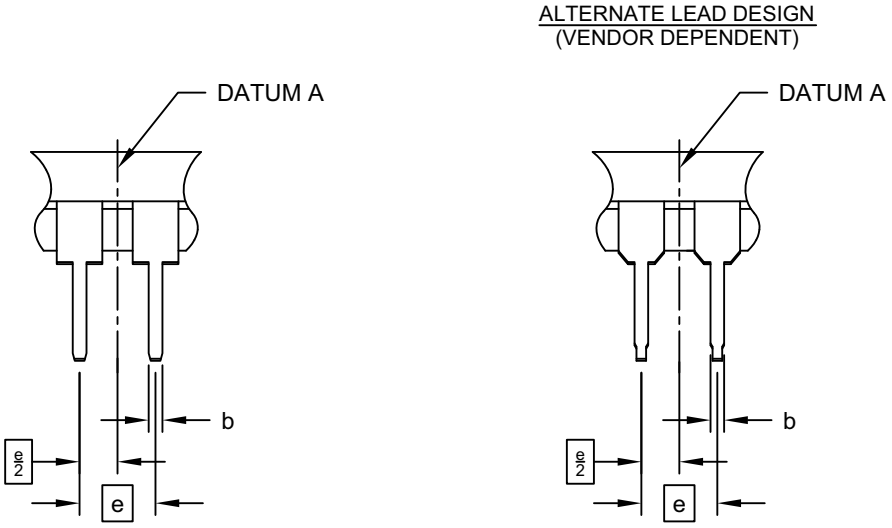



END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

## 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | - | - | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | - | - |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | - | - | .430 |

Notes:

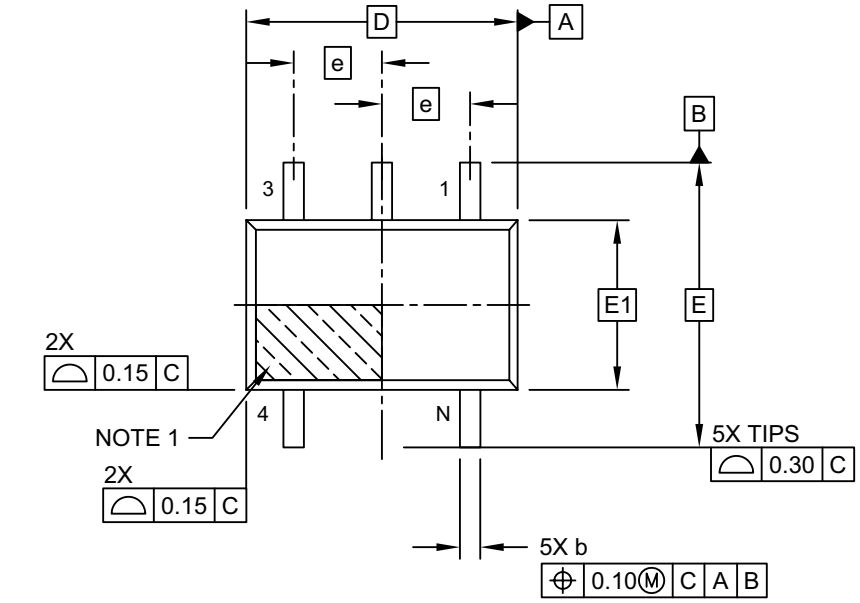
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

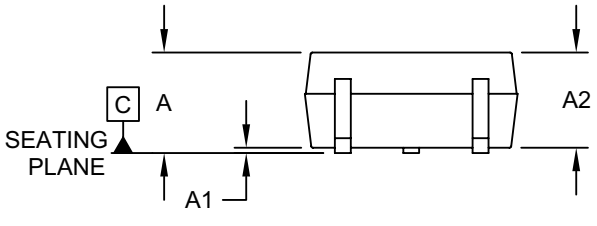
Microchip Technology Drawing No. C04-018D Sheet 2 of 2

### 5-Lead Plastic Small Outline Transistor (LT) [SC70]

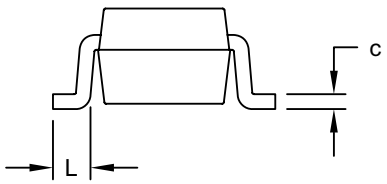
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

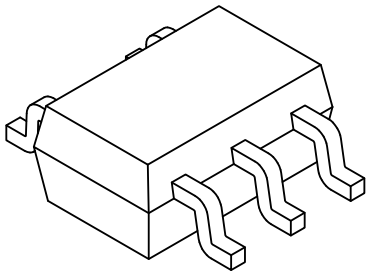



END VIEW

Microchip Technology Drawing C04-061D Sheet 1 of 2

## 5-Lead Plastic Small Outline Transistor (LT) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 5 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | - | 1.10 |
| Standoff | A1 | 0.00 | - | 0.10 |
| Molded Package Thickness | A2 | 0.80 | - | 1.00 |
| Overall Length | D | | 2.00 BSC | |
| Exposed Pad Length | D2 | 2.50 | 2.60 | 2.70 |
| Overall Width | E | | 2.10 BSC | |
| Exposed Pad Width | E1 | | 1.25 BSC | |
| Terminal Width | b | 0.15 | - | 0.40 |
| Terminal Length | L | 0.10 | 0.20 | 0.46 |
| Lead Thickness | c | 0.08 | - | 0.26 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

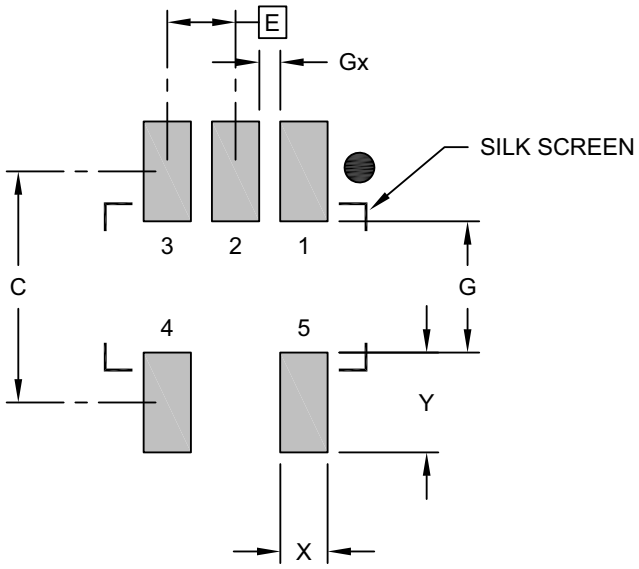
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061D Sheet 2 of 2

## 5-Lead Plastic Small Outline Transistor (LT) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 2.20 | |
| Contact Pad Width | X | | | 0.45 |
| Contact Pad Length | Y | | | 0.95 |
| Distance Between Pads | G | 1.25 | | |
| Distance Between Pads | Gx | 0.20 | | |

Notes:

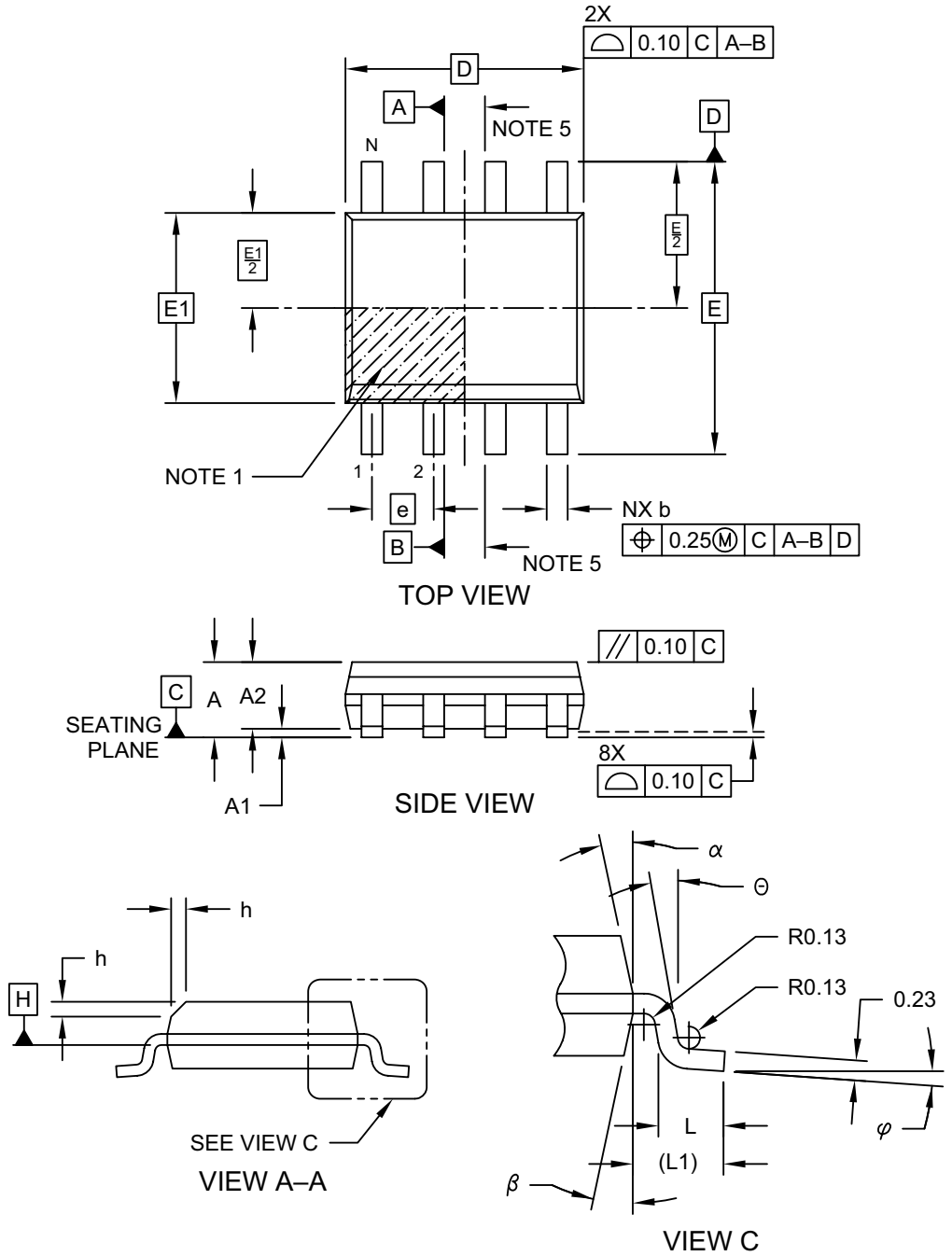
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061B

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

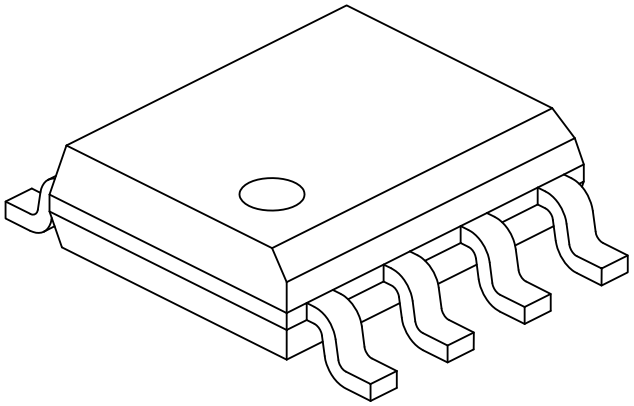
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | $\varphi$ | 0° | - | 8° |
| Lead Thickness | c | 0.17 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | $\alpha$ | 5° | - | 15° |
| Mold Draft Angle Bottom | $\beta$ | 5° | - | 15° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

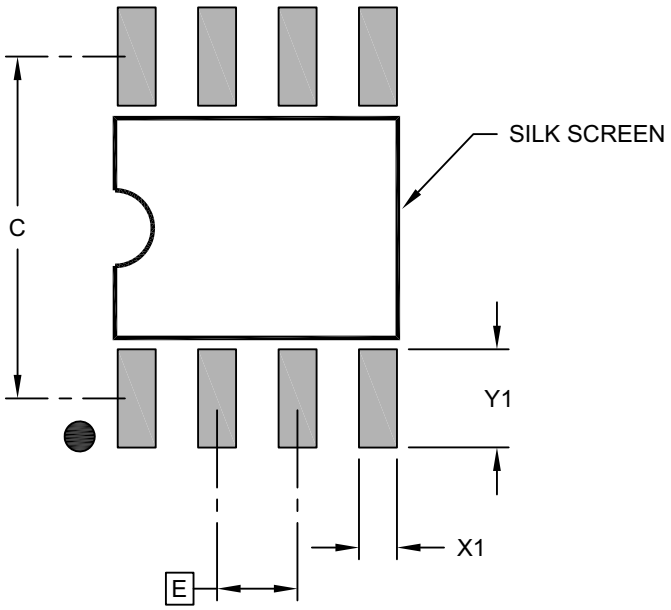
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

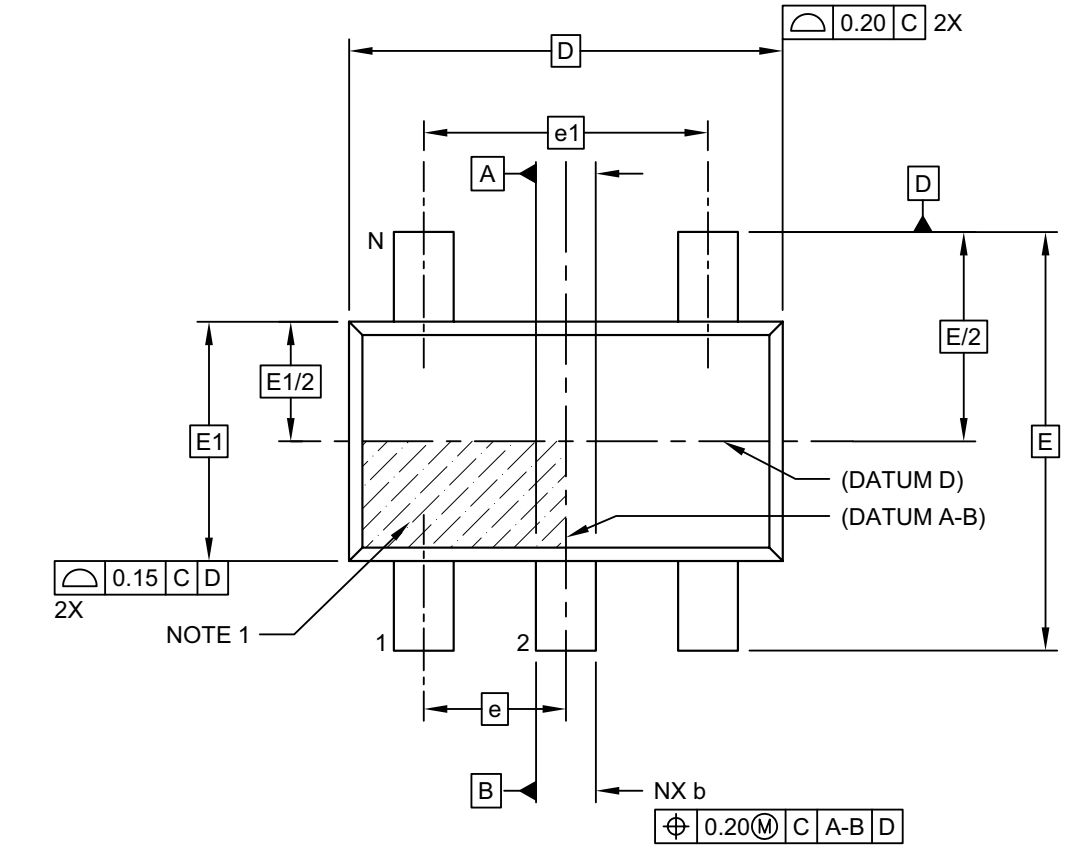
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

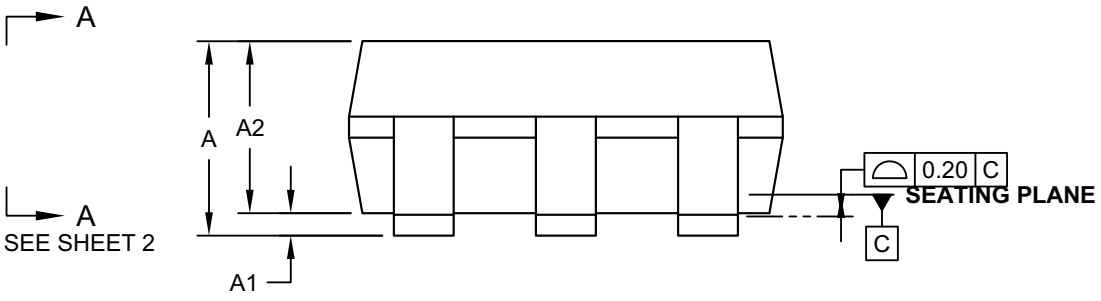
Microchip Technology Drawing C04-2057-SN Rev B

### 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW

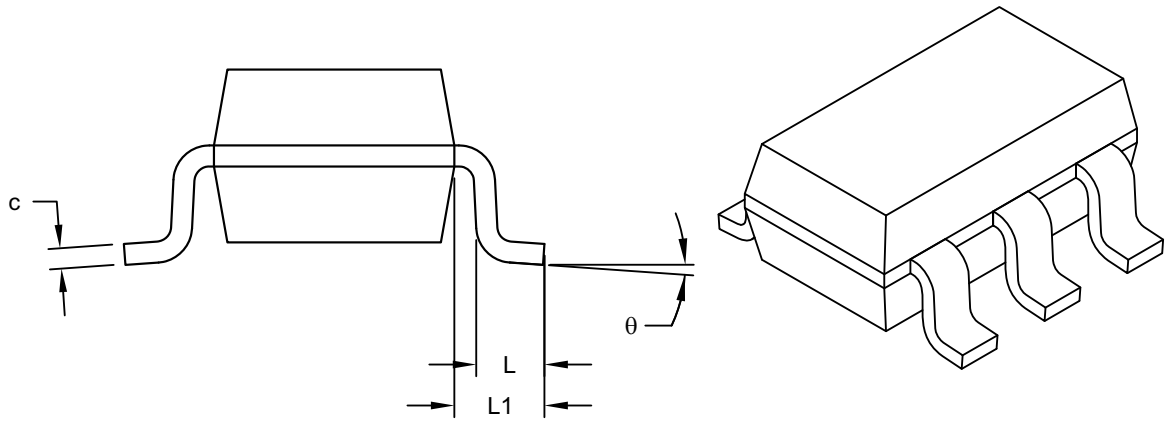



SIDE VIEW

Microchip Technology Drawing C04-028D [OT] Sheet 1 of 2

## 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




VIEW A-A
SHEET 1

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 6 | |
| Pitch | e | | 0.95 BSC | |
| Outside lead pitch | e1 | | 1.90 BSC | |
| Overall Height | A | 0.90 | - | 1.45 |
| Molded Package Thickness | A2 | 0.89 | - | 1.30 |
| Standoff | A1 | - | - | 0.15 |
| Overall Width | E | | 2.80 BSC | |
| Molded Package Width | E1 | | 1.60 BSC | |
| Overall Length | D | | 2.90 BSC | |
| Foot Length | L | 0.30 | - | 0.60 |
| Footprint | L1 | | 0.60 REF | |
| Foot Angle | ϕ | 0° | - | 10° |
| Lead Thickness | c | 0.08 | - | 0.26 |
| Lead Width | b | 0.20 | - | 0.51 |

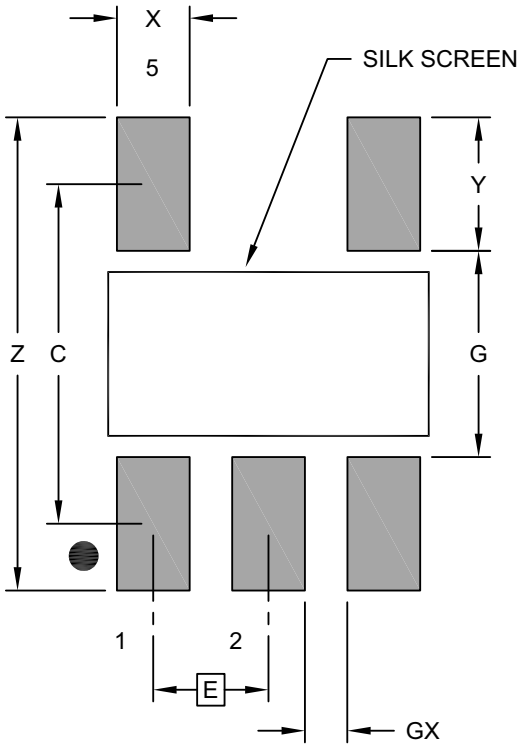
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091D [OT] Sheet 2 of 2

### 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.95 BSC | |
| Contact Pad Spacing | C | | 2.80 | |
| Contact Pad Width (X5) | X | | | 0.60 |
| Contact Pad Length (X5) | Y | | | 1.10 |
| Distance Between Pads | G | 1.70 | | |
| Distance Between Pads | GX | 0.35 | | |
| Overall Width | Z | | | 3.90 |

Notes:

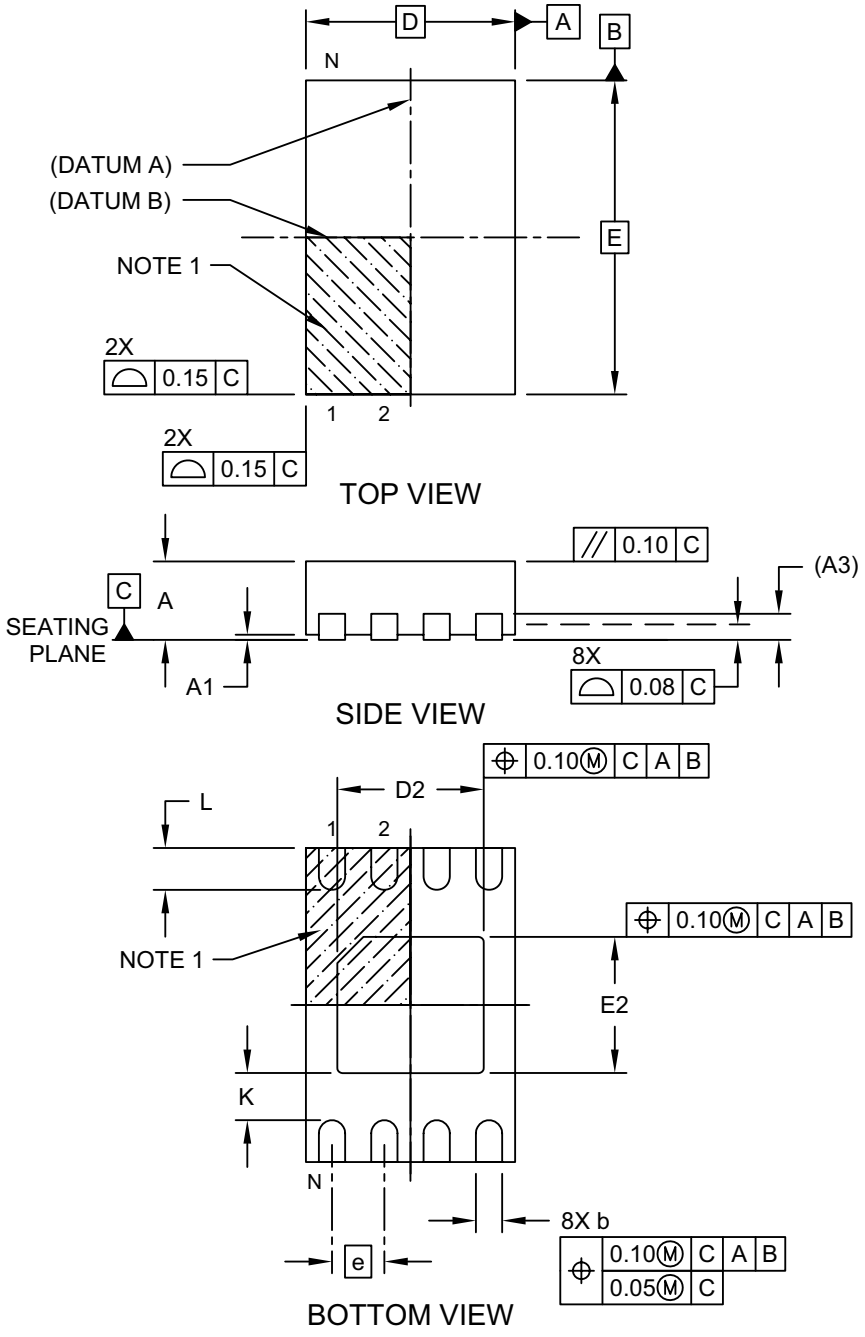
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A [OT]

**8-Lead Plastic Dual Flat, No Lead Package (MNY) – 2x3x0.8 mm Body [TDFN]**
**With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)**

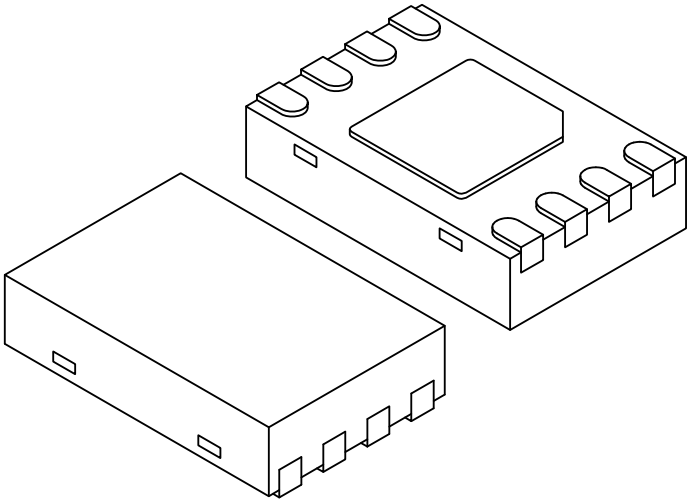
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing No. C04-129-MNY Rev E Sheet 1 of 2

### 8-Lead Plastic Dual Flat, No Lead Package (MNY) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.70 | 0.75 | 0.80 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.35 | 1.40 | 1.45 |
| Exposed Pad Width | E2 | 1.25 | 1.30 | 1.35 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.25 | 0.30 | 0.45 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

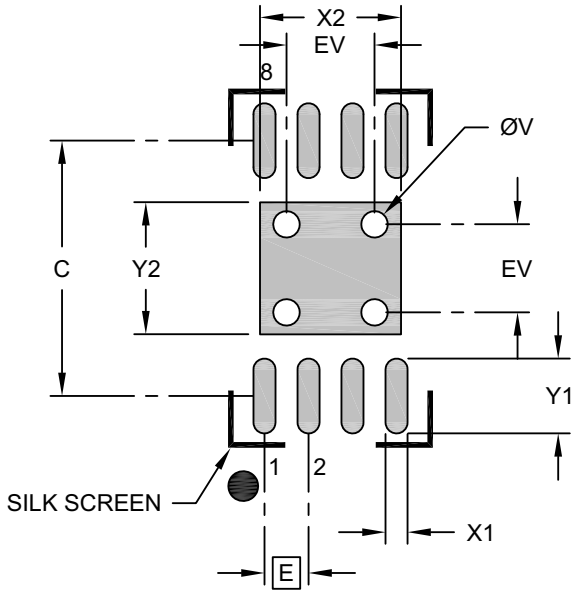
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MNY Rev E Sheet 2 of 2

### 8-Lead Plastic Dual Flat, No Lead Package (MNY) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 1.60 |
| Optional Center Pad Length | Y2 | | | 1.50 |
| Contact Pad Spacing | C | | 2.90 | |
| Contact Pad Width (X8) | X1 | | | 0.25 |
| Contact Pad Length (X8) | Y1 | | | 0.85 |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

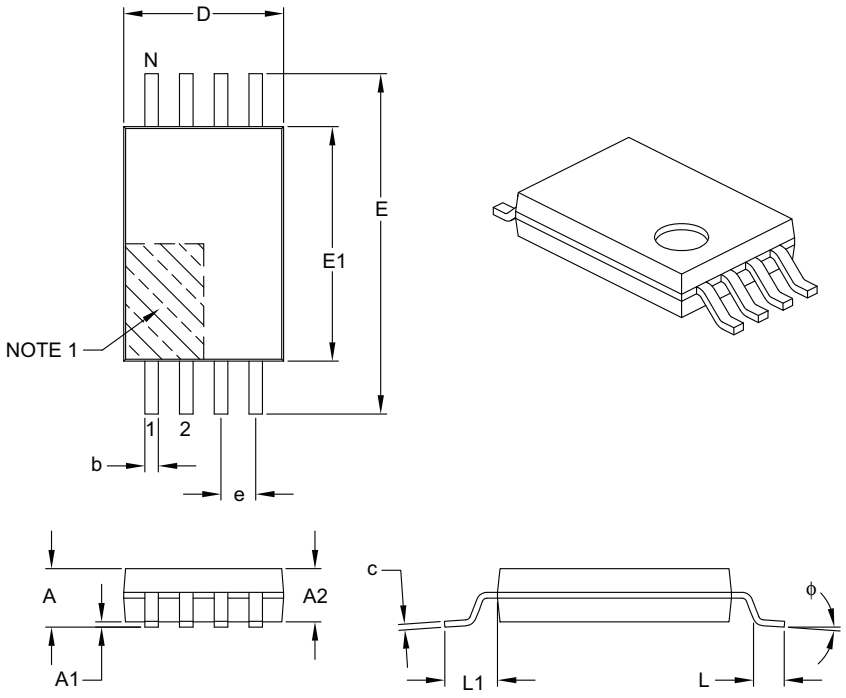
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MNY Rev. B

### 8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Overall Width | E | | 6.40 BSC | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | 2.90 | 3.00 | 3.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.19 | – | 0.30 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

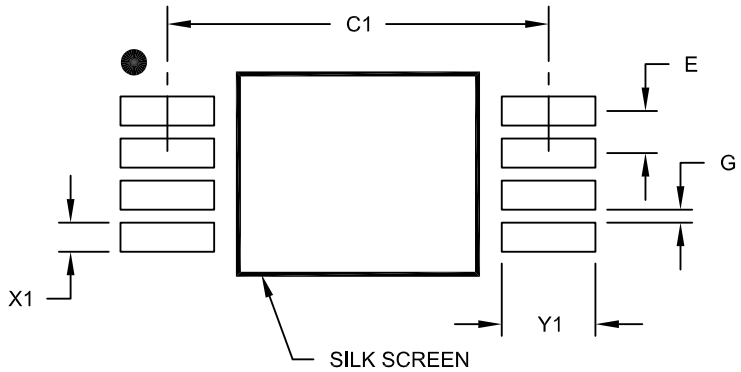
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C1 | | 5.90 | |
| Contact Pad Width (X8) | X1 | | | 0.45 |
| Contact Pad Length (X8) | Y1 | | | 1.45 |
| Distance Between Pads | G | 0.20 | | |

Notes:

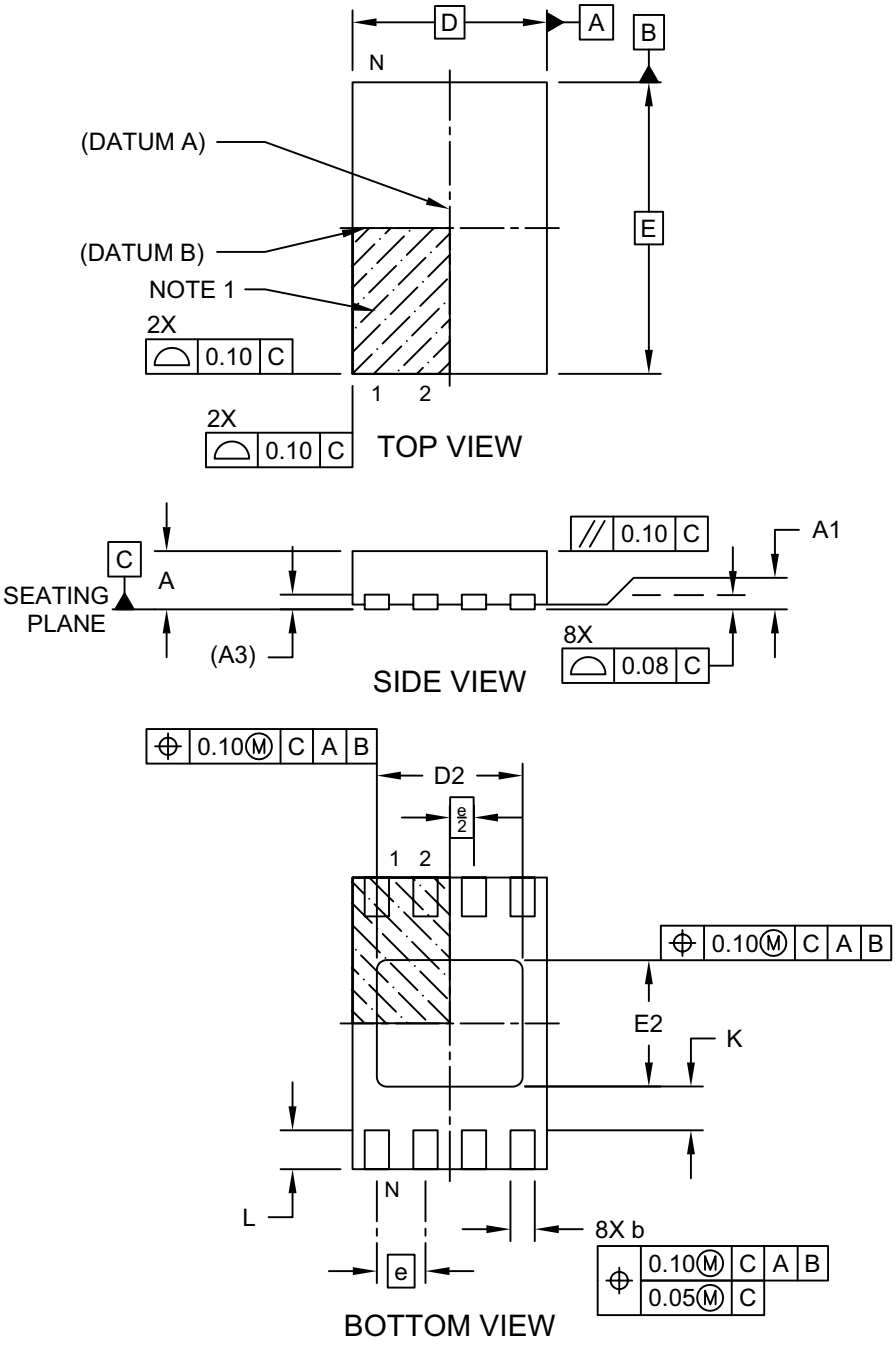
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

### 8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy YNZ Package

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-21355-Q4B Rev A Sheet 1 of 2

## 8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy YNZ Package

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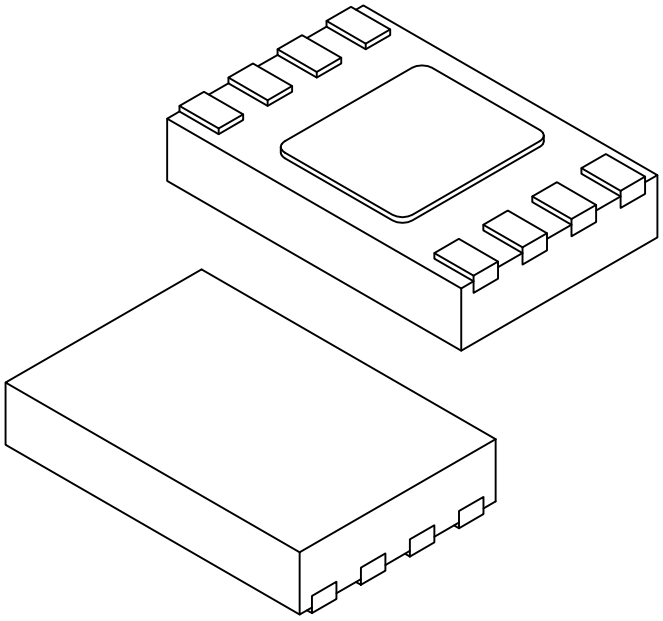


| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.50 | 0.55 | 0.60 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.152 REF | |
| Overall Length | D | | 2.00 BSC | |
| Exposed Pad Length | D2 | 1.40 | 1.50 | 1.60 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.20 | 1.30 | 1.40 |
| Terminal Width | b | 0.18 | 0.25 | 0.30 |
| Terminal Length | L | 0.35 | 0.40 | 0.45 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

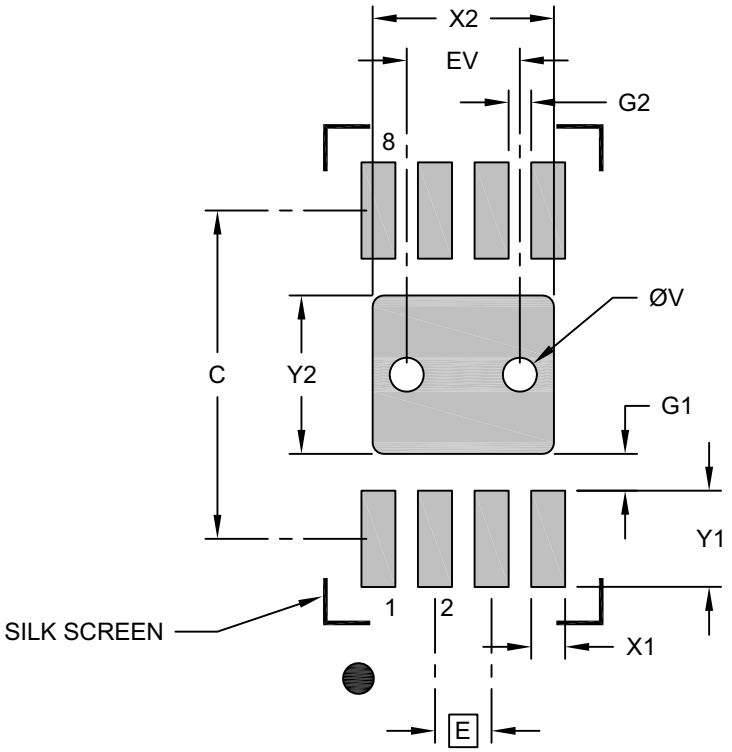
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21355-Q4B Rev A Sheet 2 of 2

### 8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy YNZ Package

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 1.60 |
| Optional Center Pad Length | Y2 | | | 1.40 |
| Contact Pad Spacing | C | | 2.90 | |
| Contact Pad Width (X8) | X1 | | | 0.30 |
| Contact Pad Length (X8) | Y1 | | | 0.85 |
| Contact Pad to Center Pad (X8) | G1 | 0.20 | | |
| Contact Pad to Contact Pad (X6) | G2 | 0.33 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-21355-Q4B Rev A

## APPENDIX A: REVISION HISTORY

### Revision L (05/2019)

Corrected Part Marking for UDFN package. Added note about exposed pad on the TDFN and UDFN packages.

### Revision K (11/2018)

Added the 24FC02 device.

### Revision J (02/2009)

Added TDFN Package; Updated Package Drawings.

### Revision H (08/2008)

Added SC-70 Package; Updated Package Drawings.

### Revision G (03/2007)

Replaced Package Drawings (Rev. AM).

### Revision F (01/2007)

Revised Features section; Changed 1.8V to 1.7V in Tables and text; Revised Ambient Temperature, Section 1.0; Replaced Package Drawings; Revised Product ID section.

### Revision E

Revised Figure 3-2 Control Byte Allocation; Figure 4-1 Byte Write; Figure 4-2 Page Write; Section 6.0 Write Protection; Figure 7-1 Current Address Read; Figure 7-2 Random Read; Figure 7-3 Sequential Read.

### Revision D

Added DFN package.

### Revision C

Corrections to Section 1.0, Electrical Characteristics.

**NOTES:**

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | [X](1) | –X | /XX |
|---|---|---|---|
| Device | Tape and Reel Option | Temperature Range | Package |

**Device:**
- 24AA02: = 1.7V, 2-Kbit $I^2C$ Serial EEPROM
- 24LC02B: = 2.5V, 2-Kbit $I^2C$ Serial EEPROM
- 24FC02: = 1.7V, High Speed, 2-Kbit $I^2C$ Serial EEPROM

**Tape and Reel Option:**
- Blank = Standard packaging (tube or tray)
- T = Tape and Reel(1)

**Temperature Range:**
- I = -40°C to +85°C (Industrial)
- E = -40°C to +125°C (Extended)

**Package:**
- MC = Plastic Dual Flat, No Lead Package – 2x3x0.9 mm Body, 8-lead (DFN)
- MS = Plastic Micro Small Outline Package, 8-lead (MSOP)
- P = Plastic Dual In-Line – 300 mil Body, 8-lead (PDIP)
- LT = Plastic Small Outline Transistor, 5-lead (SC-70) (Tape and Reel only)
- SN = Plastic Small Outline - Narrow, 3.90 mm Body, 8-lead (SOIC)
- OT = Plastic Small Outline Transistor, 5-lead (SOT-23) (Tape and Reel only)
- MNY = Plastic Dual Flat, No Lead Package - 2x3x0.8 mm Body, 8-lead (TDFN)
- ST = Plastic Thin Shrink Small Outline – 4.4 mm, 8-lead (TSSOP)
- MUY = Plastic Dual Flat, No Lead Package - 2x3x0.6 mm Body, 8-lead (UDFN)

**Examples:**

a) 24LC02BT-I/MC: Tape and Reel, Industrial Temperature, 2.5V, DFN package.

b) 24LC02BT-I/MS: Tape and Reel, Industrial Temperature, 2.5V, MSOP package.

c) 24AA02-I/P: Industrial Temperature, 1.7V, PDIP package.

d) 24LC02BT-I/LT: Tape and Reel, Industrial Temperature, 2.5V, SC-70 package.

e) 24AA02-I/SN: Industrial Temperature, 1.7V, SOIC package.

f) 24AA02T-I/OT: Tape and Reel, Industrial Temperature, 1.7V, SOT-23 package.

g) 24AA02T-I/MNY: Tape and Reel, Industrial Temperature, 1.7V, TDFN package.

h) 24AA02T-I/ST: Tape and Reel, Industrial Temperature, 1.7V, TSSOP package.

i) 24FC02-I/P: Industrial Temperature, 1.7V, PDIP package.

j) 24FC02T-I/MUY: Tape and Reel, Industrial Temperature, 1.7V, UDFN package.

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** Contact Microchip for Automotive grade ordering part numbers.

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