PIC16(L)F1825/9

14/20-Pin Flash Microcontrollers with XLP Technology

High-Performance RISC CPU

- Only 49 Instructions to Learn:
  - All single-cycle instructions except branches
- Operating Speed:
  - DC – 32 MHz oscillator/clock input
  - DC – 125 ns instruction cycle
- Up to 16 Kbytes Linear Program Memory Addressing
- Up to 1024 bytes Linear Data Memory Addressing
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Flexible Oscillator Structure

- Precision 32 MHz Internal Oscillator Block:
  - Factory calibrated to ± 1%, typical
  - Software selectable frequencies range of 31 kHz to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- Four Crystal modes up to 32 MHz
- Three External Clock modes up to 32 MHz
- 4x Phase Lock Loop (PLL)
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-Up
- Reference Clock Module:
  - Programmable clock output frequency and duty cycle

Special Microcontroller Features

- 1.8V-5.5V Operation – PIC16F1825/9
- 1.8V-3.6V Operation – PIC16LF1825/9
- Self-Programmable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable Brown-out Reset (BOR)
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Programmable Code Protection
- Power-Saving Sleep mode

Extreme Low-Power Management PIC16LF1825/9 with XLP

- Sleep mode: 20 nA @ 1.8V, typical
- Watchdog Timer: 300 nA @ 1.8V, typical
- Timer1 Oscillator: 650 nA @ 32 kHz, 1.8V, typical
- Operating Current: 48 µA/MHz @ 1.8V, typical

Analog Features

- Analog-to-Digital Converter (ADC) Module:
  - 10-bit resolution, up to 12 channels
  - Auto acquisition capability
  - Conversion available during Sleep
- Analog Comparator Module:
  - Two rail-to-rail analog comparators
  - Power mode control
  - Software controllable hysteresis
- Voltage Reference Module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - 5-bit rail-to-rail resistive DAC with positive and negative reference selection

Peripheral Highlights

- Up to 17 I/O Pins and 1 Input Only Pin:
  - High current sink/source 25 mA/25 mA
  - Programmable weak pull-ups
  - Programmable interrupt-on-change pins
- Timer0: 8-Bit Timer/Counter with 8-Bit Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Dedicated, low-power 32 kHz oscillator driver
- Three Timer2-types: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two Capture, Compare, PWM (CCP) Modules
- Two Enhanced CCP (ECCP) Modules:
  - Software selectable time bases
  - Auto-shutdown and auto-restart
  - PWM steering
- Up to Two Master Synchronous Serial Port (MSSP) with SPI and I^2C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) Module
- mTouch™ Sensing Oscillator Module:
  - Up to 12 input channels

Peripheral Highlights (Continued)

- Data Signal Modulator Module:
  - Selectable modulator and carrier sources
- SR Latch:
  - Multiple Set/Reset input options
  - Emulates 555 Timer applications

PIC12(L)F1822/1840/PIC16(L)F182x/1847 Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data EEPROM (bytes)	Data SRAM (bytes)	I/O's(2)	10-bit ADC (ch)	CapSense (ch)	Comparators	Timers (8/16-bit)	EUSART	MSSP (I^2C™/SPI)	ECCP (Full-Bridge) ECCP (Half-Bridge) CCP	SR Latch	Debug(1)	XLP
PIC12(L)F1822	(1)	2K	256	128	6	4	4	1	2/1	1	1	0/1/0	Y	I/H	Y
PIC12(L)F1840	(2)	4K	256	256	6	4	4	1	2/1	1	1	0/1/0	Y	I/H	Y
PIC16(L)F1823	(1)	2K	256	128	12	8	8	2	2/1	1	1	1/0/0	Y	I/H	Y
PIC16(L)F1824	(3)	4K	256	256	12	8	8	2	4/1	1	1	1/1/2	Y	I/H	Y
PIC16(L)F1825	(4)	8K	256	1024	12	8	8	2	4/1	1	1	1/1/2	Y	I/H	Y
PIC16(L)F1826	(5)	2K	256	256	16	12	12	2	2/1	1	1	1/0/0	Y	I/H	Y
PIC16(L)F1827	(5)	4K	256	384	16	12	12	2	4/1	1	2	1/1/2	Y	I/H	Y
PIC16(L)F1828	(3)	4K	256	256	18	12	12	2	4/1	1	1	1/1/2	Y	I/H	Y
PIC16(L)F1829	(4)	8K	256	1024	18	12	12	2	4/1	1	2	1/1/2	Y	I/H	Y
PIC16(L)F1847	(6)	8K	256	1024	16	12	12	2	4/1	1	2	1/1/2	Y	I/H	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, available using Debug Header.

2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

1: DS41413 PIC12(L)F1822/PIC16(L)F1823 Data Sheet, 8/14-Pin Flash Microcontrollers.

2: DS41441 PIC12(L)F1840 Data Sheet, 8-Pin Flash Microcontrollers.

3: DS41419 PIC16(L)F1824/1828 Data Sheet, 28/40/44-Pin Flash Microcontrollers.

4: DS41440 PIC16(L)F1825/1829 Data Sheet, 14/20-Pin Flash Microcontrollers.

5: DS41391 PIC16(L)F1826/1827 Data Sheet, 18/20/28-Pin Flash Microcontrollers.

6: DS41453 PIC16(L)F1847 Data Sheet, 18/20/28-Pin Flash Microcontrollers.

Note: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

FIGURE 1: 14-PIN DIAGRAM FOR PIC16(L)F1825

PDIP, SOIC, TSSOP

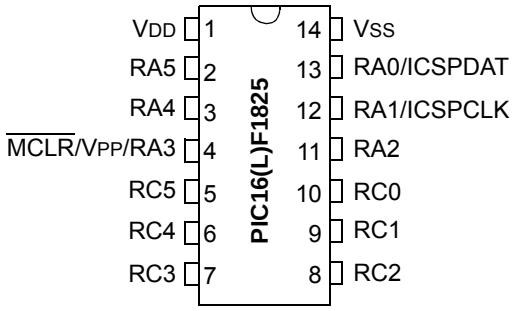

FIGURE 2: 16-PIN DIAGRAM FOR PIC16(L)F1825

QFN, UQFN

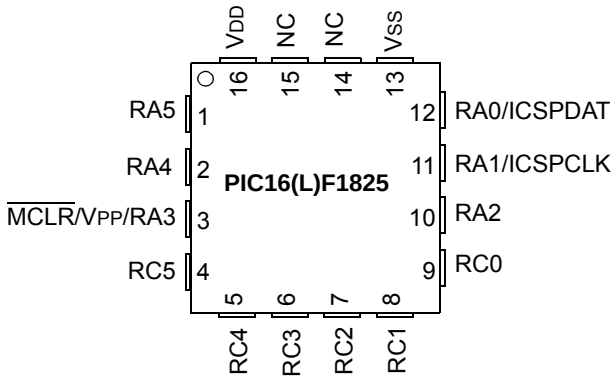

TABLE 1: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16(L)F1825)

I/O	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	A/D	Reference	Cap Sense	Comparator	SR Latch	Timers	ECCP	EUSART	MSSP	Interrupt	Modulator	Pull-up	Basic
RA0	13	12	AN0	VREF- DACOUT	CPS0	C1IN+	—	—	—	TX(1) CK(1)	—	IOC	—	Y	ICSPDAT ICDDAT
RA1	12	11	AN1	VREF+	CPS1	C12IN0-	SRI	—	—	RX(1) DT(1)	—	IOC	—	Y	ICSPCLK ICDCLK
RA2	11	10	AN2	—	CPS2	C1OUT	SRQ	T0CKI	CCP3 FLT0	—	—	INT/ IOC	—	Y	—
RA3	4	3	—	—	—	—	—	T1G(1)	—	—	$\overline{SS1}$(1)	IOC	—	Y	$\overline{MCLR}$ VPP
RA4	3	2	AN3	—	CPS3	—	—	T1G(1) T1OSO	P2B(1)	—	SDO1(1)	IOC	—	Y	OSC2 CLKOUT CLKR
RA5	2	1	—	—	—	—	—	T1CKI T1OSI	CCP2 P2A(1)	—	—	IOC	—	Y	OSC1 CLKIN
RC0	10	9	AN4	—	CPS4	C2IN+	—	—	P1D(1)	—	SCL SCK	—	—	Y	—
RC1	9	8	AN5	—	CPS5	C12IN1-	—	—	CCP4 P1C(1)	—	SDA SDI	—	—	Y	—
RC2	8	7	AN6	—	CPS6	C12IN2-	—	—	P1D(1) P2B(1)	—	SDO1(1)	—	MDCIN1	Y	—
RC3	7	6	AN7	—	CPS7	C12IN3-	—	—	CCP2(1) P1C(1) P2A(1)	—	$\overline{SS1}$(1)	—	MDMIN	Y	—
RC4	6	5	—	—	—	C2OUT	SRNQ	—	P1B	TX(1) CK(1)	—	—	MDOUT	Y	—
RC5	5	4	—	—	—	—	—	—	CCP1 P1A	RX(1) DT(1)	—	—	MDCIN2	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Pin function is selectable via the APFCON0 or APFCON1 register.

FIGURE 3: 20-PIN DIAGRAM FOR PIC16(L)F1829

PDIP, SOIC, SSOP

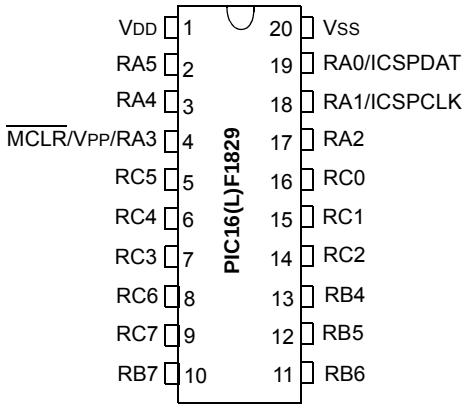

FIGURE 4: 20-PIN DIAGRAM FOR PIC16(L)F1829

QFN, UQFN

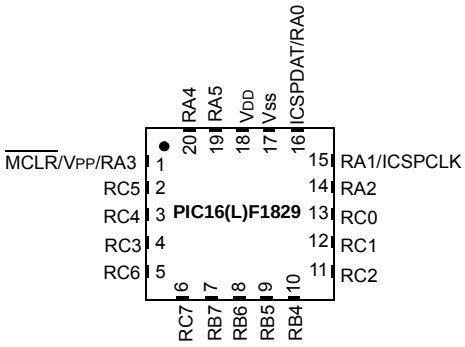

TABLE 2: 20-PIN ALLOCATION TABLE (PIC16(L)F1829)

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin QFN/UQFN	A/D	Reference	Cap Sense	Comparator	SR Latch	Timers	CCP	EUSART	SSP	Interrupt	Modulator	Pull-up	Basic
RA0	19	16	AN0	VREF- DACOUT	CPS0	C1IN+	—	—	—	—	—	IOC	—	Y	ICSPDAT/ ICDDAT
RA1	18	15	AN1	VREF+	CPS1	C12IN0-	SRI	—	—	—	—	IOC	—	Y	ICSPCLK/ ICDCLK
RA2	17	14	AN2	—	CPS2	C1OUT	SRQ	T0CKI	CCP3 FLT0	—	—	INT/ IOC	—	Y	—
RA3	4	1		—	—	—	—	T1G(1)	—	—	—	IOC	—	Y(4)	$\overline{\text{MCLR}}$ VPP
RA4	3	20	AN3	—	CPS3	—	—	T1G(1) T1OSO	P2B(1)	—	$\overline{\text{SS2}}$(1)	IOC	—	Y	OSC2 CLKOUT CLKR
RA5	2	19	—	—	—	—	—	T1CKI T1OSI	CCP2(1) P2A(1)	—	SDO2(1)	IOC	—	Y	OSC1 CLKIN
RB4	13	10	AN10	—	CPS10	—		—	—	—	SDA1 SDI1	IOC	—	Y	—
RB5	12	9	AN11	—	CPS11	—	—	—	—	RX(1) DT(1)	SDA2 SDI2	IOC	—	Y	—
RB6	11	8	—	—	—	—	—	—	—	—	SCL1 SCK1	IOC	—	Y	—
RB7	10	7	—	—	—	—	—	—	—	TX(1) CK(1)	SCL2 SCK2	IOC	—	Y	—
RC0	16	13	AN4	—	CPS4	C2IN+	—	—	P1D(1)	—	$\overline{\text{SS2}}$(1)	—	—	Y	—
RC1	15	12	AN5	—	CPS5	C12IN1-	—	—	P1C(1)	—	SDO2(1)	—	—	Y	—
RC2	14	11	AN6	—	CPS6	C12IN2-	—	—	P1D(1) P2B(1)	—	—	—	MDCIN1	Y	—
RC3	7	4	AN7	—	CPS7	C12IN3-	—	—	P1C(1) CCP2(1) P2A(1)	—	—	—	MDMIN	Y	—
RC4	6	3	—	—	—	C2OUT	SRNQ	—	P1B	TX(1) CK(1)	—	—	MDOUT	Y	—
RC5	5	2	—	—	—	—	—	—	CCP1 P1A	RX(1) DT(1)	—	—	MDCIN2	Y	—
RC6	8	5	AN8	—	CPS8	—	—	—	CCP4	—	$\overline{\text{SS1}}$	—	—	Y	—
RC7	9	6	AN9	—	CPS9	—	—	—	—	—	SDO1	—	—	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	VDD
Vss	20	17	—	—	—	—	—	—	—	—	—	—	—	—	Vss

Note 1: Pin function is selectable via the APFCON0 or APFCON1 register.