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NTE74166
Integrated Circuit
TTL – 8–Bit Parallel or Serial–In/Serial–Out Shift Register

Description:

The NTE74166 is an 8–bit parallel–in or serial–in, serial–out shift register in a 16–Lead plastic DIP type package having the complexity of 77 equivalent gates on a monolithic chip. The parallel–in or serial–in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip–flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low–to–high–level edge of the clock pulse through a two–input positive NOR gate permitting one input to be used as a clock enable or clock–inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free–running and the register can be stopped on command with the other clock input. The clock inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip–flops to zero.

The NTE74166 is compatible with most other TTL logic families and all inputs are buffered to lower the drive requirements to one LS–TTL standard load. Input clamping diodes minimize switching transients an simplify system design.

Features:

- Synchronous Load
- Direct Overriding Clear
- Parallel–to–Serial Conversion

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 5.5V
Power Dissipation, P_D 360mW
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	−800	μA
Low−Level Output Current	I_{OL}	–	–	16	mA
Clock Frequency	f_{clock}	0	–	25	MHz
Width of Clock or Clear Pulse	t_w	20	–	–	ns
Mode−Control Setup Time	t_{su}	30	–	–	ns
Data Setup Time	t_{su}	20	–	–	ns
Hold Time at Any Input	t_h	0	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2	–	–	V
Low Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA	2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	40	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−1.6	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4	−18	–	−57	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5	–	90	122	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time.

Note 5. With all outputs open, 4.5V applied to the serial input, all other inputs except the clock grounded, I_{CC} is measured after a momentary GND, then 4.5V, is applied to clock.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 400Ω, C_L = 15pF	25	35	–	MHz
Propagation Delay Time (From Clear Input to High−to−Low Level Output)	t_{PHL}		–	23	35	ns
Propagation Delay Time (From Clock Input to High−to−Low Level Output)	t_{PHL}		–	20	30	ns
Propagation Delay Time (From Clock Input to Low−to−High Level Output)	t_{PLH}		–	17	26	ns

Function Table:

Inputs						Internal Outputs		Output
$\overline{\text{CLEAR}}$	SHIFT/ $\overline{\text{LOAD}}$	Clock Inhibit	Clock	Serial	Parallel A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Pin Connection Diagram