



# **PIC18F1XK22/LF1XK22**

## **Data Sheet**

20-Pin Flash Microcontrollers  
with nanoWatt XLP™ Technology

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# MICROCHIP

# PIC18F1XK22/LF1XK22

## 20-Pin Flash Microcontrollers with nanoWatt XLP™ Technology

### High Performance RISC CPU:

- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 256 bytes data EEPROM
- Up to 16 Kbytes linear program memory addressing
- Up to 512 bytes linear data memory addressing
- Up to 16 MIPS operation
- 16-bit wide instructions, 8-bit wide data path
- Priority levels for interrupts
- 31-level, software accessible hardware stack
- 8 x 8 single-cycle hardware multiplier

### Flexible Oscillator Structure:

- Precision 16 MHz internal oscillator block:
  - Factory calibrated to  $\pm 1\%$
  - Software selectable frequencies range of 31 kHz to 16 MHz
  - 64 MHz performance available using PLL – no external components required
- Four crystal modes up to 64 MHz
- Two external clock modes up to 64 MHz
- 4X Phase Lock Loop (PLL)
- Secondary oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor
  - Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up

### Special Microcontroller Features:

- Full 5.5V operation – PIC18F1XK22
- 1.8V-3.6V operation – PIC18LF1XK22
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable Brown-out Reset (BOR)
- Extended Watchdog Timer (WDT):
  - Programmable period from 4ms to 131s
- Programmable code protection
- In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug via two pins

### Extreme Low-Power Management PIC18LF1XK22 with nanoWatt XLP™:

- Sleep mode: 34 nA
- Watchdog Timer: 460 nA
- Timer1 Oscillator: 650 nA @ 32 kHz

### Analog Features:

- Analog-to-Digital Converter (ADC) module
  - 10-bit resolution, 12 channels
  - Auto acquisition capability
  - Conversion available during Sleep
- Analog Comparator module:
  - Two rail-to-rail analog comparators
  - Independent input multiplexing
  - Inputs and outputs externally accessible
- Voltage Reference module:
  - Programmable (% of VDD), 16 steps
  - Two 16-level voltage ranges using VREF pins
  - Programmable Fixed Voltage Reference (FVR), 3 levels

### Peripheral Highlights:

- 17 I/O pins and 1 input only pin:
  - High current sink/source 25 mA/25 mA
  - Programmable weak pull-ups
  - Programmable interrupt-on-change
  - Three external interrupt pins
- Four Timer modules:
  - 3 16-bit timers/counters with prescaler
  - 1 8-bit timer/counter with 8-bit period register, prescaler and postscaler
  - Dedicated, low-power Timer1 oscillator
- Enhanced Capture/Compare/PWM (ECCP) module:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and Auto-restart
  - PWM output steering control
- Master Synchronous Serial Port (MSSP) module
  - 3-wire SPI (supports all 4 SPI modes)
  - I<sup>2</sup>C™ Master and Slave modes (Slave mode address masking)
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter module (EUSART)
  - Supports RS-232, RS-485 and LIN 2.0
  - Auto-Baud Detect
  - Auto Wake-up on Break
- SR Latch (555 Timer) module with:
  - Configurable inputs and outputs
  - Supports mTouch™ capacitive sensing applications

# PIC18F1XK22/LF1XK22

TABLE 1: DEVICE OVERVIEW

Device	Program Memory		Data Memory		Pins	I/O <sup>(1)</sup>	10-bit A/D Channels	Comparators	Timers 8-bit/16-bit	ECCP	MSSP	EUSART	SR Latch
	Bytes	Words	SRAM (bytes)	Data EEPROM (bytes)									
PIC18F13K22 PIC18LF13K22	8K	4K	256	256	20	18	12-ch	2	1 / 3	1	1	1	Yes
PIC18F14K22 PIC18LF14K22	16K	8K	512	256	20	18	12-ch	2	1 / 3	1	1	1	Yes

**Note 1:** One pin is input-only.

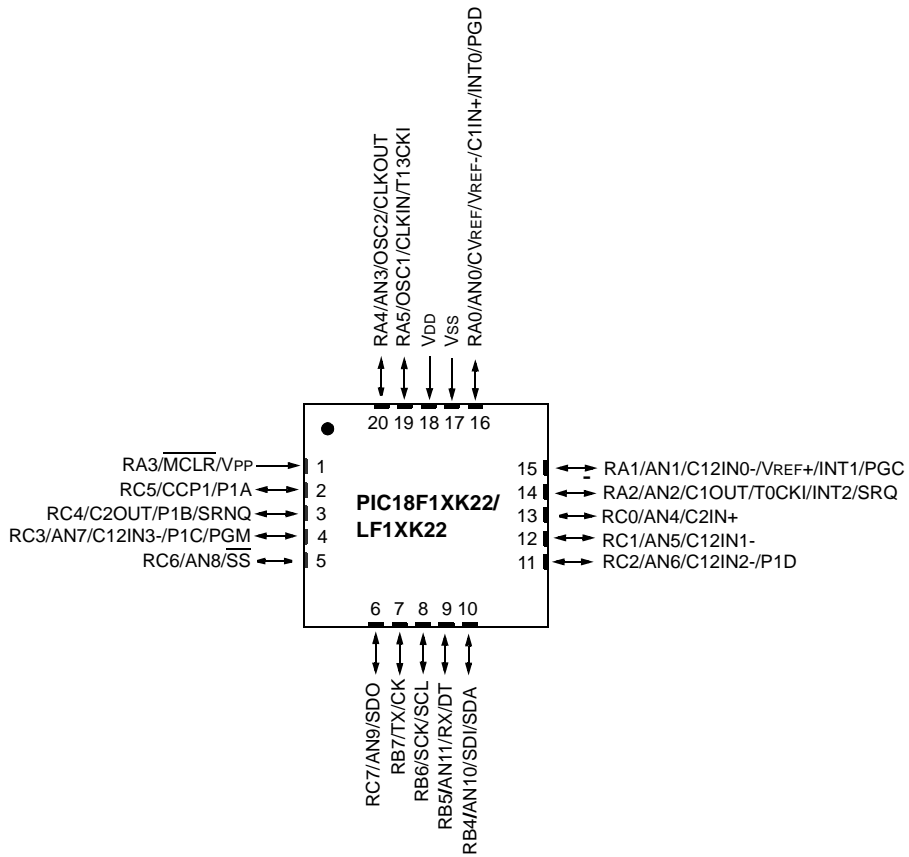
# PIC18F1XK22/LF1XK22

## Pin Diagrams

### 20-pin PDIP, SSOP, SOIC (300 MIL)



### 20-Pin QFN 4x4



# PIC18F1XK22/LF1XK22

**TABLE 1-1: PIC18F1XK22/LF1XK22 PIN SUMMARY**

20-Pin DIL	20-Pin QFN	IO	Analog	Comparator	Reference	ECCP	EUSART	MSSP	SR Latch	Timers	Interrupts	Pull-up	Basic
19	16	RA0	AN0	C1IN+	VREF-/CVREF	—	—	—	—	—	IOC/INT0	Y	PGD
18	15	RA1	AN1	C12IN0-	VREF+	—	—	—	—	—	IOC/INT1	Y	PGC
17	14	RA2	AN2	C1OUT	—	—	—	—	SRQ	T0CKI	IOC/INT2	Y	—
4	1	RA3	—	—	—	—	—	—	—	—	IOC	Y	MCLR/VPP
3	20	RA4	AN3	—	—	—	—	—	—	—	IOC	Y	OSC2/CLKOUT
2	19	RA5	—	—	—	—	—	—	—	T13CKI	IOC	Y	OSC1/CLKIN
13	10	RB4	AN10	—	—	—	—	SDI/SDA	—	—	IOC	Y	—
12	9	RB5	AN11	—	—	—	RX/DT	—	—	—	IOC	Y	—
11	8	RB6	—	—	—	—	—	SCL/SCK	—	—	IOC	Y	—
10	7	RB7	—	—	—	—	TX/CK	—	—	—	IOC	Y	—
16	13	RC0	AN4	C2IN+	—	—	—	—	—	—	—	—	—
15	12	RC1	AN5	C12IN1-	—	—	—	—	—	—	—	—	—
14	11	RC2	AN6	C12IN2-	—	P1D	—	—	—	—	—	—	—
7	4	RC3	AN7	C12IN3-	—	P1C	—	—	—	—	—	—	PGM
6	3	RC4	—	C2OUT	—	P1B	—	—	SRNQ	—	—	—	—
5	2	RC5	—	—	—	CCP1/P1A	—	—	—	—	—	—	—
8	5	RC6	AN8	—	—	—	—	SS	—	—	—	—	—
9	6	RC7	AN9	—	—	—	—	SDO	—	—	—	—	—
1	18	—	—	—	—	—	—	—	—	—	—	—	VDD
20	17	—	—	—	—	—	—	—	—	—	—	—	VSS