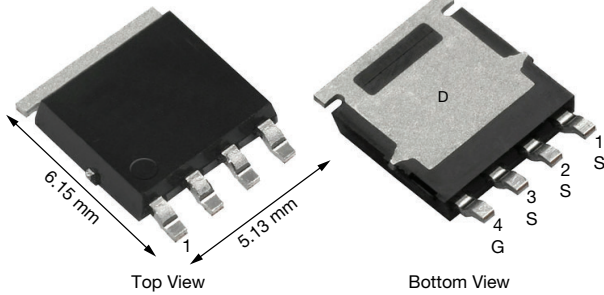


## N-Channel 60 V (D-S) MOSFET

PowerPAK® SO-8L Single



### FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low  $Q_g$  and  $Q_{oss}$  reduce power loss and improve efficiency
- Flexible leads provide resilience to mechanical stress
- 100 %  $R_g$  and UIS tested
- $Q_{gd}/Q_{gs}$  ratio < 1 optimizes switching characteristics
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

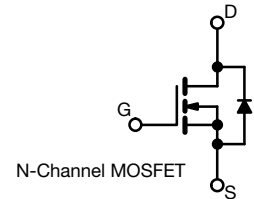


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

PRODUCT SUMMARY	
$V_{DS}$ (V)	60
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0072
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0110
$Q_g$ typ. (nC)	15
$I_D$ (A) <sup>a</sup>	39.3
Configuration	Single

### APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- DC/AC inverters
- Boost converters
- Motor drive control



### ORDERING INFORMATION

Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SiJ462ADP-T1-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	60	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	39.3
		$T_C = 70$ °C	31.4
		$T_A = 25$ °C	15.8 <sup>b, c</sup>
		$T_A = 70$ °C	12.6 <sup>b, c</sup>
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	100	A
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	20.2
		$T_A = 25$ °C	3.2 <sup>b, c</sup>
Single pulse avalanche current	$I_{AS}$	15	A
Single pulse avalanche energy	$E_{AS}$	11.25	mJ
Maximum power dissipation	$P_D$	$T_C = 25$ °C	22.3
		$T_C = 70$ °C	14.2
		$T_A = 25$ °C	3.6 <sup>b, c</sup>
		$T_A = 70$ °C	2.3 <sup>b, c</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>		260	°C

### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b, f</sup>	$R_{thJA}$	27	34	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	4.5	5.6	

#### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W



SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	60	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 1\text{ mA}$	-	33	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-4.7	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	-	2.5	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 75\text{ }^\circ\text{C}$	-	-	20	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	0.0057	0.0072	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	0.0086	0.0110	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 10\text{ A}$	-	49	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{ISS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1235	-	pF
Output capacitance	$C_{OSS}$		-	282	-	
Reverse transfer capacitance	$C_{RSS}$		-	10	-	
Total gate charge	$Q_g$	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	19.8	30	nC
		$V_{DS} = 30\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	9.6	15	
Gate-source charge	$Q_{gs}$		-	3.8	-	
Gate-drain charge	$Q_{gd}$		-	2.9	-	
Output charge	$Q_{OSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	-	17.1	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.3	0.85	1.5	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	11	22	ns
Rise time	$t_r$		-	6	12	
Turn-off delay time	$t_{d(off)}$		-	20	40	
Fall time	$t_f$		-	6	12	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	-	20	40	
Rise time	$t_r$		-	73	146	
Turn-off delay time	$t_{d(off)}$		-	21	42	
Fall time	$t_f$		-	10	20	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	20.2	A
Pulse diode forward current ( $t_p = 100\text{ }\mu\text{s}$ )	$I_{SM}$		-	-	100	
Body diode voltage	$V_{SD}$	$I_S = 5\text{ A}$	-	0.76	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ }^\circ\text{C}$	-	9.5	19	ns
Body diode reverse recovery charge	$Q_{rr}$		-	21	42	nC
Reverse recovery fall time	$t_a$		-	10	-	ns
Reverse recovery rise time	$t_b$		-	11	-	

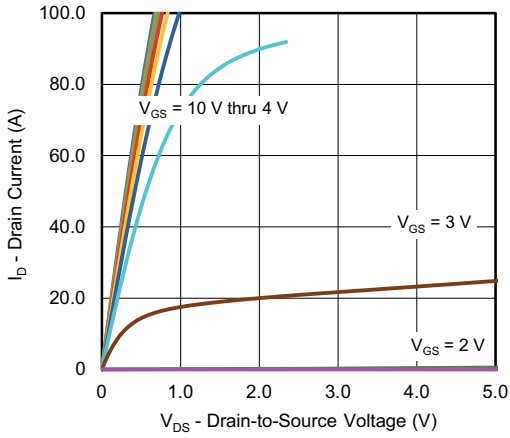
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

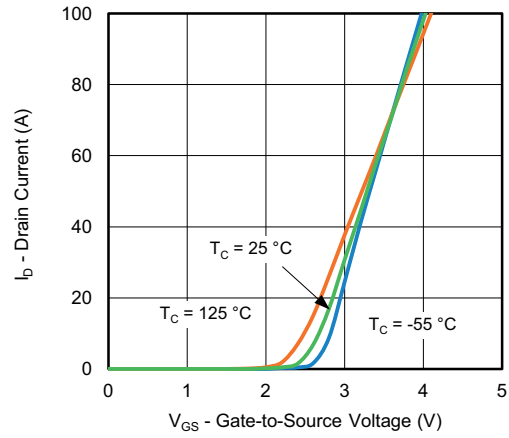
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



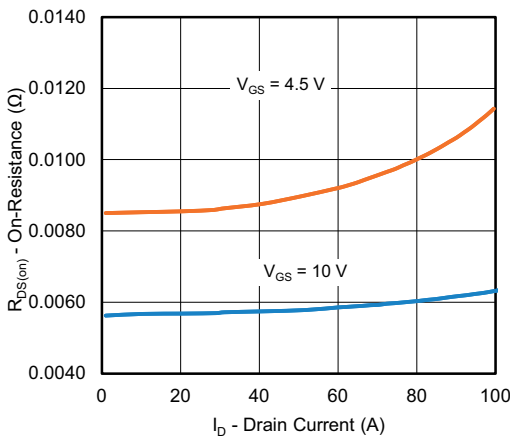
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



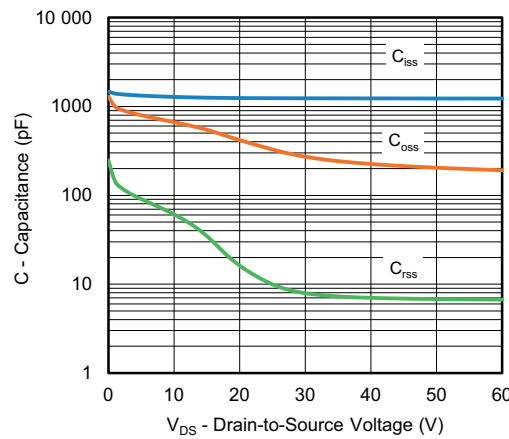
**Output Characteristics**



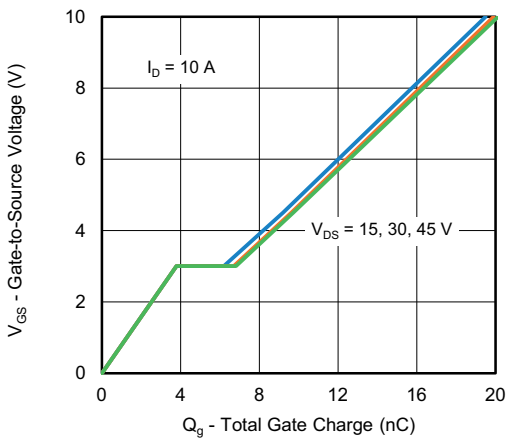
**Transfer Characteristics**



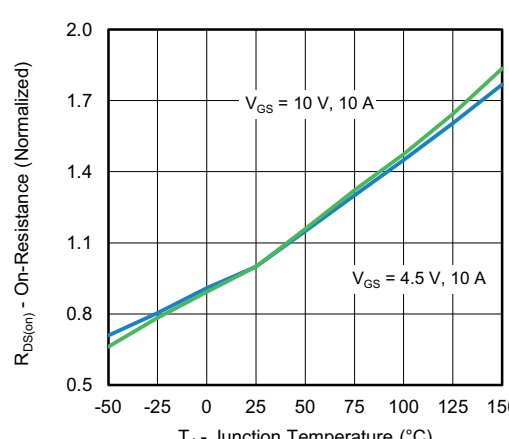
**On-Resistance vs. Drain Current**



**Capacitance**



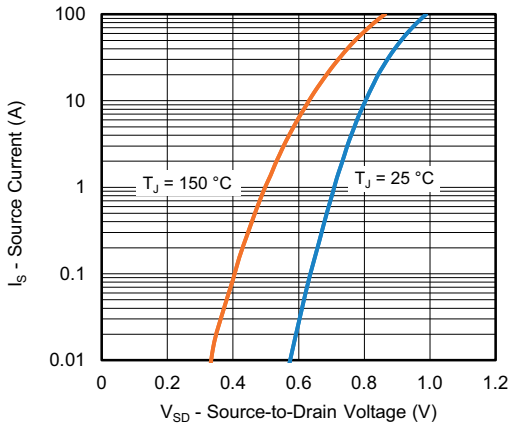
**Gate Charge**



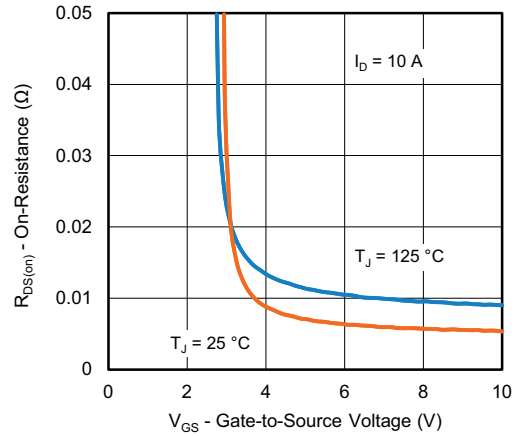
**On-Resistance vs. Junction Temperature**



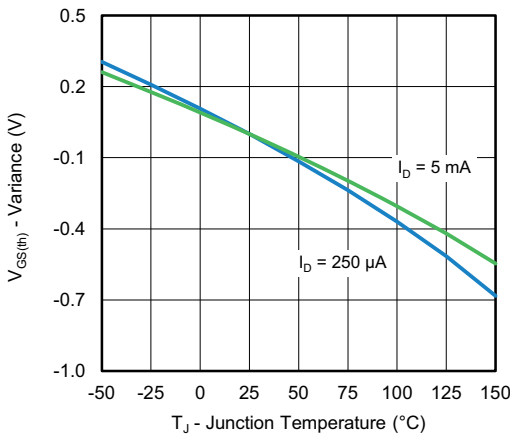
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



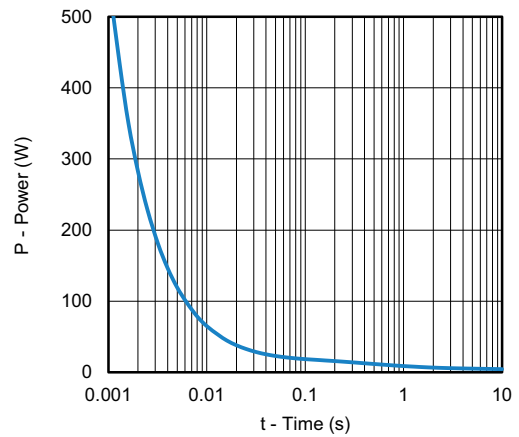
**Source-Drain Diode Forward Voltage**



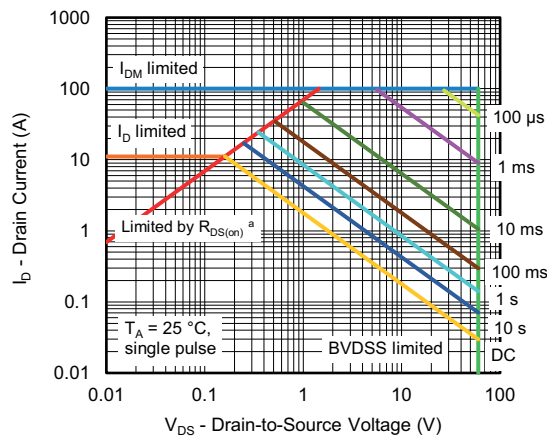
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**



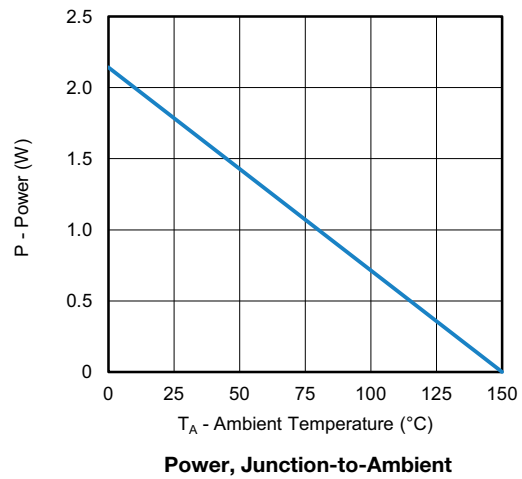
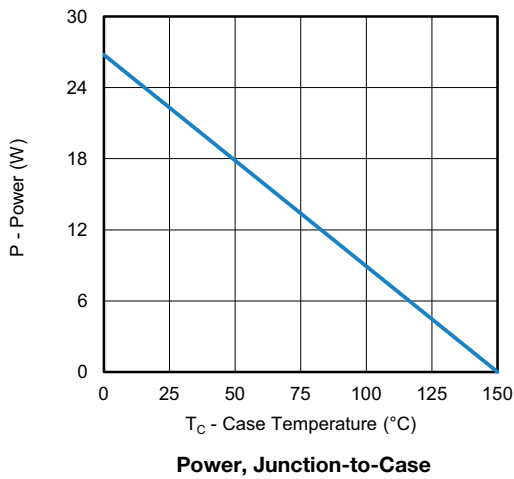
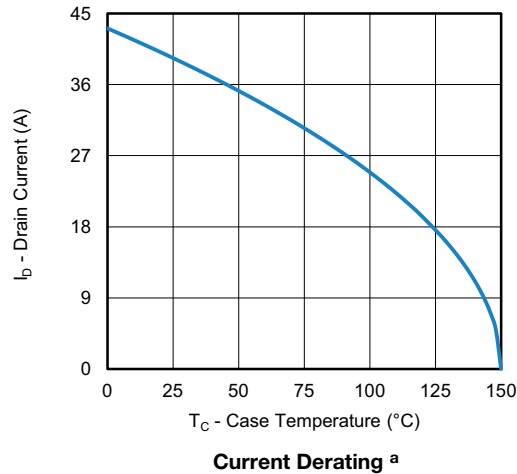
**Safe Operating Area**

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

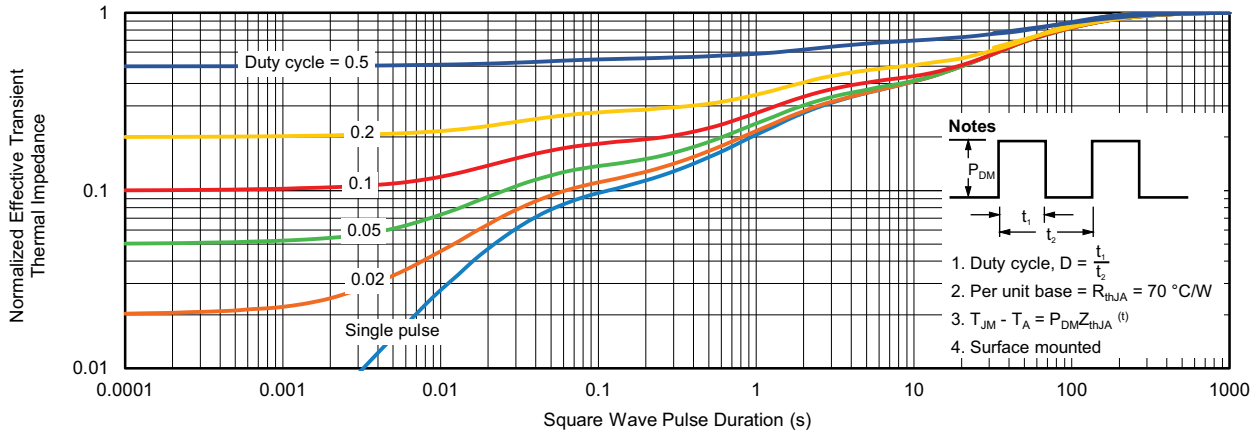


**Note**

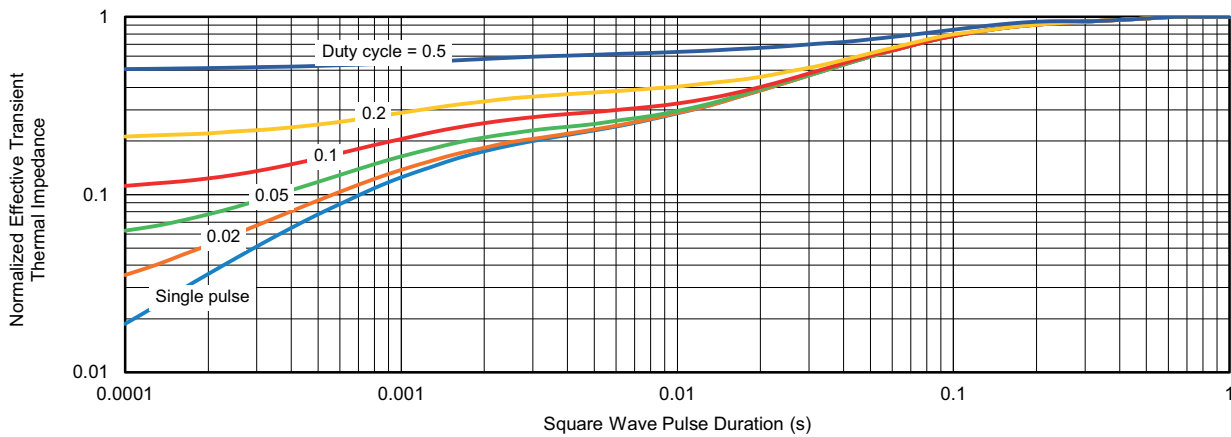
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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