# TJF1052i

## Galvanically isolated high-speed CAN transceiver

Rev. 2 — 15 January 2015 Product data sheet

## 1. General description

The TJF1052i is a high-speed CAN transceiver that provides a galvanically isolated interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The TJF1052i is specifically targeted at industrial applications, where galvanic isolation barriers are needed between the high- and low-voltage parts.

**Safety:** Isolation is required for safety reasons, eg. to protect humans from electric shock or to prevent the electronics being damaged by high voltages.

**Signal integrity:** The isolator uses proprietary capacitive isolation technology to transmit and receive CAN signals. This technology enables more reliable data communications in noisy environments, such as electric pumps, elevators or industrial equipment.

**Performance:** The transceiver is designed for high-speed CAN applications, supplying the differential transmit and receive capability to a CAN protocol controller in a microcontroller. Integrating the galvanic isolation along with the transceiver in the TJF1052i removes the need for stand-alone isolation. It also improves reliability and system performance parameters such as loop delay.

The TJF1052i belongs to the third generation of high-speed CAN transceivers from NXP Semiconductors, offering significant improvements over first- and second-generation devices. It offers improved ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, and also features ideal passive behavior to the CAN bus when the transceiver supply voltage is off.

The TJF1052i implements the CAN physical layer as defined in the current ISO11898 standard (ISO11898-2:2003). Pending the release of the updated version of ISO11898-2 including CAN FD, additional timing parameters defining loop delay symmetry are specified. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 2 Mbit/s.

The TJF1052i is an excellent choice for all types of industrial CAN networks where isolation is required for safety reasons or to enhance signal integrity in noisy environments.

## 2. Features and benefits

### 2.1 General

- Isolator and Transceiver integrated into a single SO16 package, reducing board space
- ISO 11898-2:2003 compliant
- Loop delay symmetry timing enables reliable communication at data rates up to 2 Mbit/s in the CAN FD fast phase

- Flawless cooperation between the Isolator and the Transceiver
  - Fewer components improves reliability in applications
  - Guaranteed performance (eg. max loop delay <220 ns)
- Electrical transient immunity of 45 kV/μs (typ)
- Suitable for use in 12 V and 24 V systems; compatible with 3 V to 5 V microcontrollers
- Bus common mode voltage ($V_{cm}$) = ±25 V
- Low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

### 2.2 Power management

- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus when not powered up (zero load)

### 2.3 Protection

- Up to 5 kV (RMS) rated isolation
- Three versions available (1 kV, 2.5 kV and 5 kV)
- Voltage compliant with UL 1577, IEC 61010 and IEC 60950
- 5 kV (RMS) rated isolation voltage compliant with UL 1577, IEC 61010 and IEC 60950
- High ESD handling capability on the bus pins
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on supply pins

## 3. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD1}$ | supply current 1 | $V_{TXD}$ = 0 V; bus dominant | - | - | 2.6 | mA |
| | | $V_{TXD}$ = $V_{DD1}$; bus recessive | - | - | 5.6 | mA |
| $I_{DD2}$ | supply current 2 | $V_{TXD}$ = 0 V; bus dominant; 60 Ω load | - | - | 70 | mA |
| | | $V_{TXD}$ = $V_{DD1}$; bus recessive | - | - | 10 | mA |
| $V_{uvd(swoff)(VDD2)}$ | switch-off undervoltage detection voltage on pin $V_{DD2}$ | | 1.3 | - | 2.7 | V |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2 at pins CANH and CANL | −8 | - | +8 | kV |
| $V_{CANH}$ | voltage on pin CANH | | −58 | - | +58 | V |
| $V_{CANL}$ | voltage on pin CANL | | −58 | - | +58 | V |
| $T_{vj}$ | virtual junction temperature | | −40 | - | +125 | °C |
| $T_{amb}$ | ambient temperature | | −40 | - | +105 | °C |


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## 4. Ordering information

**Table 2. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | **Name** | **Description** | **Version** |
| TJF1052IT/5<br>TJF1052IT/2<br>TJF1052IT/1 | SO16 | plastic small outline package; 16 leads; body width 7.5 mm | SOT162-1 |

**Table 3. Voltage ratings**

| Type number | Rated insulation voltage according to UL 1577, IEC 61010 and IEC 60950 |
|---|---|
| TJF1052iT/5 | 5 kV (RMS) |
| TJF1052iT/2 | 2.5 kV (RMS) |
| TJF1052iT/1 | 1 kV (RMS) |

## 5. Block diagram

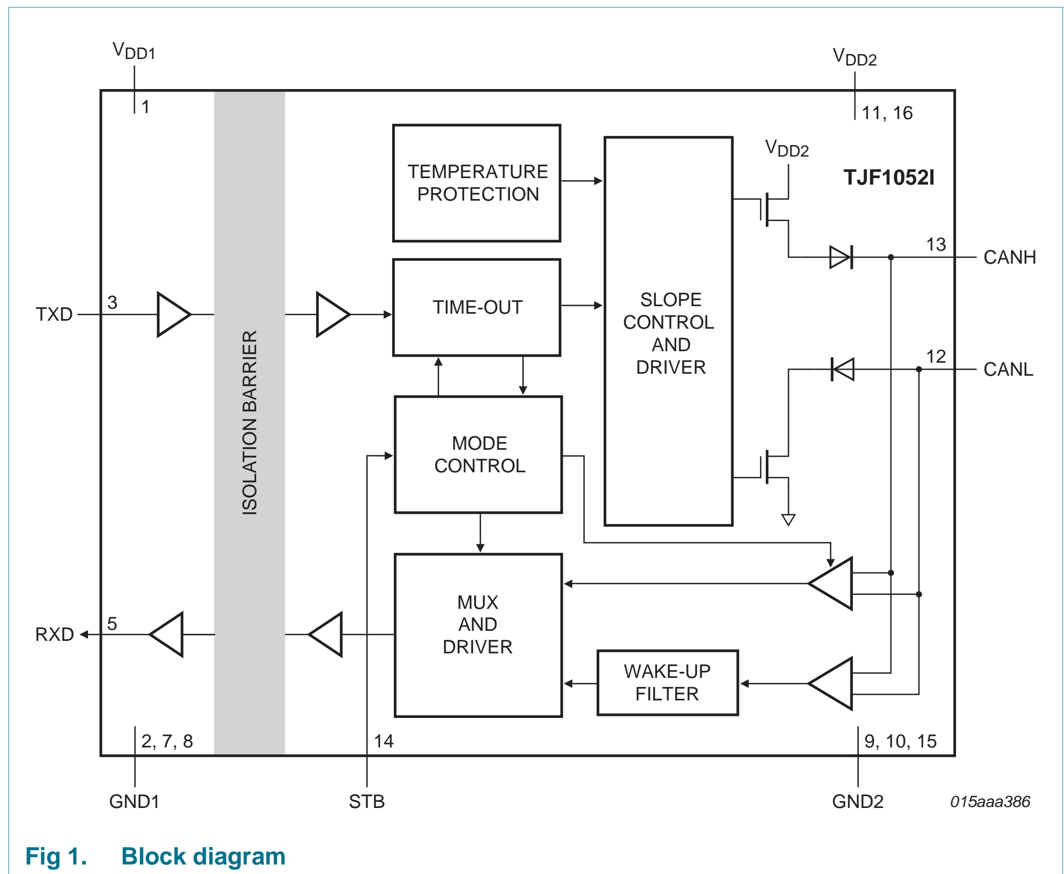


**Fig 1. Block diagram**


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# 6. Pinning information

## 6.1 Pinning

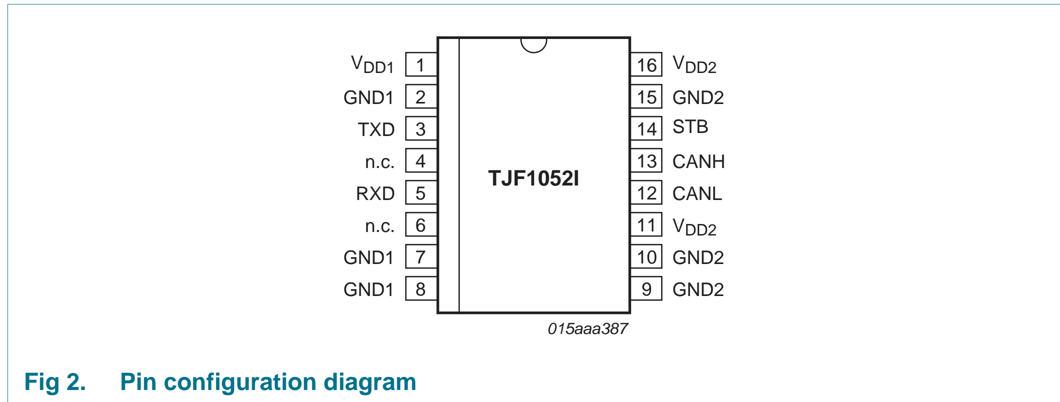


**Fig 2. Pin configuration diagram**

## 6.2 Pin description

**Table 4. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $V_{DD1}$ | 1 | supply voltage 1 |
| GND1 | 2 | ground supply 1[1] |
| TXD | 3 | transmit data input |
| n/c | 4 | not connected |
| RXD | 5 | receive data output; reads out data from the bus lines |
| n/c | 6 | not connected |
| GND1 | 7 | ground supply 1[1] |
| GND1 | 8 | ground supply 1[1] |
| GND2 | 9 | ground supply 2[1] |
| GND2 | 10 | ground supply 2[1] |
| $V_{DD2}$ | 11 | supply voltage 2 |
| CANL | 12 | LOW-level CAN bus line |
| CANH | 13 | HIGH-level CAN bus line |
| STB | 14 | Standby mode control input[2] |
| GND2 | 15 | ground supply 2[1] |
| $V_{DD2}$ | 16 | supply voltage 2 |

[1] All GND1 pins (pins 2, 7 and 8) should be connected together and to ground domain 1. All GND2 pins (pins 9, 10 and 15) should be connected together and to ground domain 2. Refer to the application notes for further information.

[2] Setting STB HIGH disables the CAN bus connection.


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# 7. Functional description

## 7.1 Operation

### 7.1.1 Normal mode

During normal operation, the TJF1052i transceiver transmits and receives data via bus lines CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

The isolator used in the TJF1052i is an AC device that employs on-off keying to guarantee the DC output state at all times. The states of TXD, RXD and the CAN bus at start-up, shut-down and during normal operation are described in Table 5.

Care should be taken regarding power sequencing if the device is used in networks that support remote wake-up (see Section 12 "Application information").

**Table 5. Input/output states at start-up, shut-down and during normal operation**

| TXD | RXD | $V_{DD1}$ | $V_{DD2}$ | CAN | Comments |
|---|---|---|---|---|---|
| H | H | >$V_{uvd(VDD1)}$ | >$V_{uvd(stb)VDD2)}$ | recessive | Normal mode operation |
| L | L | >$V_{uvd(VDD1)}$ | >$V_{uvd(stb)VDD2)}$ | dominant | Normal mode with TXD dominant time-out active |
| X | X | unpowered | >$V_{uvd(stb)VDD2)}$ | dominant | dominant after $V_{DD1}$ power loss until TXD dominant timeout; recessive while $V_{DD2}$ is ramping up from an unpowered state |
| X | L | >$V_{uvd(VDD1)}$ | unpowered | disconnected | RXD transitions L-to-H when $V_{DD2}$ restored |

### 7.1.2 Standby mode

Standby mode is provided to improve the response of the TJF1052i to an undervoltage on $V_{DD2}$. The microcontroller cannot switch the transceiver directly to Standby mode. The TJF1052i switches to Standby mode during $V_{DD2}$ power-up and power-down. See Section 7.2.2 for a description of undervoltage protection on $V_{DD2}$.

## 7.2 Fail-safe features

### 7.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD goes LOW. If the LOW state on TXD persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset by a positive edge on TXD. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

### 7.2.2 Undervoltage protection: $V_{DD2}$

If the voltage on pin $V_{DD2}$ falls below the standby threshold, $V_{uvd(stb)(VDD2)}$, the transceiver switches to Standby mode. In Standby mode, the transceiver is not able to transmit or receive data on the bus lines. The transmitter and the Normal mode receiver are switched off and the bus lines are biased to ground to minimize the supply current. The TJF1052i



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will remain in Standby mode until $V_{DD2}$ rises above $V_{uvd(stb)(VDD2)}$ (max). The low-power receiver continues to monitor the bus while the TJF1052i is in Standby mode. Data on the bus is still reflected onto RXD, but the transfer speed is reduced.

If the voltage on $V_{DD2}$ falls below the switch-off threshold, $V_{uvd(swoff)(VDD2)}$, the transceiver switches off and disengages from the bus (zero load). It is guaranteed to switch on again in Standby mode when $V_{DD2}$ rises above $V_{uvd(swoff)(VDD2)}$ (max).

#### 7.2.3 Undervoltage protection: $V_{DD1}$

If the voltage on pin $V_{DD1}$ falls below the undervoltage detection threshold, $V_{uvd(VDD1)}$, the CAN bus switches to dominant state and the TXD dominant timeout timer is started. RXD will not go high again until the supply voltage has been restored on $V_{DD1}$ ($V_{DD1} > V_{uvd(VDD1)}$).

#### 7.2.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the output drivers are disabled. They are enabled again when the virtual junction temperature falls below $T_{j(sd)}$ and TXD is HIGH. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

### 7.3 Insulation characteristics and safety-related specifications

**Table 6. Isolator characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $d_{L(IO1)}$ | minimum air gap | | [1] | 8.6 | - | - | mm |
| $d_{L(IO2)}$ | minimum external tracking | | [2] | 8.1 | - | - | mm |
| $R_{ins}$ | insulation resistance | $T_A$ = 125 °C | [3] | 100 | - | - | GΩ |
| | | $T_A$ = 150 °C | [3] | 10 | - | - | GΩ |
| - | pollution degree | - | | 2 | - | - | - |
| - | material group (IEC 60664) | | | 2 | - | - | - |

[1] Based on the measured data in the package outline. $d_{L(IO1)}$ is the clearance distance. Note that the clearance distance cannot be larger than the creepage distance ($d_{L(IO2)}$).

[2] Based on the measured data in the package outline. $d_{L(IO2)}$ is the creepage distance. According to IEC 60950-1, normative annex F (also IEC60664 chapter 6.2, Example 11), the effective minimum external tracking is 1.0 mm less due to the presence of an intervening, unconnected conductive part.

[3] Guaranteed by design at a voltage differential of 500 V with the pins on each side of the isolation barrier connected together, simulating a 2-pin device.


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**Table 7. Working voltages and isolation**

| Insulation Characteristics | | | | |
|---|---|---|---|---|
| Parameter | Standard | TJF1052i/1 | TJF1052i/2 | TJF1052i/5 |
| max. working insulation voltage per IEC 60664 ($V_{IORM}$)[1] | IEC 60664 | 300 $V_{RMS}$ | 450 $V_{RMS}$ | 800 $V_{RMS}$ |
| | | 420 $V_{peak}$ | 630 $V_{peak}$ | 1125 $V_{peak}$ |
| max. transient overvoltage per IEC 60664 ($V_{IOTM}$)[2] | $t_{TEST}$ = 1.2/50 μs (certification) IEC 60664 | 2500 $V_{peak}$ | 4000 $V_{peak}$ | 6000 $V_{peak}$ |
| rated insulation voltage per UL 1577 ($V_{ISO}$) | UL 1577 | | | |
| | $t_{TEST}$ = 60 s (qualification) | 1000 $V_{RMS}$ | 2500 $V_{RMS}$ | 5000 $V_{RMS}$ |
| | $t_{TEST}$ = 1 s (production) | 1200 $V_{RMS}$ | 3000 $V_{RMS}$ | 6000 $V_{RMS}$ |
| **Insulation classification in terms of Overvoltage Category[3]** | | | | |
| Insulation type | Max. working voltage | TJF1052i/1 | TJF1052i/2 | TJF1052i/5 |
| basic insulation[4] | ≤150 $V_{RMS}$ | I - III | I - IV | I - IV |
| | ≤300 $V_{RMS}$ | I - II | I - III | I - IV |
| | ≤600 $V_{RMS}$ | I | I - II | I - III |
| | ≤1000 $V_{RMS}$ | - | - | I - II |
| reinforced insulation[4] | ≤150 $V_{RMS}$ | I - II | I - III | I - IV |
| | ≤300 $V_{RMS}$ | I | I - II | I - III |
| | ≤600 $V_{RMS}$ | - | I | I - II |
| | ≤1000 $V_{RMS}$ | - | - | I |

[1] The working voltage is the input-to-output voltage that can be applied without time limit. Which TJF1052i variant should be selected depends on the overvoltage category and the related insulation voltage.

[2] UL stress test is performed at higher than IEC-specified levels.

[3] Based on transient overvoltages as indicated in IEC60664; creepage and clearance distances not taken into account.

[4] Reinforced insulation should have an impulse withstand voltage one step higher than that specified for basic insulation.

**Table 8. Safety approvals**

| Standard | File number |
|---|---|
| IEC 60950 | CB NL-33788 |
| IEC 61010-1 2nd Edition | CB NL-33789 |
| UL1577 | 20131213-E361297 |


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## 8. Limiting values

**Table 9. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages and currents are referenced to GND2 unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CANH}$ | voltage on pin CANH | | | –58 | +58 | V |
| $V_{CANL}$ | voltage on pin CANL | | | –58 | +58 | V |
| $V_{DD1}$ | supply voltage 1 | | [1] | –0.3 | +6.0 | V |
| $V_{DD2}$ | supply voltage 2 | | | –0.3 | +6.0 | V |
| $V_I$ | input voltage | on pin TXD | [1] | –0.3 | $V_{DD1}$ + 0.3 | V |
| $V_O$ | output voltage | on pin RXD | [1] | –0.3 | $V_{DD1}$ + 0.3 | V |
| $I_O$ | output current | on pin RXD | [1] | - | 10 | mA |
| $V_{trt}$ | transient voltage | on pins CANH and CANL | | –150 | +100 | V |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2 (150 pF, 330 Ω) | [2] | | | |
| | | at pins CANH and CANL | | –8 | +8 | kV |
| | | Human Body Model (HBM); 100 pF, 1.5 kΩ | [3] | | | |
| | | at pins CANH and CANL | [4] | –8 | +8 | kV |
| | | at any other pin | | –4 | +4 | kV |
| | | Machine Model (MM); 200 pF, 0.75 μH, 10 Ω | [5] | | | |
| | | at any pin | | –300 | +300 | V |
| | | Charged Device Model (CDM); field Induced charge; 4 pF | [6] | | | |
| | | at corner pins | | –750 | +750 | V |
| | | at any pin | | –500 | +500 | V |
| $T_{vj}$ | virtual junction temperature | | [7] | –40 | +125 | °C |
| $T_{amb}$ | ambient temperature | | | –40 | +105 | °C |
| $T_{stg}$ | storage temperature | | [8] | –65 | +150 | °C |

[1] Referenced to GND1.

[2] According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2.

[3] According to AEC-Q100-002.

[4] ±8 kV to GND2 and $V_{DD2}$; ±6 kV to GND1.

[5] According to AEC-Q100-003.

[6] According to AEC-Q100-011 Rev-C1. The classification level is C4B.

[7] An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value used in the calculation of $T_{vj}$. The rating for $T_{vj}$ limits the allowable combinations of power dissipation (P) and ambient temperature ($T_{amb}$).

[8] If UL compliance is required, the maximum storage temperature is limited to 130 °C.

## 9. Thermal characteristics

**Table 10. Thermal characteristics**

*According to IEC 60747-1.*

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{th(vj-a)}$ | thermal resistance from virtual junction to ambient | in free air | 100 | K/W |


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## 10. Static characteristics

**Table 11. Static characteristics**

*$T_{vj}$ = −40 °C to +125 °C; $V_{DD1}$ = 3.0 V to 5.25 V; $V_{DD2}$ = 4.75 V to 5.25 V unless otherwise specified. Positive currents flow into the IC. All voltages and currents are referenced to GND2 unless otherwise specified*[1].

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **DC supplies; pin $V_{DD1}$ and $V_{DD2}$** | | | | | | | |
| $I_{DD1}$ | supply current 1 | $V_{DD1}$ = 3 V to 5 V; $V_{DD2}$ = 5 V; $V_{TXD}$ = 0 V; bus dominant | [2] | - | - | 2.6 | mA |
| | | $V_{DD1}$ = 3 V to 5 V; $V_{DD2}$ = 5 V; $V_{TXD}$ = $V_{DD1}$; bus recessive | [2] | - | - | 5.6 | mA |
| $I_{DD2}$ | supply current 2 | $V_{DD1}$ = 3 V to 5 V; $V_{DD2}$ = 5 V; $V_{TXD}$ = 0 V; bus dominant; $R_L$ = 60 Ω | | - | - | 70 | mA |
| | | $V_{DD1}$ = 3 V to 5 V; $V_{DD2}$ = 5 V; $V_{TXD}$ = $V_{DD1}$; bus recessive | | - | - | 10 | mA |
| $V_{uvd(stb)(VDD2)}$ | standby undervoltage detection voltage on pin $V_{DD2}$ | | | 3.5 | - | 4.75 | V |
| $V_{uvd(swoff)(VDD2)}$ | switch-off undervoltage detection voltage on pin $V_{DD2}$ | | | 1.3 | - | 2.7 | V |
| $V_{uvd(VDD1)}$ | undervoltage detection voltage on pin $V_{DD1}$ | | [2] | 1.3 | - | 2.7 | V |
| $V_{uvhys}$ | undervoltage hysteresis voltage | on pin $V_{DD1}$ | [2] | 40 | - | 100 | mV |
| | | on pin $V_{DD2}$ | | 80 | - | 200 | mV |
| **CAN transmit data input; pin TXD** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | [2] | 2.0 | - | $V_{DD1}$ | V |
| $V_{IL}$ | LOW-level input voltage | | [2] | 0 | - | 0.8 | V |
| $I_{LI}$ | input leakage current | | [2] | −10 | - | +10 | μA |
| **CAN receive data output; pin RXD** | | | | | | | |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −4 mA | [2] | $V_{DD1}$ − 0.4 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 4 mA | [2] | - | - | 0.4 | V |
| **Standby mode control input; pin STB** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7$V_{CC}$ | - | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | LOW-level input voltage | | | −0.3 | - | 0.3$V_{CC}$ | V |
| $I_{IH}$ | HIGH-level input current | $V_{STB}$ = $V_{CC}$ | | −1 | - | +1 | μA |
| $I_{IL}$ | LOW-level input current | $V_{STB}$ = 0 V | | −15 | - | −1 | μA |
| **Bus lines; pins CANH and CANL** | | | | | | | |
| $V_{O(dom)}$ | dominant output voltage | $V_{TXD}$ = 0 V; t < $t_{to(dom)TXD}$ | | | | | |
| | | pin CANH | | 2.75 | 3.5 | 4.5 | V |
| | | pin CANL | | 0.5 | 1.5 | 2.25 | V |
| $V_{dom(TX)sym}$ | transmitter dominant voltage symmetry | $V_{dom(TX)sym}$ = $V_{CC}$ − $V_{CANH}$ − $V_{CANL}$ | | −400 | - | +400 | mV |


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**Table 11. Static characteristics** *...continued*

*$T_{vj}$ = −40 °C to +125 °C; $V_{DD1}$ = 3.0 V to 5.25 V; $V_{DD2}$ = 4.75 V to 5.25 V unless otherwise specified. Positive currents flow into the IC. All voltages and currents are referenced to GND2 unless otherwise specified*[1].

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{O(dif)bus}$ | bus differential output voltage | $V_{TXD}$ = 0 V; t < $t_{to(dom)TXD}$ $R_L$ = 45 Ω to 65 Ω | | 1.5 | - | 3 | V |
| | | $V_{TXD}$ = $V_{CC}$ recessive; no load | | −50 | - | +50 | mV |
| $V_{O(rec)}$ | recessive output voltage | Normal mode; $V_{TXD}$ = $V_{CC}$; no load | | 2 | $0.5V_{CC}$ | 3 | V |
| $V_{th(RX)dif}$ | differential receiver threshold voltage | $V_{cm(CAN)}$ = −25 V to +25 V | [3] | | | | |
| | | Normal mode | | 0.5 | - | 0.9 | V |
| | | Standby mode; $V_{cm(CAN)}$ = −12 V to +12 V | [4] | 0.4 | - | 1.15 | V |
| $V_{hys(RX)dif}$ | differential receiver hysteresis voltage | $V_{cm(CAN)}$ = −25 V to +25 V Normal mode | | - | 165 | - | mV |
| $I_{O(sc)dom}$ | dominant short-circuit output current | $V_{TXD}$ = 0 V; t < $t_{to(dom)TXD}$; $V_{DD2}$ = 5 V | | | | | |
| | | pin CANH; $V_{CANH}$ = 0 V | | −100 | −70 | −40 | mA |
| | | pin CANL; $V_{CANL}$ = 5 V / 40 V | | 40 | 70 | 100 | mA |
| $I_{O(sc)rec}$ | recessive short-circuit output current | Normal mode; $V_{TXD}$ = $V_{DD1}$ $V_{CANH}$ = $V_{CANL}$ = −27 V to +32 V | | −5 | - | +5 | mA |
| $I_L$ | leakage current | $V_{DD2}$ = 0 V; $V_{CANH}$ = $V_{CANL}$ = 5 V | | −3 | - | +3 | μA |
| $R_i$ | input resistance | | | 9 | 15 | 28 | kΩ |
| $\Delta R_i$ | input resistance deviation | between $V_{CANH}$ and $V_{CANL}$ | | −3 | - | +3 | % |
| $R_{i(dif)}$ | differential input resistance | | | 19 | 30 | 52 | kΩ |
| $C_{i(cm)}$ | common-mode input capacitance | | [5] | - | - | 20 | pF |
| $C_{i(dif)}$ | differential input capacitance | | [5] | - | - | 10 | pF |
| **Temperature detection** | | | | | | | |
| $T_{j(sd)}$ | shutdown junction temperature | | [5] [6] | - | 190 | - | °C |

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Referenced to GND1.

[3] $V_{cm(CAN)}$ is the common mode voltage of CANH and CANL.

[4] Standby mode entered when $V_{DD2}$ falls below $V_{uvd(stb)(VDD2)}$.

[5] Guaranteed by design.

[6] RXD is LOW during thermal shutdown.


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## 11. Dynamic characteristics

**Table 12. Dynamic characteristics**

*$T_{vj}$ = –40 °C to +125 °C; $V_{DD1}$ = 3.0 V to 5.25 V; $V_{DD2}$ = 4.75 V to 5.25 V unless otherwise specified*[1].

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 3** | | | | | | |
| $t_{d(TXD-busdom)}$ | delay time from TXD to bus dominant | Normal mode | - | 72 | 120 | ns |
| $t_{d(TXD-busrec)}$ | delay time from TXD to bus recessive | Normal mode | - | 97 | 120 | ns |
| $t_{d(busdom-RXD)}$ | delay time from bus dominant to RXD | Normal mode | - | 67 | 130 | ns |
| $t_{d(busrec-RXD)}$ | delay time from bus recessive to RXD | Normal mode | - | 72 | 130 | ns |
| $t_{PD(TXD-RXD)}$ | propagation delay from TXD to RXD | Normal mode | 72 | - | 220 | ns |
| $t_{bit(RXD)}$ | bit time on pin RXD | $t_{bit(TXD)}$ = 500 ns [2] | 400 | - | 550 | ns |
| $t_{to(dom)TXD}$ | TXD dominant time-out time | $V_{TXD}$ = 0 V; Normal mode | 0.3 | 1.7 | 5 | ms |
| CMTI | common-mode transient immunity | $V_I = V_{DD1}$ or $V_I$ = 0 V [3] | 20 | 45 | - | kV/μs |
| $t_{startup}$ | start-up time | [4] | - | - | 500 | μs |

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] See Figure 4.

[3] See Figure 6.

[4] The start-up time is the time from the application of power to valid data at the output. Guaranteed by design.



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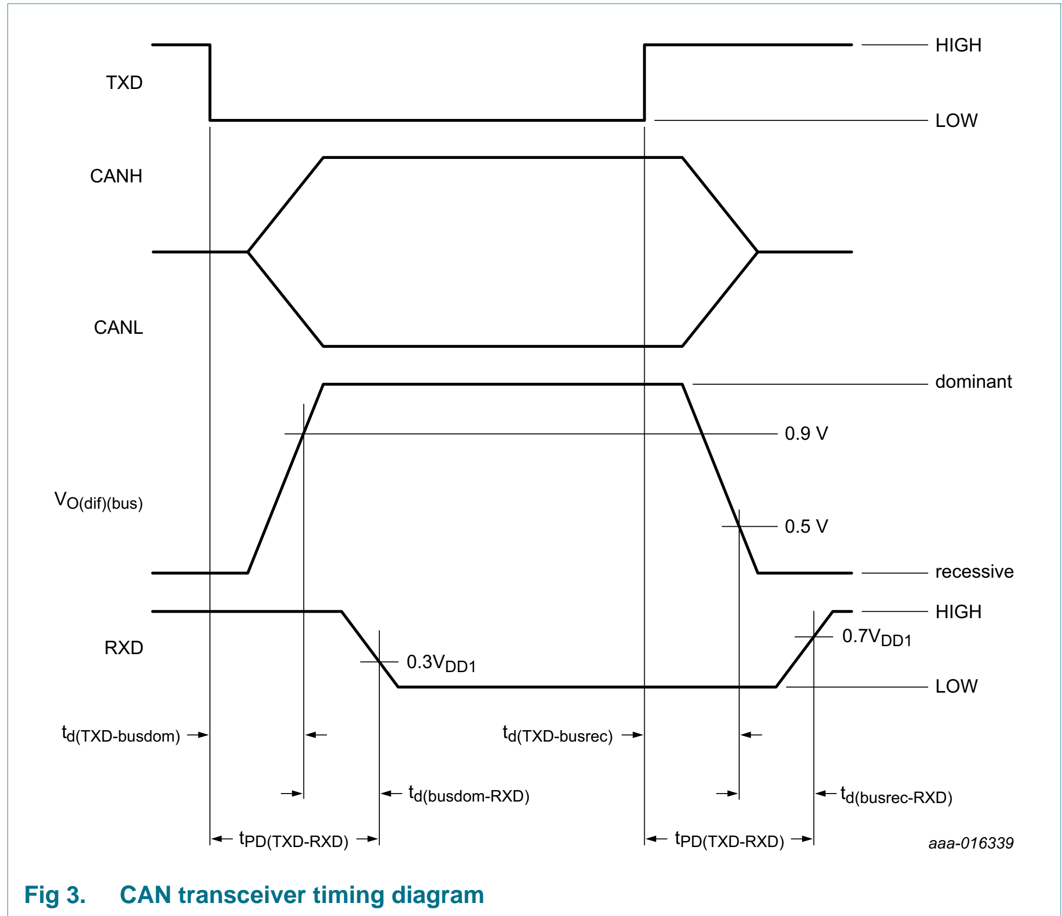


**Fig 3. CAN transceiver timing diagram**

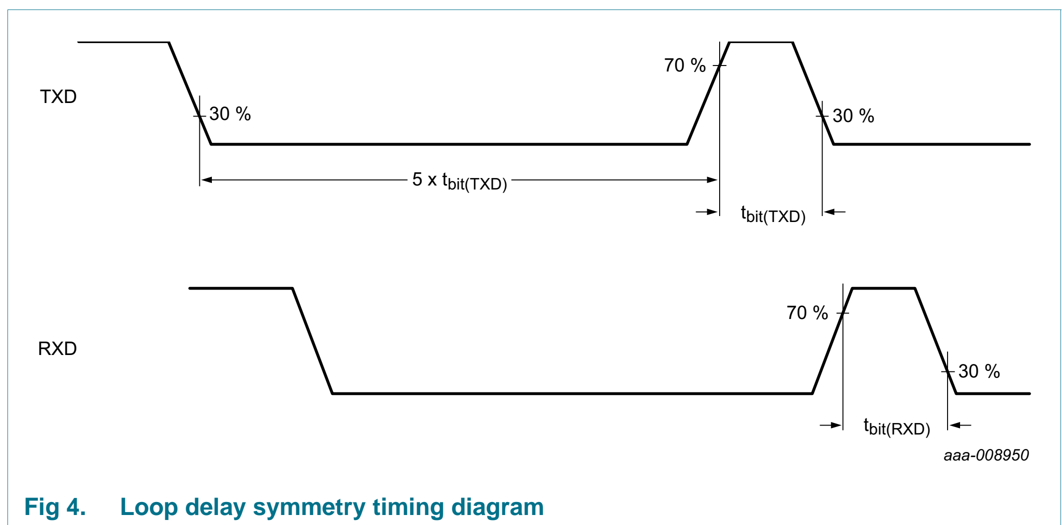


**Fig 4. Loop delay symmetry timing diagram**


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# 12. Application information

Isolated CAN applications are becoming more and more common in industrial automation processes. The TJF1052i is the ideal solution for use in DeviceNet networks or in applications that require an isolated CAN node. The device can also be used to isolate high-voltage on-demand pumps and motors in belt elimination projects.

If the TJF1052i is used in a HS-CAN network that supports remote bus wake-up, the power-down sequence of the supplies must be managed properly to avoid a dominant pulse on the CAN bus. $V_{DD2}$ should pass the minimum undervoltage threshold ($V_{uvd(stb)(VDD2)(min)}$) before $V_{DD1}$ falls below its maximum undervoltage detection threshold ($V_{uvd(VDD1)(max)}$). Power-up sequencing can happen in any order.

Digital inputs and outputs are 3 V compliant, allowing the TJF1052i to interface directly with 3 V and 5 V microcontrollers.

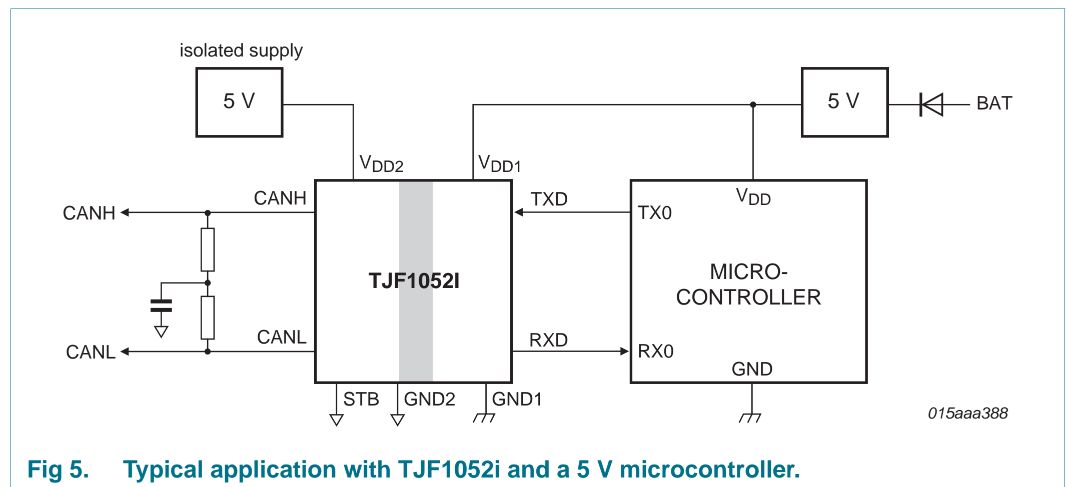


**Fig 5. Typical application with TJF1052i and a 5 V microcontroller.**

## 12.1 Application hints

Further information on the application of the TJF1052i can be found in NXP application hints *AH1301 Application Hints - TJA1052i Galvanic Isolated High Speed CAN Transceiver.*


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## 13. Test information

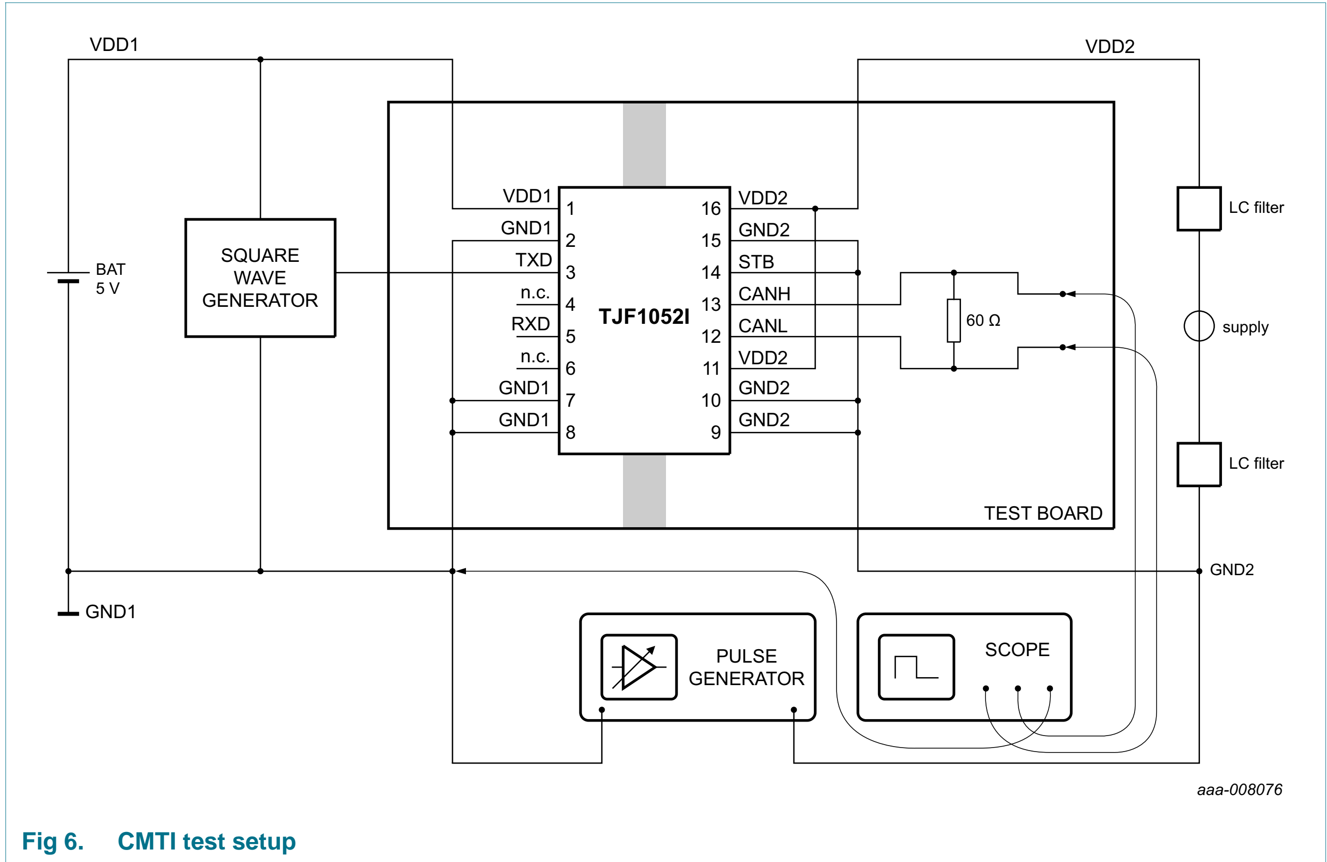


Fig 6. CMTI test setup

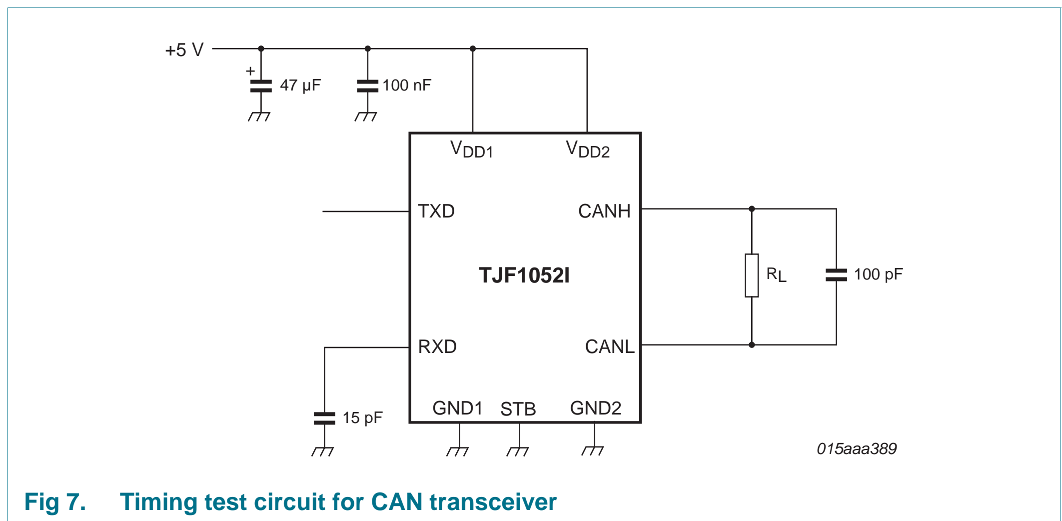


Fig 7. Timing test circuit for CAN transceiver


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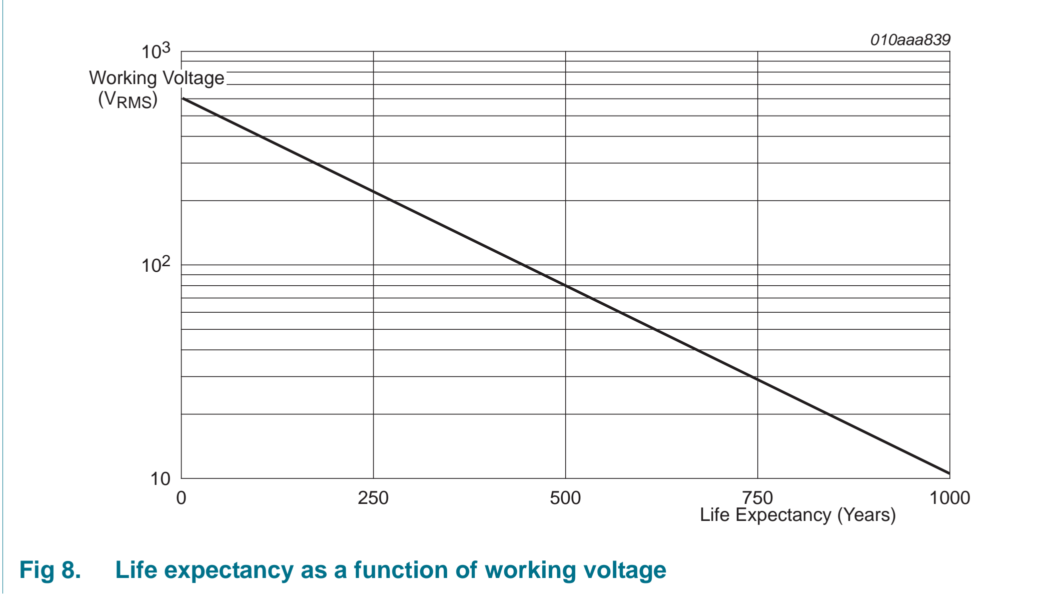


**Fig 8. Life expectancy as a function of working voltage**


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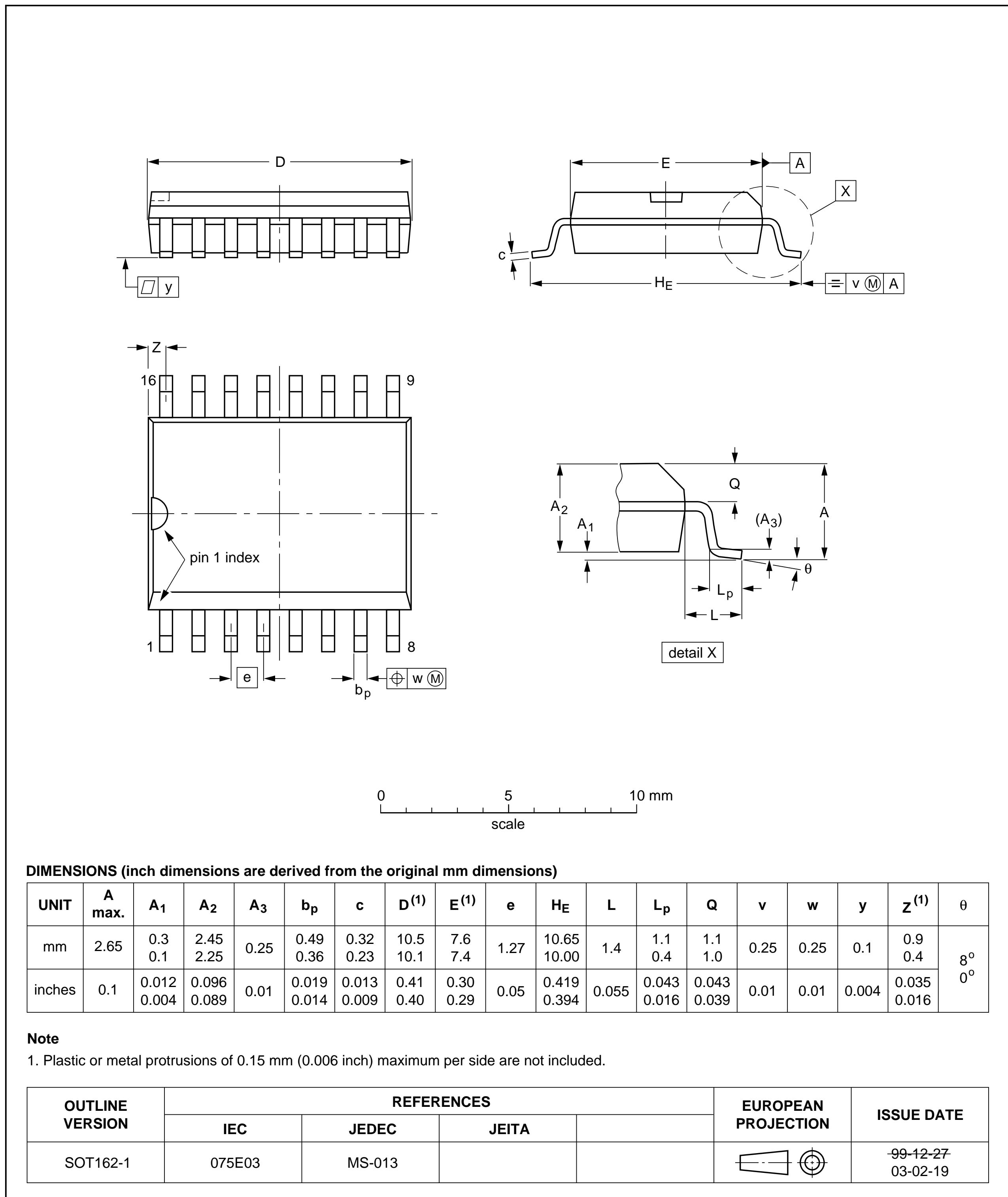
## 14. Package outline

**SO16: plastic small outline package; 16 leads; body width 7.5 mm** **SOT162-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D(1) | E(1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z(1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 10.5<br>10.1 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | 8°<br>0° |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.41<br>0.40 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT162-1 | 075E03 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 9. Package outline SOT162-1 (SO16)**



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# 15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

# 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 16.3 Wave soldering

Key characteristics in wave soldering are:



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- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

**Table 13. SnPb eutectic process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 14. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.


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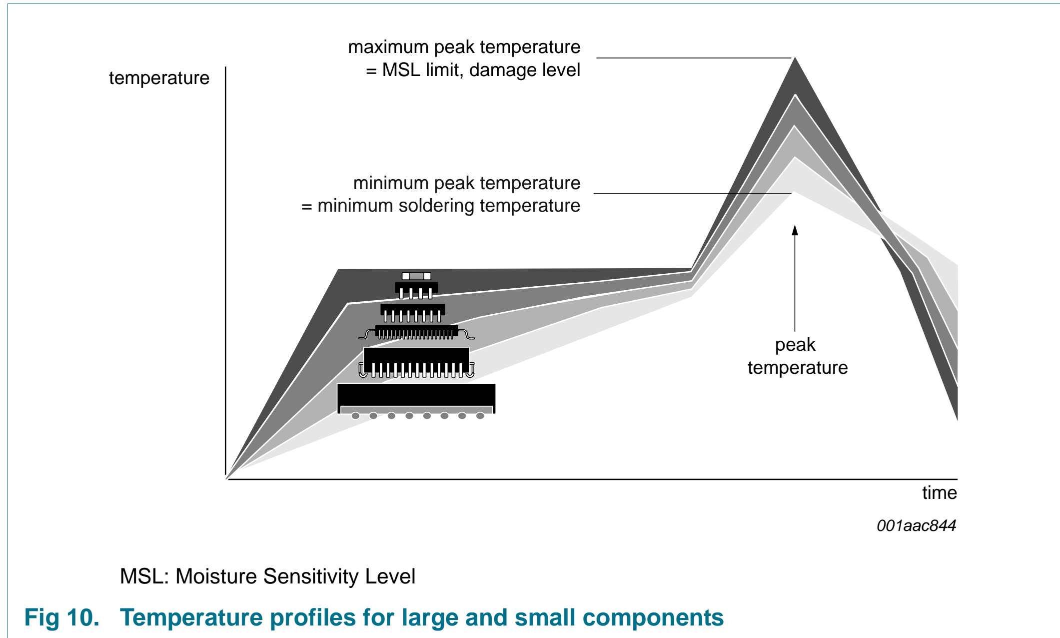


MSL: Moisture Sensitivity Level

**Fig 10. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 17. Revision history

**Table 15. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TJF1052I v.2 | 20150115 | Product data sheet | - | TJF1052I v.1 |
| Modifications: | • Section 1: text revised (4th paragraph); paragraph added<br>• Section 2: minor amendments to text<br>• Section 2.1: features added<br>• UL1577 certification added (Section 2.3 third bullet; Table 8 file number added)<br>• Table 1, Table 9: measurements conditions changed ($V_{CANH}$, $V_{CANL}$)<br>• Section 7.1.1: minor changes to text<br>• Table 6: measurement conditions changed: $R_{ins}$; Table note 3 revised<br>• Table 8: file numbers updated<br>• Table 9: measurements conditions changed: $V_{ESD}$;; table note section revised<br>• Table 11: Table note 1 added along with references to Table note 2; parameters renamed: $I_{O(sc)dom}$ and $I_{O(sc)rec}$<br>• Table 12: parameter $t_{bit(RXD)}$ added; Table note 1, Table note 2 and Figure 4 added; parameter $f_{data}$ deleted<br>• Figure 3, Figure 6 amended<br>• Section 12.1 "Application hints": added<br>• Section 18.3: 'Translations' disclaimer added | | | |
| TJF1052I v.1 | 20130710 | Product data sheet | - | - |



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