

**16-Mbit (1M x 16 / 2M x 8) Static RAM**

**Features**

- TSOP I package configurable as 1M x 16 or as 2M x 8 SRAM
- Very high speed: 45 ns
- Wide voltage range: 2.20V–3.60V
- Ultra low standby power
  - Typical standby current: 1.5  $\mu$ A
  - Maximum standby current: 12  $\mu$ A
- Ultra low active power
  - Typical active current: 2.2 mA @ f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed/power
- Offered in Pb-free 48-Ball VFBGA and 48-Pin TSOP I packages

**Functional Description**

The CY62167EV30 is a high performance CMOS static RAM organized as 1M words by 16 bits/2M words by 8 bits. This device features an advanced circuit design designed to provide an ultra low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications

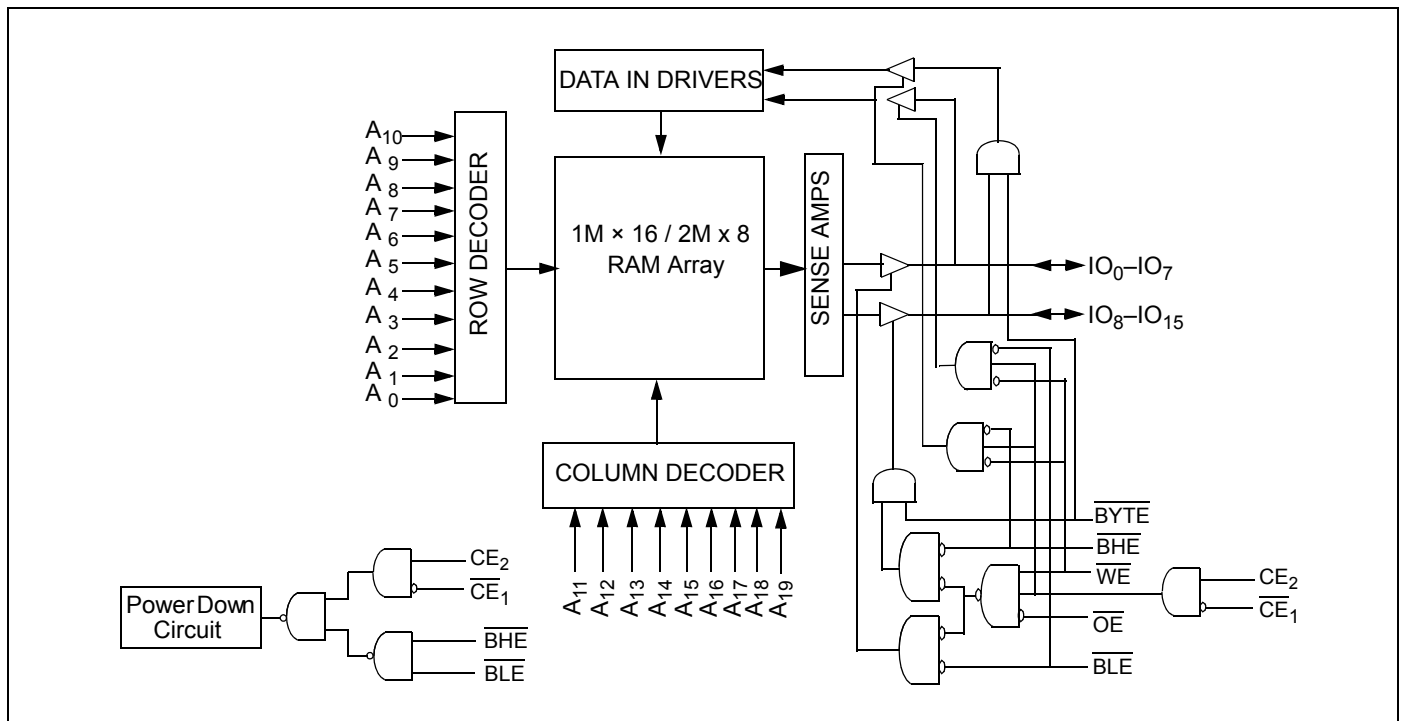
such as cellular telephones. The device also has an automatic power down feature that reduces power consumption by 99% when addresses are not toggling. Place the device into standby mode when deselected ( $CE_1$  HIGH or  $CE_2$  LOW or both BHE and BLE are HIGH). The input and output pins ( $IO_0$  through  $IO_{15}$ ) are placed in a high impedance state when: the device is deselected ( $CE_1$  HIGH or  $CE_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or a write operation is in progress ( $CE_1$  LOW,  $CE_2$  HIGH and WE LOW).

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from IO pins ( $IO_0$  through  $IO_7$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ). If Byte High Enable (BHE) is LOW, then data from the IO pins ( $IO_8$  through  $IO_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on  $IO_0$  to  $IO_7$ . If Byte High Enable (BHE) is LOW, then data from memory appears on  $IO_8$  to  $IO_{15}$ . See the "Truth Table" on page 9 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

**Logic Block Diagram**



## Pin Configuration

Figure 1. 48-Ball VFBGA (6 x 7 x 1mm) / (6 x 8 x 1mm) Top View [1, 2, 3]

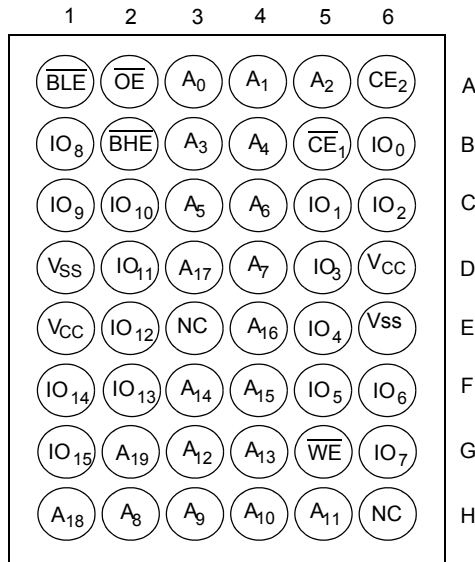
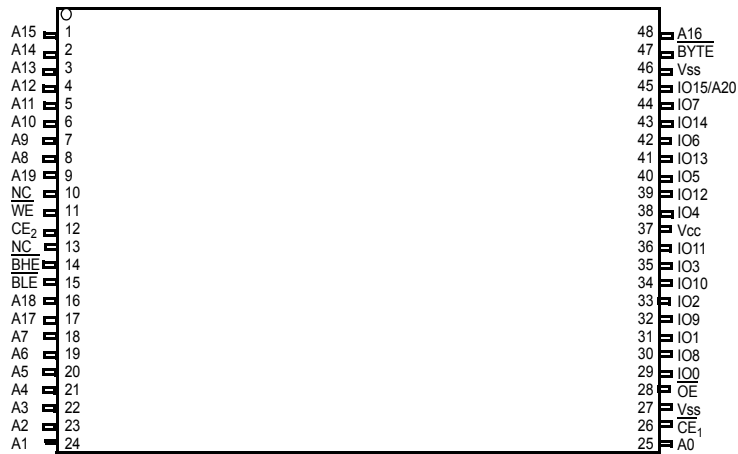


Figure 2. 48-Pin TSOP I Top View [3, 4]



## Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (µA)	
					f = 1 MHz		f = f <sub>max</sub>			
Min	Typ <sup>[5]</sup>	Max	Typ <sup>[5]</sup>	Max	Typ <sup>[5]</sup>	Max	Typ <sup>[5]</sup>	Max		
CY62167EV30LL	2.20	3.0	3.60	45	2.2	4.0	25	30	1.5	12

### Notes

- The information related to 6 x 7 x 1 mm VFBGA package is preliminary.
- Ball H6 for the VFBGA package can be used to upgrade to a 32M density.
- NC pins are not connected on the die.
- The BYTE pin in the 48-TSOP I package has to be tied to V<sub>CC</sub> to use the device as a 1M X 16 SRAM. The 48-TSOP I package can also be used as a 2M X 8 SRAM by tying the BYTE signal to V<sub>SS</sub>. In the 2M x 8 configuration, Pin 45 is A20, while BHE, BLE and IO<sub>8</sub> to IO<sub>14</sub> pins are not used.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(typ), T<sub>A</sub> = 25°C.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to + 150°C

Ambient Temperature with Power Applied ..... -55°C to + 125°C

Supply Voltage to Ground Potential ..... -0.3V to 3.9V  $V_{CC(max)} + 0.3V$

DC Voltage Applied to Outputs in High Z State<sup>[6, 7]</sup> ..... -0.3V to 3.9V  $V_{CC(max)} + 0.3V$

DC Input Voltage<sup>[6, 7]</sup> ..... -0.3V to 3.9V ( $V_{CC(max)} + 0.3V$ )

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (MIL-STD-883, Method 3015)

Latch up Current ..... >200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[8]</sup>
CY62167EV30LL	Industrial	-40°C to +85°C	2.2V to 3.6V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ <sup>[5]</sup>	Max	
V <sub>OH</sub>	Output HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OH</sub> = -0.1 mA	2.0			V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OH</sub> = -1.0 mA	2.4			V
V <sub>OL</sub>	Output LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OL</sub> = 0.1 mA			0.4	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OL</sub> = 2.1 mA			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		1.8		V <sub>CC</sub> + 0.3V	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		2.2		V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		-0.3		0.6	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	For VFPGA package	-0.3		0.8	V
			For TSOP I package	-0.3		0.7 <sup>[9]</sup>	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = V <sub>CC(max)</sub> I <sub>OUT</sub> = 0 mA CMOS levels		25	30	mA
		f = 1 MHz			2.2	4.0	mA
I <sub>SB1</sub>	Automatic CE Power Down Current—CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V or CE <sub>2</sub> ≤ 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V <sub>CC</sub> = 3.60V			1.5	12	μA
I <sub>SB2</sub> <sup>[10]</sup>	Automatic CE Power Down Current—CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V or CE <sub>2</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.60V			1.5	12	μA

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz,	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF

### Notes

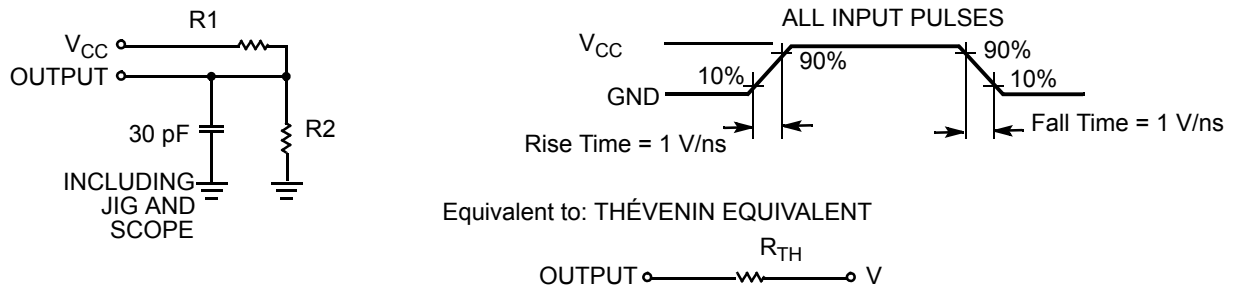
- V<sub>IL</sub> (min) = -2.0V for pulse durations less than 20 ns.
- V<sub>IH</sub> (max) = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC</sub> (min) and 200 μs wait time after V<sub>CC</sub> stabilization.
- Under DC conditions the device meets a V<sub>IL</sub> of 0.8V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7V. This is applicable to TSOP I package only.
- Only chip enables (CE<sub>1</sub> and CE<sub>2</sub>), byte enables (BHE and BLE) and BYTE must be tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	VFBGA (6 x 7 x 1mm)	VFBGA (6 x 8 x 1mm)	TSOP I	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	27.74	55	60	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		9.84	16	4.3	°C/W

## AC Test Loads and Waveforms



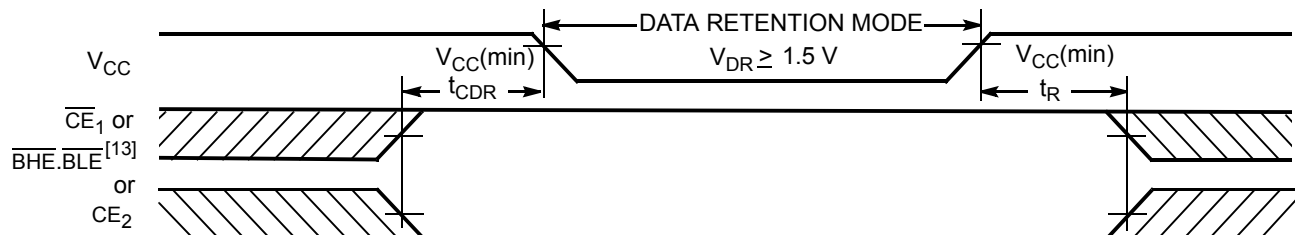
Parameters	2.2V to 2.7V	2.7V to 3.6V	Unit
R1	16667	1103	$\Omega$
R2	15385	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.20	1.75	V

## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[5]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.5			V
$I_{CCDR}^{[10]}$	Data Retention Current	$V_{CC} = 1.5V$ to $3.0V$ , $CE_1 \geq V_{CC} - 0.2V$ , $CE_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ (-45ZXI (TSOP I))			8	$\mu A$
		$V_{CC} = 1.5V$ , $CE_1 \geq V_{CC} - 0.2V$ , $CE_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ (-45BAXI/ -45BVXI/ -45BVI (VFBGA))			10	$\mu A$
$t_{CDR}^{[11]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[12]}$	Operation Recovery Time		$t_{RC}$			ns

## Data Retention Waveform



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC}(\min) \geq 100 \mu s$  or stable at  $V_{CC}(\min) \geq 100 \mu s$ .
- $\overline{BHE.BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range<sup>[14, 15]</sup>

Parameter	Description	45 ns		Unit
		Min	Max	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	45		ns
$t_{AA}$	Address to Data Valid		45	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid		45	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to LOW Z <sup>[16]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[16, 17]</sup>		18	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z <sup>[16]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to High Z <sup>[16, 17]</sup>		18	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Up	0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to Power Down		45	ns
$t_{DBE}$	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		45	ns
$t_{LZBE}$	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z <sup>[16]</sup>	10		ns
$t_{HZBE}$	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HIGH Z <sup>[16, 17]</sup>		18	ns
<b>WRITE CYCLE<sup>[18]</sup></b>				
$t_{WC}$	Write Cycle Time	45		ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End	35		ns
$t_{AW}$	Address Setup to Write End	35		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Setup to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35		ns
$t_{BW}$	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	35		ns
$t_{SD}$	Data Setup to Write End	25		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[16, 17]</sup>		18	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[16]</sup>	10		ns

### Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of  $V_{CC}(typ)/2$ , input pulse levels of 0 to  $V_{CC}(typ)$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in "AC Test Loads and Waveforms" on page 4.
15. AC timing parameters are subject to byte enable signals ( $\overline{BHE}$  or  $\overline{BLE}$ ) not switching when chip is disabled. See application note AN13842 for further clarification.
16. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
17.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

## Switching Waveforms

Figure 3 shows address transition controlled read cycle waveforms.<sup>[19, 20]</sup>

Figure 3. Read Cycle No. 1

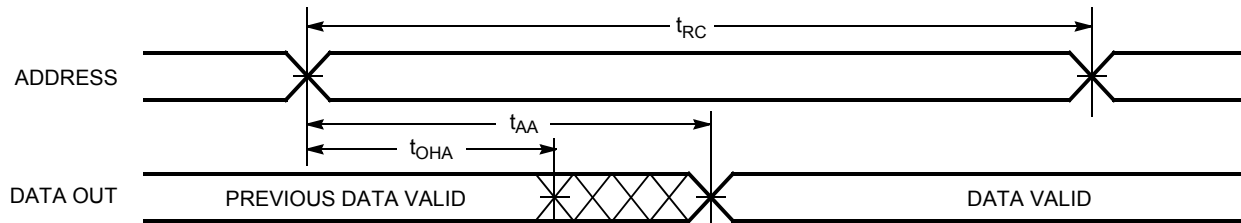
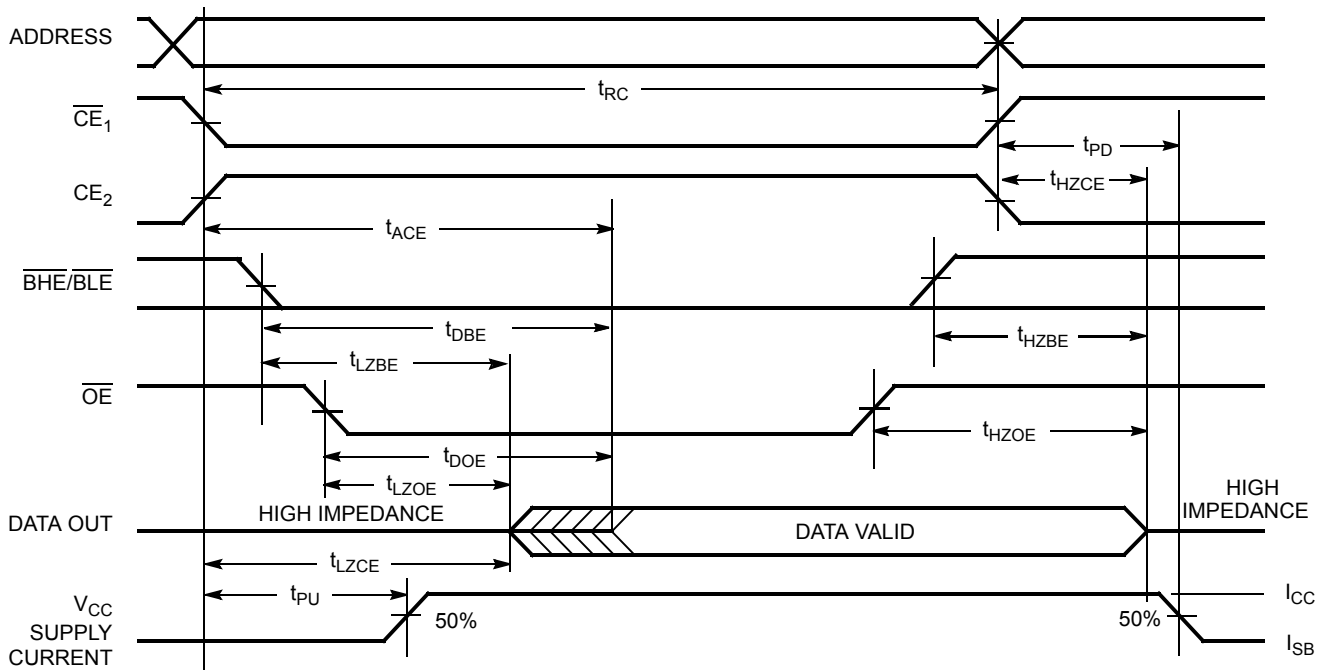


Figure 4 shows  $\overline{OE}$  controlled read cycle waveforms.<sup>[20, 21]</sup>

Figure 4. Read Cycle No. 2



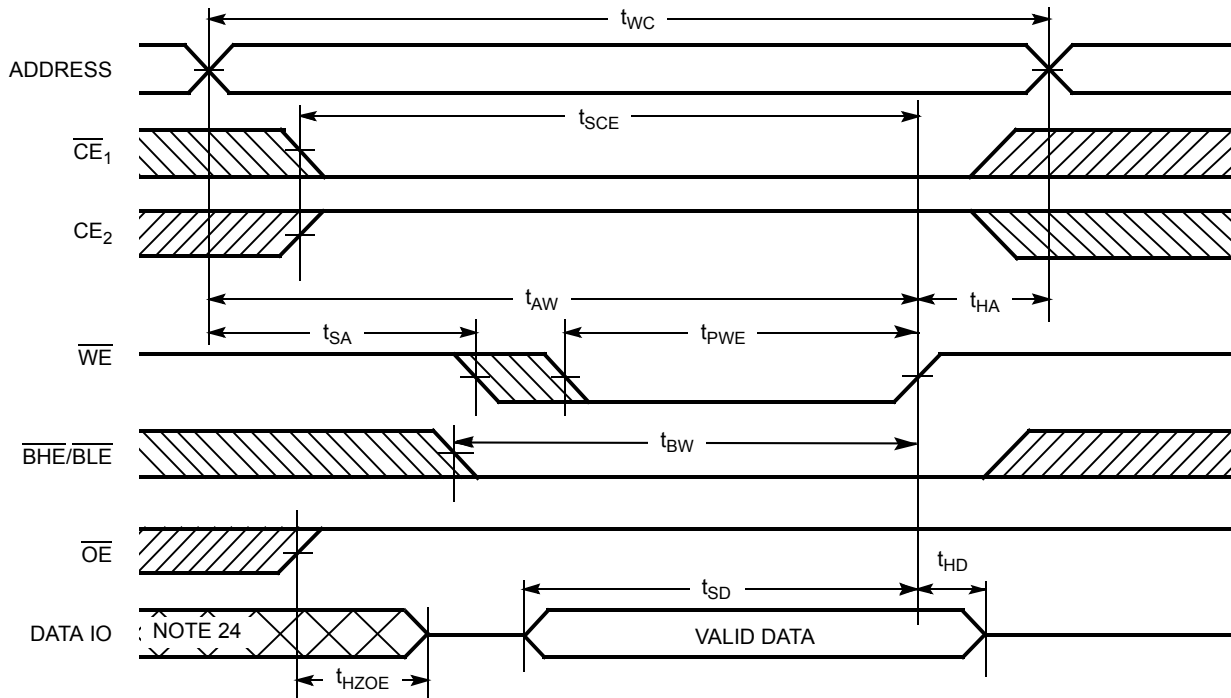
### Notes

19. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ .
20.  $\overline{WE}$  is HIGH for read cycle.
21. Address valid before or similar to  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 5 shows  $\overline{WE}$  controlled write cycle waveforms.<sup>[18, 22, 23]</sup>

Figure 5. Write Cycle No. 1



Notes

- 22. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
- 23. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 24. During this period the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 6 shows  $\overline{CE}_1$  or  $CE_2$  controlled write cycle waveforms.<sup>[18, 22, 23]</sup>

Figure 6. Write Cycle No. 2

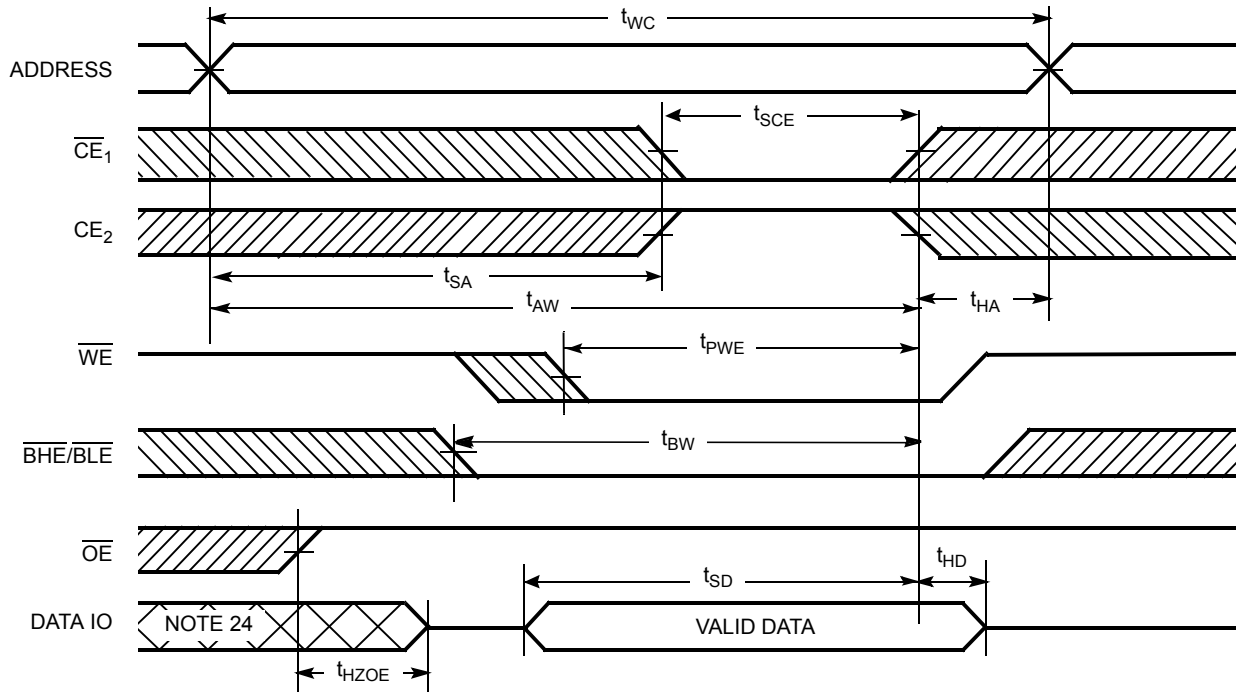
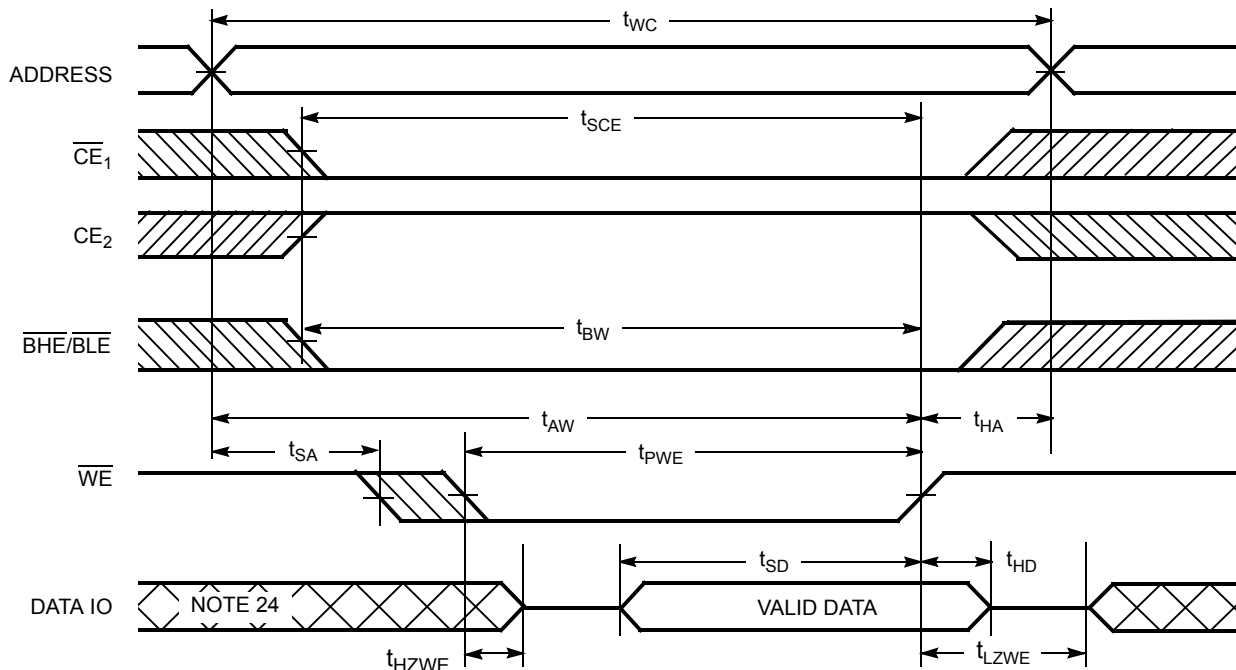


Figure 7 shows  $\overline{WE}$  controlled,  $\overline{OE}$  LOW write cycle waveforms.<sup>[23]</sup>

Figure 7. Write Cycle No. 3

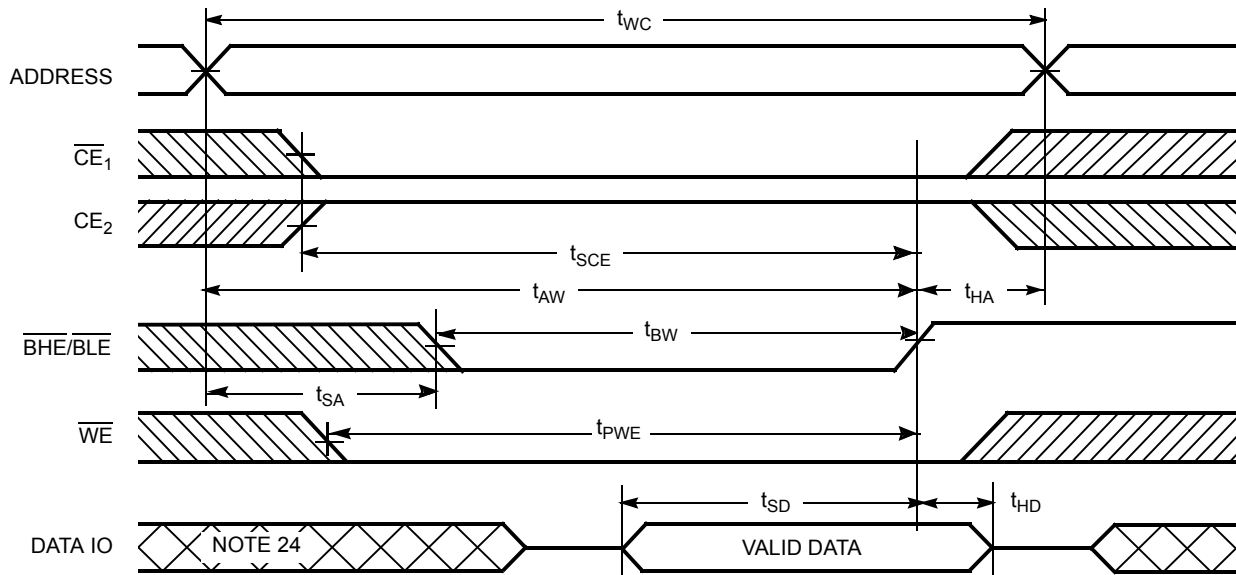




Switching Waveforms (continued)

Figure 8 shows  $\overline{\text{BHE}}/\overline{\text{BLE}}$  controlled,  $\overline{\text{OE}}$  LOW write cycle waveforms.<sup>[23]</sup>

Figure 8. Write Cycle No. 4



Truth Table

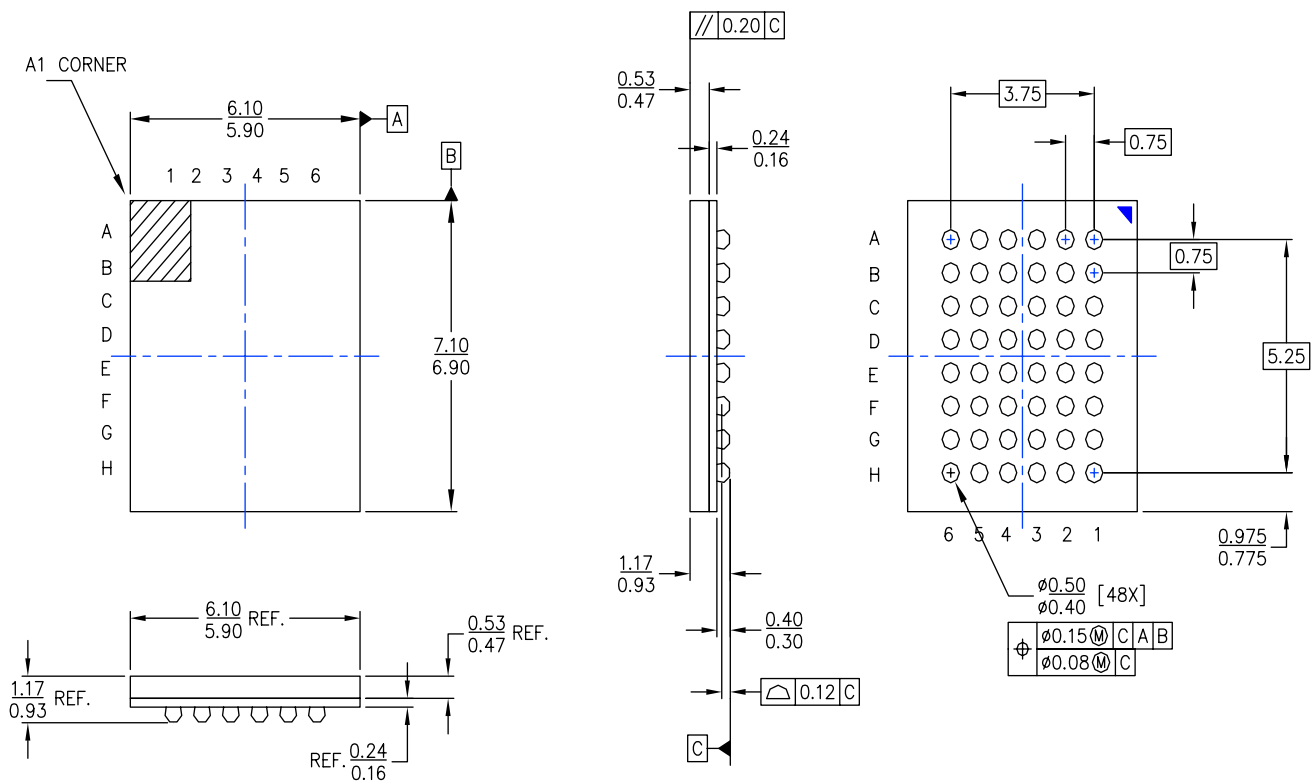
$\overline{\text{CE}}_1$	$\overline{\text{CE}}_2$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect / Power Down	Standby ( $I_{\text{SB}}$ )
X	L	X	X	X	X	High Z	Deselect / Power Down	Standby ( $I_{\text{SB}}$ )
X	X	X	X	H	H	High Z	Deselect / Power Down	Standby ( $I_{\text{SB}}$ )
L	H	H	L	L	L	Data Out ( $\text{IO}_0\text{--}\text{IO}_{15}$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	H	L	H	L	Data Out ( $\text{IO}_0\text{--}\text{IO}_7$ ); High Z ( $\text{IO}_8\text{--}\text{IO}_{15}$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	H	L	L	H	High Z ( $\text{IO}_0\text{--}\text{IO}_7$ ); Data Out ( $\text{IO}_8\text{--}\text{IO}_{15}$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	H	H	L	H	High Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	H	H	H	L	High Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	H	H	L	L	High Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	L	X	L	L	Data In ( $\text{IO}_0\text{--}\text{IO}_{15}$ )	Write	Active ( $I_{\text{CC}}$ )
L	H	L	X	H	L	Data In ( $\text{IO}_0\text{--}\text{IO}_7$ ); High Z ( $\text{IO}_8\text{--}\text{IO}_{15}$ )	Write	Active ( $I_{\text{CC}}$ )
L	H	L	X	L	H	High Z ( $\text{IO}_0\text{--}\text{IO}_7$ ); Data In ( $\text{IO}_8\text{--}\text{IO}_{15}$ )	Write	Active ( $I_{\text{CC}}$ )

### Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167EV30LL-45BAXI	001-13297	48-ball VFBGA (6 x 7 x 1 mm) (Pb-free)	Industrial
	CY62167EV30LL-45BVI	51-85150	48-ball VFBGA (6 x 8 x 1 mm)	
	CY62167EV30LL-45BVXI	51-85150	48-ball VFBGA (6 x 8 x 1 mm) (Pb-free)	
	CY62167EV30LL-45ZXI	51-85183	48-pin TSOP I (Pb-free)	

### Package Diagrams

Figure 9. 48-Ball VFBGA (6 x 7 x 1 mm), 001-13297

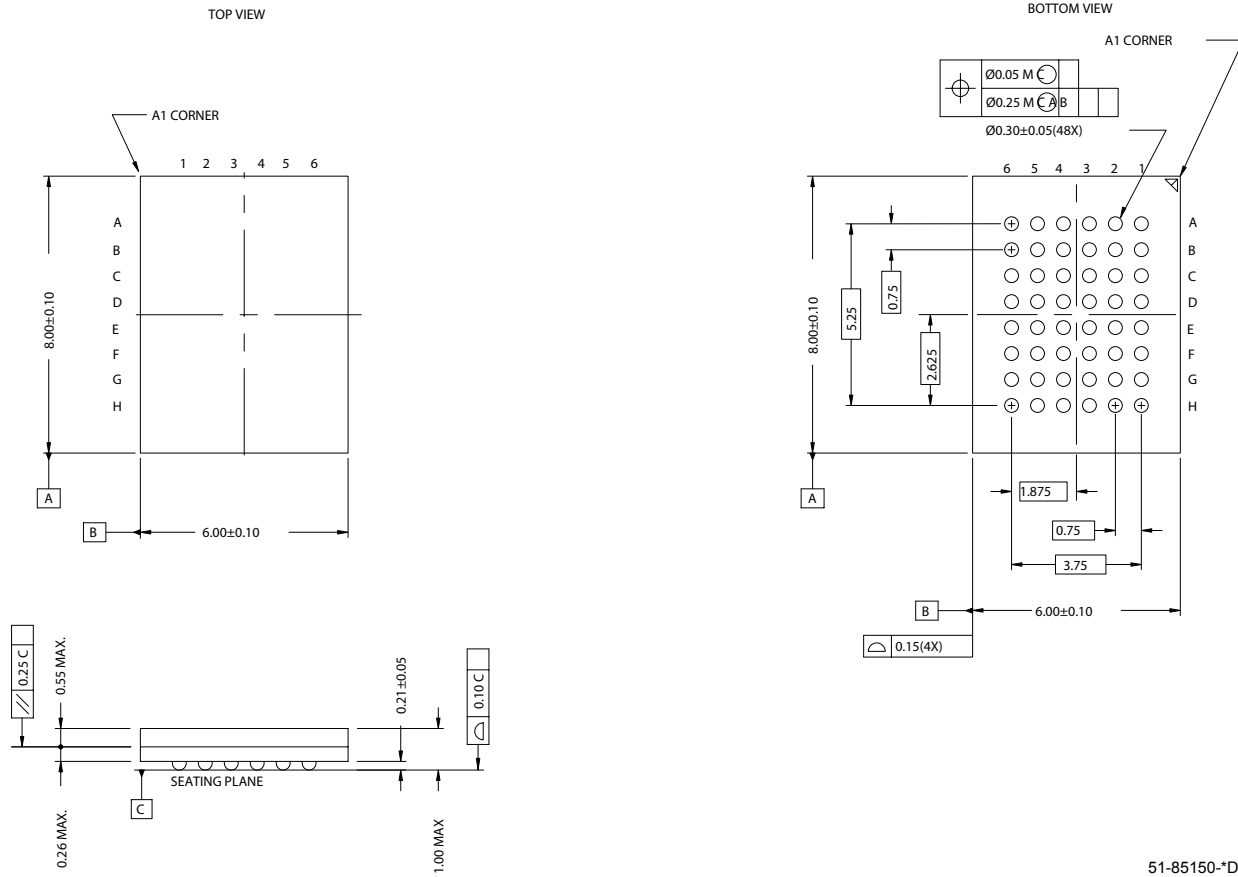


- NOTES:
1. ALL DIMENSION ARE IN MM [MAX/MIN]
  2. JEDEC REFERENCE : MO-216
  3. PACKAGE WEIGHT : 0.03g

001-13297-A

Package Diagrams (continued)

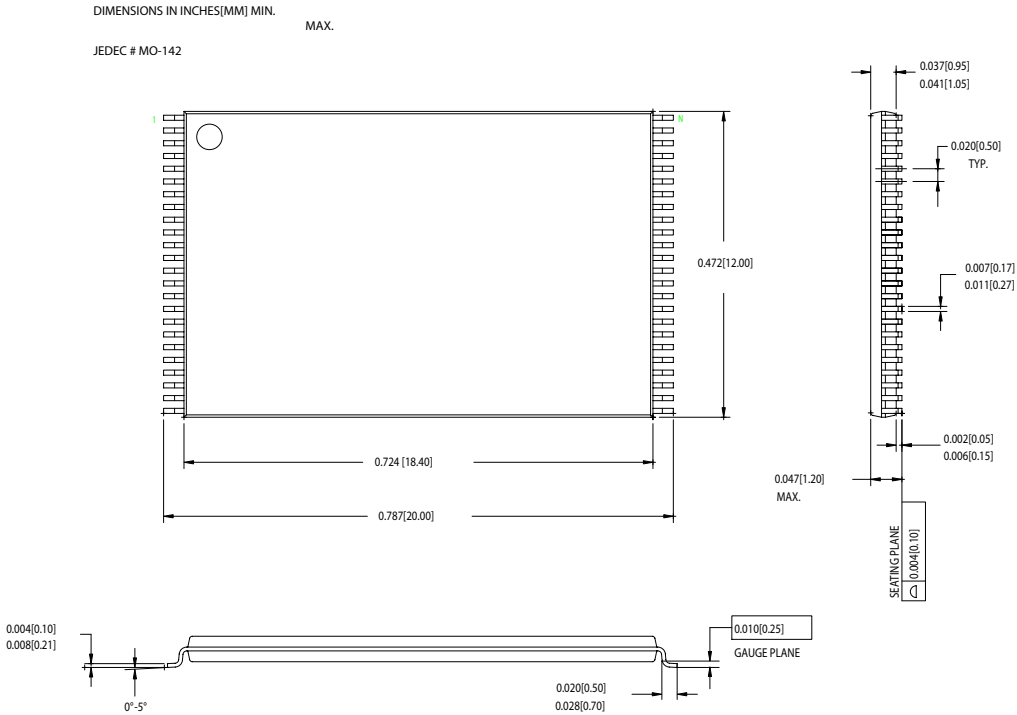
Figure 10. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150



51-85150-\*D

Package Diagrams (continued)

Figure 11. 48-Pin TSOP I (12 mm x 18.4 mm x 1.0 mm), 51-85183



51-85183-\*A

**Document History Page**

Document Title: CY62167EV30 MoBL® 16-Mbit (1M x 16 / 2M x 8) Static RAM				
Document Number: 38-05446				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	202600	01/23/04	AJU	New Data Sheet
*A	463674	See ECN	NXR	Converted from Advance Information to Preliminary Removed 'L' bin and 35 ns speed bin from product offering Modified Data sheet to include x8 configurability. Changed ball E3 in FBGA pinout from DNU to NC Changed the I <sub>SB2(Typ)</sub> value from 1.3 $\mu$ A to 1.5 $\mu$ A Changed the I <sub>CC(Max)</sub> value from 40 mA to 25 mA Changed Vcc stabilization time in footnote #9 from 100 $\mu$ s to 200 $\mu$ s Changed the AC Test Load Capacitance value from 50 pF to 30 pF Corrected typo in Data Retention Characteristics (tr) from 100 $\mu$ s to trc ns Changed t <sub>OHA</sub> , t <sub>LZCE</sub> , t <sub>LZBE</sub> , and t <sub>LZWE</sub> from 6 ns to 10 ns Changed t <sub>LZOE</sub> from 3 ns to 5 ns. Changed t <sub>HZOE</sub> , t <sub>HZCE</sub> , t <sub>HZBE</sub> , and t <sub>HZWE</sub> from 15 ns to 18 ns Changed t <sub>SCE</sub> , t <sub>AW</sub> , and t <sub>BW</sub> from 40 ns to 35 ns Changed t <sub>PE</sub> from 30 ns to 35 ns Changed t <sub>SD</sub> from 20 ns to 25 ns Updated 48 ball FBGA Package Information. Updated the Ordering Information table
*B	469169	See ECN	NSI	Minor Change: Moved to external web
*C	1130323	See ECN	VKN	Converted from preliminary to final Changed I <sub>CC</sub> max spec from 2.8 mA to 4.0 mA for f=1MHz Changed I <sub>CC</sub> typ spec from 22 mA to 25 mA for f=f <sub>max</sub> Changed I <sub>CC</sub> max spec from 25 mA to 30 mA for f=f <sub>max</sub> Added V <sub>IL</sub> spec for TSOP I package and footnote# 9 Added footnote# 10 related to I <sub>SB2</sub> and I <sub>CCDR</sub> Changed I <sub>SB1</sub> and I <sub>SB2</sub> spec from 8.5 $\mu$ A to 12 $\mu$ A Changed I <sub>CCDR</sub> spec from 8 $\mu$ A to 10 $\mu$ A Added footnote# 15 related to AC timing parameters
*D	1323984	See ECN	VKN/AESA	Modified I <sub>CCDR</sub> spec for TSOP I package Added 48-Ball VFBGA (6 x 7 x 1mm) package Added footnote# 1 related to VFBGA (6 x 7 x 1mm) package Updated Ordering Information table

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