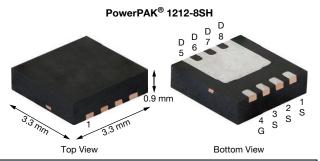
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RoHS

P-Channel 30 V (D-S) MOSFET



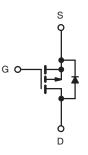
PRODUCT SUMMARY					
V _{DS} (V)	-30				
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.014				
$R_{DS(on)}$ max. (Ω) at V_GS = -4.5 V	0.0251				
Q _g typ. (nC)	13.1				
I _D (A) ^d	-34.4				
Configuration	Single				

FEATURES

- TrenchFET[®] power MOSFET
- 100 % R_g and UIS tested
- Material categorization: COMPLIANT For definitions of compliance please see HALOGEN WWW.vishay.com/doc?99912

APPLICATIONS

- Notebook adapter switch
- Notebook battery management
- Load switch



P-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH107DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T	$_{A} = 25 \ ^{\circ}C$, unless o	therwise noted))		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	-30	V	
Gate-source voltage		V _{GS}	± 25	- v	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		-34.4		
	T _C = 70 °C		-27.5		
	T _A = 25 °C	I _D	-12.6 ^{a, b}		
	T _A = 70 °C	1	-10.1 ^{a, b}	•	
Pulsed drain current (t = 300 µs)	I _{DM}	-100	— A		
Continuous source-drain diode current	T _C = 25 °C		-22.1 ^d		
	T _A = 25 °C	I _S	-2.9 ^{a, b}		
Avalanche current		I _{AS}	-15		
Single-pulse avalanche energy	L = 0.1 mH	E _{AS}	11.2	mJ	
Maximum power dissipation	T _C = 25 °C		26.5		
	T _C = 70 °C		17.0	w	
	T _A = 25 °C	P _D	3.57 ^{a, b}	vv	
	T _A = 70 °C	1	2.28 ^{a, b}		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	*0	
Soldering recommendations (peak temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient a, c	t ≤ 10 s	R _{thJA}	28	35	°C/W	
Maximum junction-to-case	Steady state	R _{thJC}	3.8	4.7		

Notes

a. Surface mounted on 1" x 1" FR4 board

b. t = 10 s

c. Maximum under steady state conditions is 81 °C/W

d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

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SiSH107DN

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static	•		•	•		•	
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = -250 \mu\text{A}$	-30	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = -250 μΑ	-	-20	-	mV/°C	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	2.5	-		
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \ \mu A$	-1.0	-	-2.5	V	
Gate-source leakage	I _{GSS}	V_{DS} = 0 V, V_{GS} = ± 25 V	-	-	± 100	nA	
Zara gata valtaga duain avuvant		$V_{DS} = -30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	-1	μA	
Zero gate voltage drain current	I _{DSS}	V_{DS} = -30 V, V_{GS} = 0 V, T_{J} = 55 °C	-	-	-5	μΑ	
Drain source on state resistance a	Passa	$V_{GS} = -10 \text{ V}, \text{ I}_{D} = -10 \text{ A}$	-	0.011	0.014	Ω	
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -10 \text{ A}$	-	0.019	0.0251		
Forward transconductance ^a	9 _{fs}	$V_{DS} = -0 V, I_{D} = -10 A$	-	28	-	S	
Dynamic ^b							
Input capacitance	C _{iss}		-	1400	-	pF	
Output capacitance	C _{oss}	V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz	-	208	-		
Reverse transfer capacitance	C _{rss}		-	182	-		
Tatal asta abarra	0	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}$ $V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -10 \text{ A}$	-	27.2	41	nC	
Total gate charge	Qg		-	13.1	20		
Gate-source charge	Q _{gs}		-	4.6	-		
Gate-drain charge	Q _{gd}		-	4.9	-		
Gate resistance	R _g	f = 1 MHz	2.3	4.7	8	Ω	
Turn-on delay time	t _{d(on)}		-	10	20		
Rise time	tr	V_{DD} = -15 V, R_{L} = 1.5 Ω	-	5	10		
Turn-off delay time	t _{d(off)}	$I_D \cong$ -10 A, V_{GEN} = -10 V, R_g = 1 Ω	-	27	54		
Fall time	t _f		-	7	14		
Turn-on delay time	t _{d(on)}		-	20	40	ns	
Rise time	t _r	V_{DD} = -15 V, R_L = 1.5 Ω	-	70	140		
Turn-off delay time	t _{d(off)}	$I_D\cong$ -10 A, V_{GEN} = -4.5 V, R_g = 1 Ω	-	23	46		
Fall time	t _f		-	15	30		
Drain-Source Body Diode Characteris	tics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-22.1	^	
Pulse diode forward current	I _{SM}		-	-	-100	A	
Body diode voltage	V _{SD}	$I_{\rm S} = -3$ A, $V_{\rm GS} = 0$ V	-	-0.79	-1.2	V	
Body diode reverse recovery time	t _{rr}		-	11	22	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = -10 A, di/dt = 100 A/μs,	-	4	8	nC	
Reverse recovery fall time	t _a	T _J = 25 °C	-	6	-		
Reverse recovery rise time	t _b		-	5	-	ns	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing

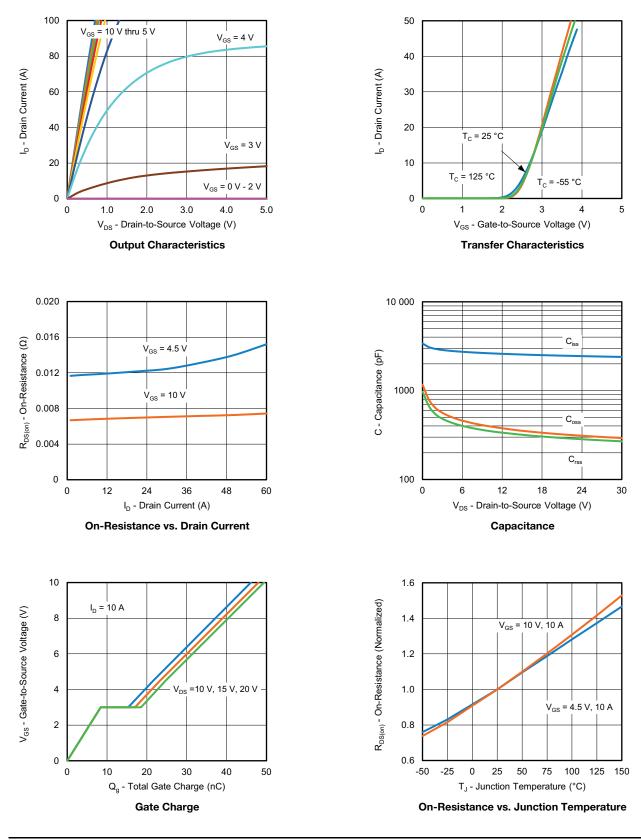
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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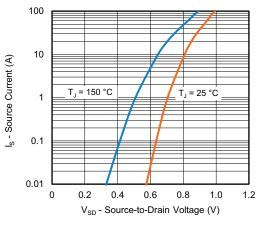
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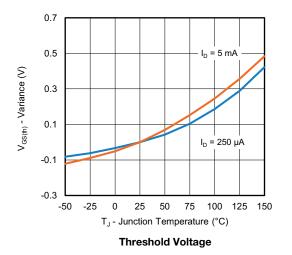


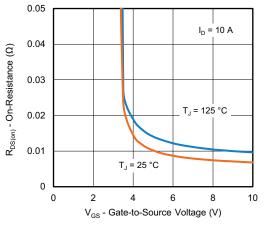
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

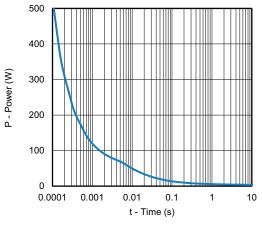


Source-Drain Diode Forward Voltage

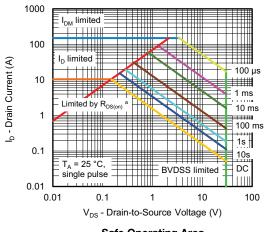




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area

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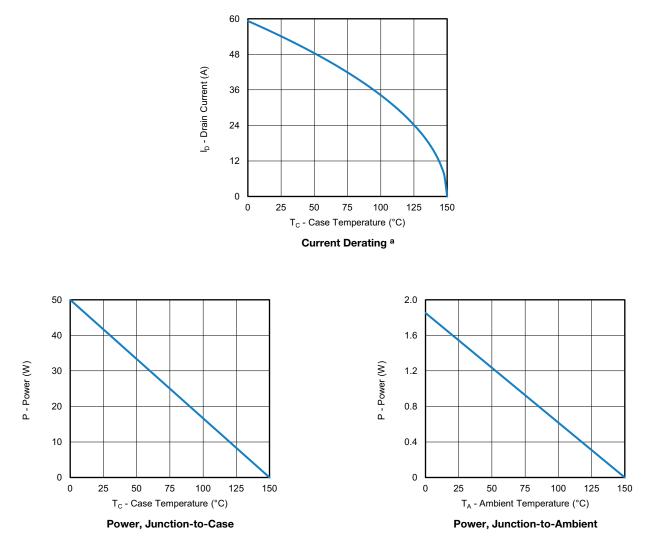
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MOSFET TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



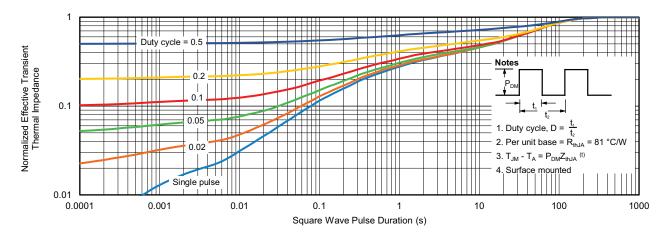
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

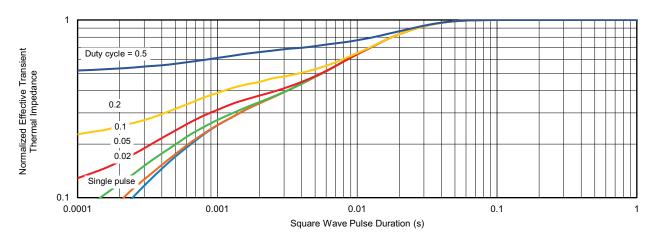


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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