MRF24J40MD/ME

2.4 GHz IEEE Std. 802.15.4™ RF Transceiver Module with PA/LNA

Features:

- IEEE Std. 802.15.4™ Compliant RF Transceiver
- Supports ZigBee®, MiWi™ Development Environment Proprietary Wireless Networking Protocols
- 4-Wire Serial Peripheral Interface (SPI) with Interrupt
- Small size: 0.9" x 1.3" (22.9 mm x 33.0 mm), Surface Mountable: Pin Compatible with MRF24J40MB and MRF24J40MC
- Integrated Crystal, Internal Voltage Regulator, Matching Circuitry, Power Amplifier, Low Noise Amplifier
- PCB Antenna (MRF24J40MD), External Antenna Connector (MRF24J40ME): Ultra Miniature Coaxial (U.FL), 50Ω
- Easy Integration into Final Product: Minimize Product Development, Quicker Time to Market
- Compliance:
  - Modular Certified for the United States (FCC) and Canada (IC)
  - European R&TTE Directive Assessed Radio Module
  - Australia/New Zealand
- Compatible with Microchip microcontroller families (PIC16, PIC18, PIC24, dsPIC33 and PIC32)
- Range up to 4000 ft

Operational:

- Operating Voltage: 3.0V-3.6V (3.3V typical)
- Temperature Range: -40°C to +85°C Industrial
- Low-Current Consumption:
  - Rx Mode: 32 mA (typical)
  - Tx Mode: 140 mA (typical)
  - Sleep: 10 μA (typical)

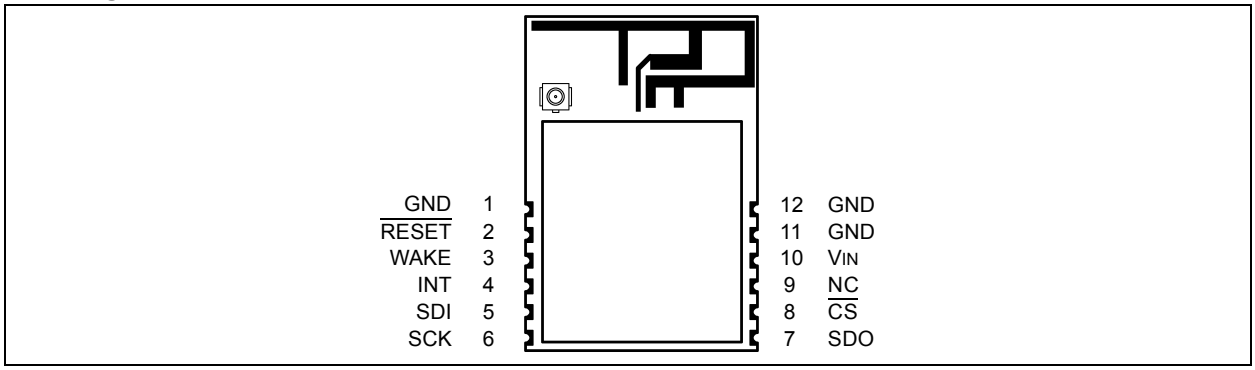
RF/Analog Features:

- ISM Band 2.405 GHz-2.475 GHz Operation
- Data Rate: 250 kbps
- -104 dBm Typical Sensitivity with -23 dBm Maximum Input Level
- +19 dBm Typical Output Power with 45 dB Tx Power Control Range
- Integrated Low Phase Noise VCO, Frequency Synthesizer and PLL Loop Filter
- Digital VCO and Filter Calibration
- Integrated RSSI ADC and I/Q DACs
- Integrated LDO
- High Receiver RSSI Dynamic Range

MAC/Baseband Features:

- Hardware CSMA-CA Mechanism, Automatic ACK Response and FCS Check
- Independent Beacon, Transmit and GTS FIFO
- Supports all CCA modes and RSS/LQI
- Automatic Packet Retransmit Capable
- Hardware Security Engine (AES-128) with CTR, CCM and CBC-MAC modes
- Supports Encryption and Decryption for MAC Sub layer and Upper Layer

Pin Diagram:



1.0 DEVICE OVERVIEW

The MRF24J40MD/ME is a 2.4 GHz IEEE Std. 802.15.4™ compliant, surface mount module with integrated crystal, internal voltage regulator, matching circuitry, Power Amplifier (PA), Low Noise Amplifier (LNA) with PCB Trace Antenna (MRF24J40MD) or 50Ω external antenna connector (MRF24J40ME). The MRF24J40MD/ME module operates in the non-licensed 2.4 GHz frequency band. The integrated module design frees the integrator from extensive RF and antenna design, and regulatory compliance testing allowing quicker time to market.

The MRF24J40MD/ME module is compatible with Microchip's MiWi™ Development Environment software stacks. The MiWi Development Environment software stack including the source code is available as a free download, from the Microchip web site: http://www.microchip.com/wireless.

The MRF24J40MD/ME module has received regulatory approvals for modular devices in the United States (FCC) and Canada (IC). Modular approval removes the need for expensive RF and antenna design, and allows the end user to place the MRF24J40MD/ME module inside a finished product and does not require regulatory testing for an intentional radiator (RF transmitter). To maintain conformance, refer to module settings in **Section 3.1.2 "RF Exposure"** for the United States and **Section "Transmitter Antenna (from Section 7.1.2 RSS-Gen, Issue 3, December 2010): User manuals for transmitters shall display the following notice in a conspicuous location:"** for Canada.

The MRF24J40MD/ME module is an R&TTE Directive assessed radio module for operation in Europe. The module tests can be applied toward final product certification and Declaration of Conformity (DoC). To maintain conformance for Europe, refer to module settings in **Section 3.4 "Australia"**. Additional testing may be required depending on the end application.

1.1 Interface Description

Figure 1-1 shows a simplified block diagram of the MRF24J40MD/ME module. The module is based on the Microchip Technology MRF24J40 IEEE 802.15.4™ 2.4 GHz RF Transceiver IC. The module interfaces to many popular Microchip PIC® microcontrollers through a 4-wire SPI interface, interrupt, wake, reset, power and ground, as shown in Figure 1-2. Table 1-1 provides the pin descriptions.

Serial communication and module configuration for the MRF24J40MD/ME module are documented in the *"MRF24J40 Data Sheet"* (DS39776). Refer to the data sheet for specific serial interface protocol and register definitions.

Also, see **Section 1.4 "Operation"** for specific register settings that are unique to the MRF24J40MD/ME module.

FIGURE 1-1: MRF24J40MD/ME BLOCK DIAGRAM

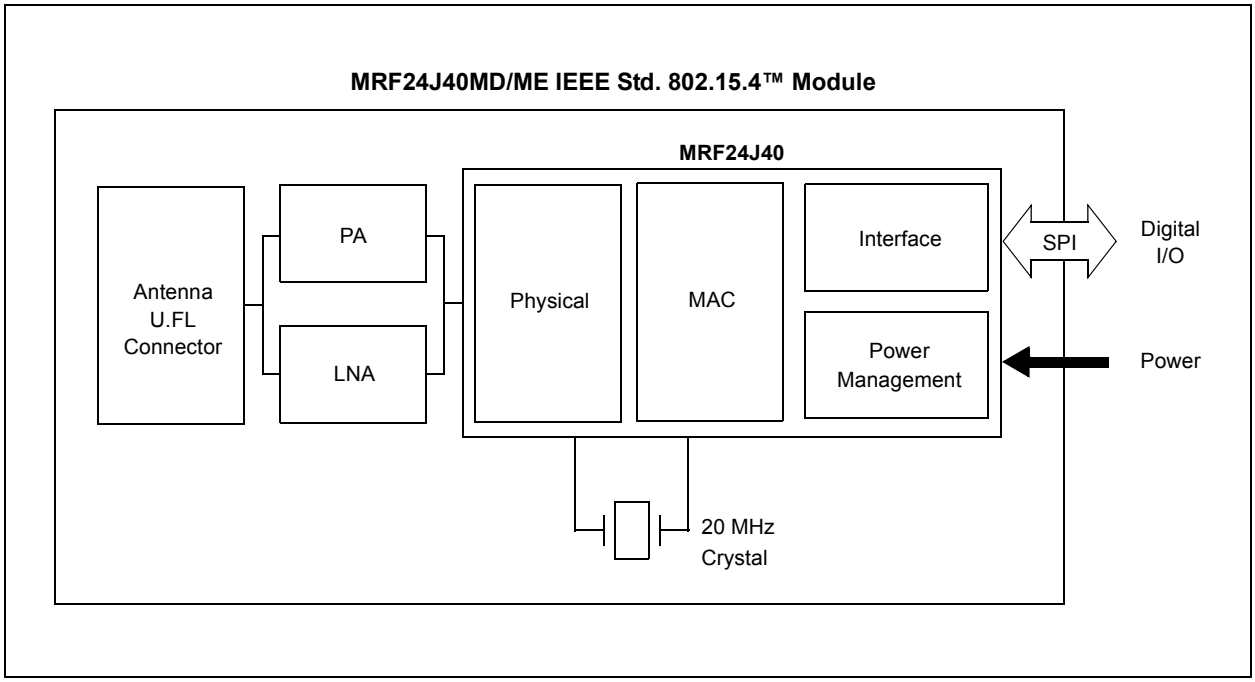
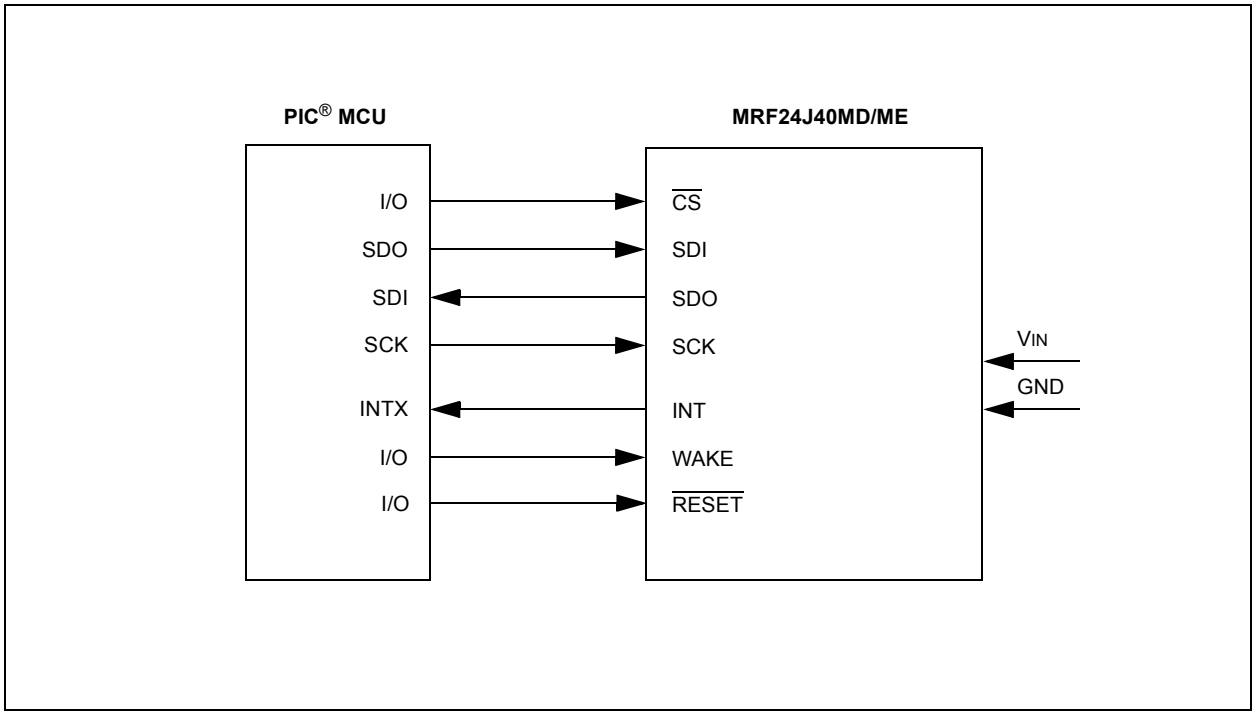


TABLE 1-1: PIN DESCRIPTION

Pin	Symbol	Type	Description
1	GND	Ground	Ground
2	$\overline{\text{RESET}}$	DI	Global hardware Reset pin
3	WAKE	DI	External wake-up trigger
4	INT	DO	Interrupt pin to microcontroller
5	SDI	DI	Serial interface data input
6	SCK	DI	Serial interface clock
7	SDO	DO	Serial interface data output from MRF24J40
8	$\overline{\text{CS}}$	DI	Serial interface enable
9	NC	—	No connection
10	VIN	Power	Power supply
11	GND	Ground	Ground
12	GND	Ground	Ground

Legend: Pin type abbreviation: D = Digital, I = Input, O = Output

FIGURE 1-2: MICROCONTROLLER TO MRF24J40MD/ME INTERFACE



1.2 Mounting Details

The MRF24J40MD/ME is a surface mountable module. Module dimensions are shown in Figure 1-3. The module Printed Circuit Board (PCB) is 0.032" thick with castellated mounting points on the edge. Figure 1-4 is a recommended host PCB footprint for the MRF24J40MD/ME.

The MRF24J40MD has an integrated PCB antenna. For the best performance, follow the mounting details shown in Figure 1-5. It is recommended that the module be mounted on the edge of the host PCB, and an area around the antenna, approximately 1.2", be kept clear of metal objects. A host PCB ground plane around the MRF24J40MD acts as a counterpoise to the PCB antenna. It is recommended to extend the ground plane at least 0.4" around the module.

The MRF24J40ME has 50Ω ultra miniature coaxial (U.FL) connector.

Caution: The U.FL connector is fragile and can only tolerate very limited number of insertions.

1.3 Soldering Recommendations

The MRF24J40MD/ME module was assembled using a standard lead-free reflow profile. The module is compatible with standard lead-free solder reflow profiles. To avoid damaging the module, the following recommendations are given:

- Refer to the solder paste data sheet for specific reflow profile recommendations
- Use no-clean flux solder paste
- Do not wash as moisture can be trapped under the shield
- Use only one flow. If the PCB requires multiple flows, apply the module on the last flow

FIGURE 1-3: MODULE DETAILS

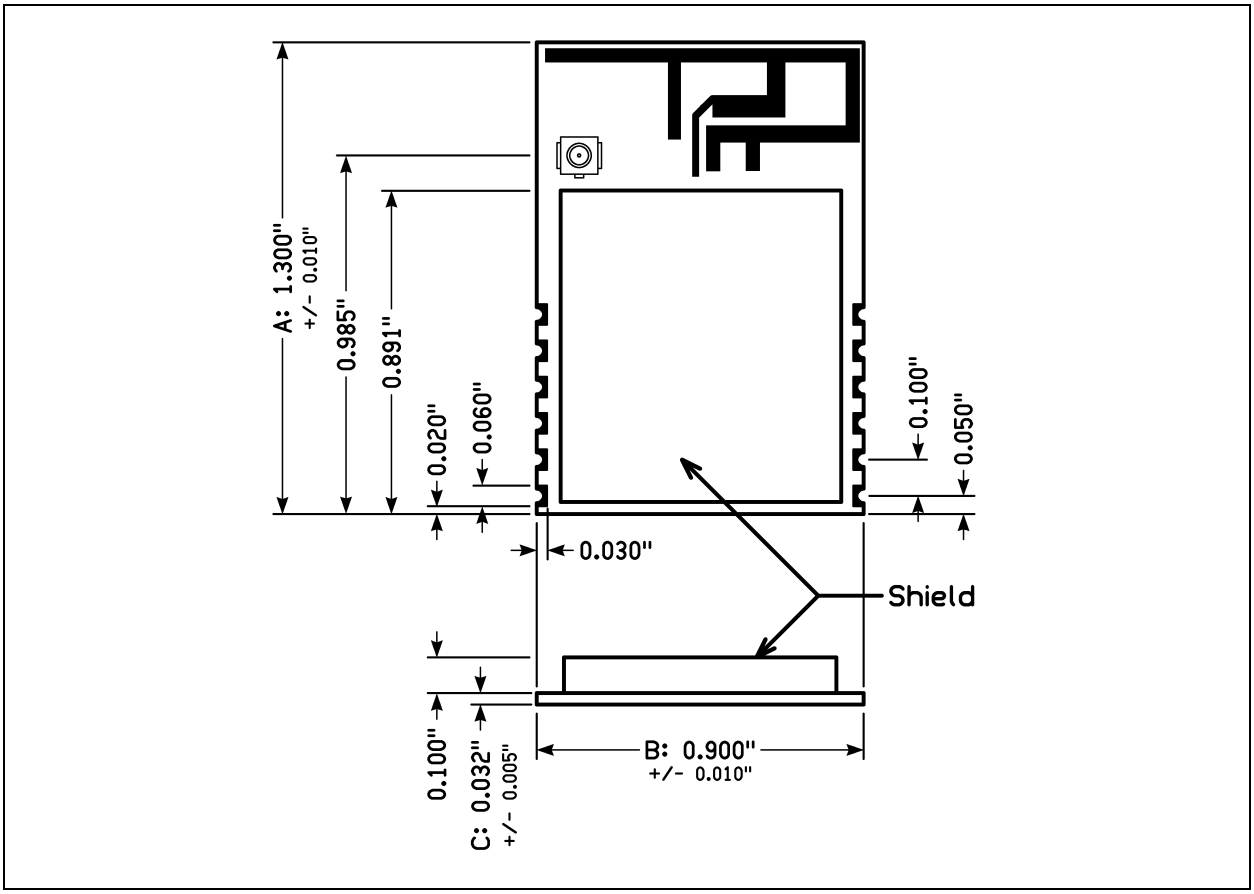


FIGURE 1-4: RECOMMENDED PCB FOOTPRINT

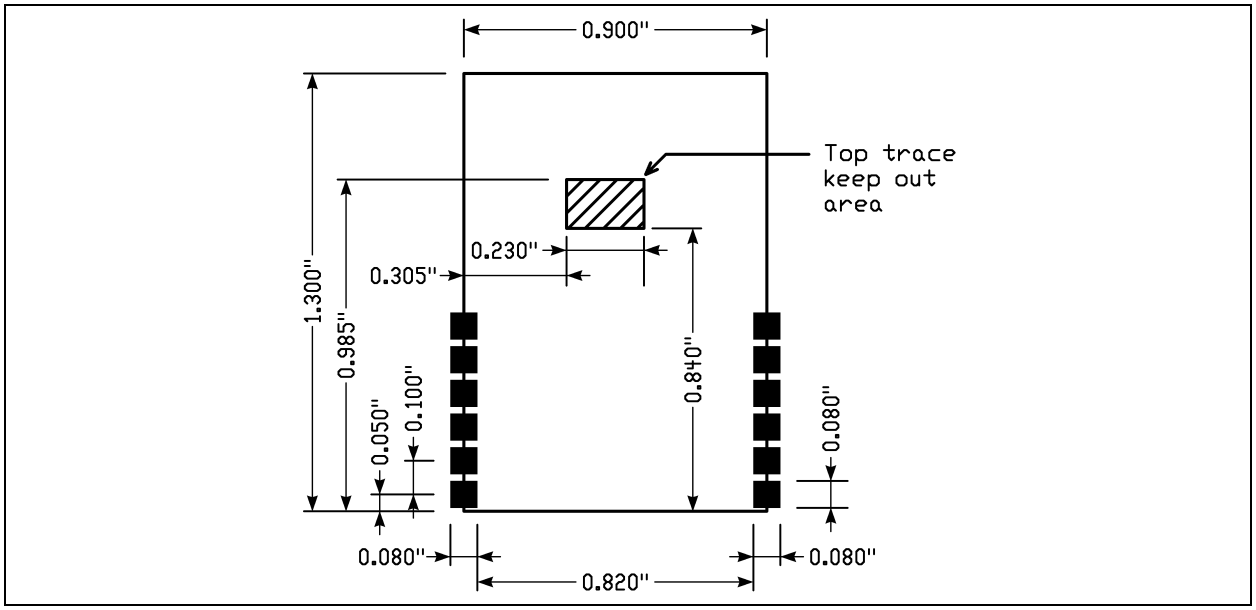
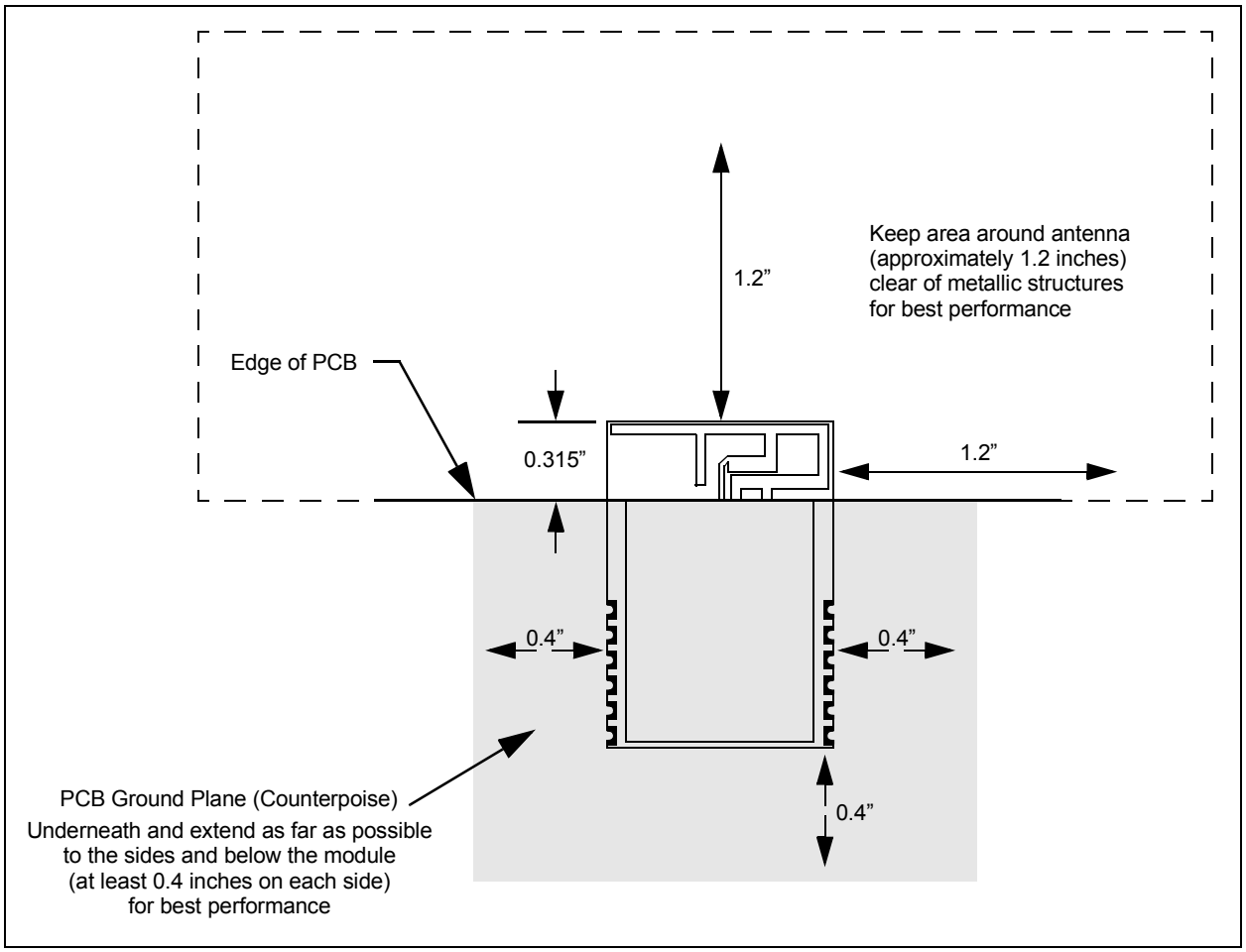


FIGURE 1-5: MOUNTING DETAILS



1.4 Operation

The MRF24J40MD/ME module is based on the Microchip Technology MRF24J40 2.4 GHz IEEE 802.15.4 RF Transceiver IC. Serial communication and configuration are documented in the "*MRF24J40 Data Sheet*" (DS39776).

This section emphasizes operational settings that are unique to the MRF24J40MD/ME module design that must be followed for proper operation.

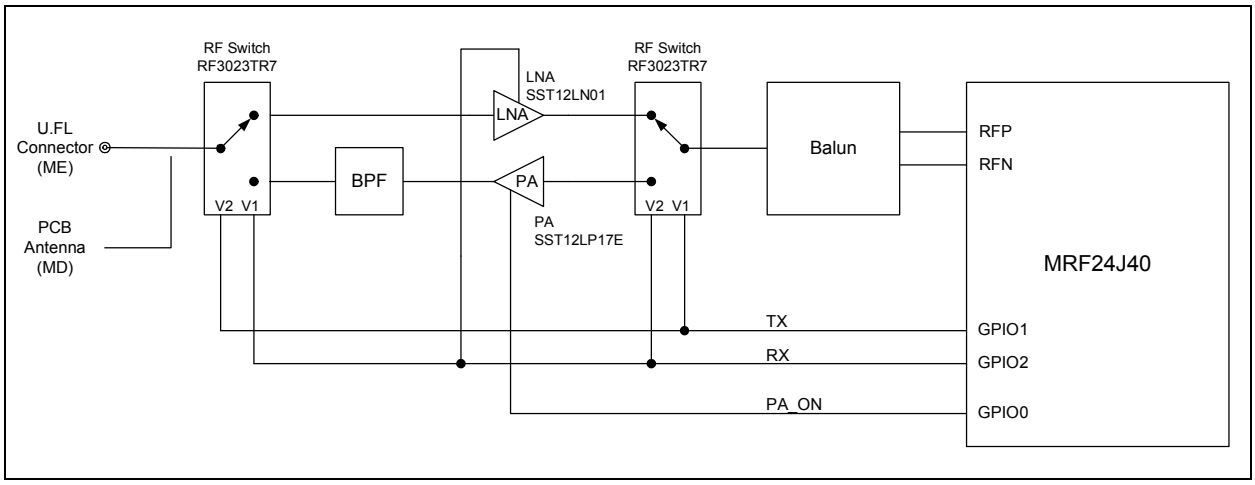
1.4.1 PA/LNA CONTROL

Operation of the PA U6 and LNA U1 is controlled by the MRF24J40 internal RF state machine through RF switches, U3 and U4, and the GPIO0, GPIO1 and GPIO2 pins on the MRF24J40. Figure 1-6 shows the PA/LNA block diagram. Figure 2-5 is the schematic diagram for the module.

The internal RF state machine is configured for the PA/LNA Mode by setting TESTMODE (0x22<2:0>) = `111`. Pins GPIO0, GPIO1 and GPIO2 control the RF switches, PA and LNA automatically when the MRF24J40 receives and transmits data.

Note:	A complete explanation of the operation of the PA/LNA control is documented in the *"MRF24J40 Data Sheet"* (DS39776), Section 4.2 "External PA/LNA Control".

FIGURE 1-6: PA/LNA BLOCK DIAGRAM



1.4.2 ENERGY DETECTION (ED)

Before performing an energy detection (see Section 3.6.1 “RSSI Firmware Request (RSSI Mode 1)” in the *“MRF24J40 Data Sheet”* (DS39776), perform the following steps:

1. Configure the internal RF state machine to normal operation (TESTMODE (0x22F<2:0>) = 000).
2. Configure GPIO2 and GPIO1 direction for output (TRISGP2 (0x34<2>) = 1 and TRISGP1 (0x34<1>) = 1).
3. Set GPIO2 (0x33<2>) = 1 and GPIO1 (0x32<1>) = 0. This enables the LNA and disables the PA.
4. Perform the energy detection following the steps in Section 3.6.1 “RSSI Firmware Request (RSSI Mode 1)” in the *“MRF24J40 Data Sheet”* (DS39776).

Note:	The LNA will amplify the received signal. The RSSI value will include the receive signal strength plus the LNA amplification.

1.4.3 SLEEP

To get the lowest power consumption from the MRF24J40MD/ME module during Sleep, it is necessary to disable the PA, PA voltage regulator and LNA. To do this, perform the following steps:

1. Configure the internal RF state machine to normal operation (TESTMODE (0x22F<2:0>) = 000).
2. Configure the GPIO2, GPIO1 and GPIO0 direction for output (TRISGP2 (0x34<2>) = 1, TRISGP1 (0x34<1>) = 1) = 1 and TRISGP0 (0x34<0>) = 1).
3. Set GPIO2 (0x33<2>) = 0 and GPIO1 (0x32<1>) = 0. This disables the LNA and the PA.
4. Put the MRF24J40 to Sleep following the steps in the *“MRF24J40 Data Sheet”* (DS39776).

When waking the module, re-enable the PA/LNA Mode.