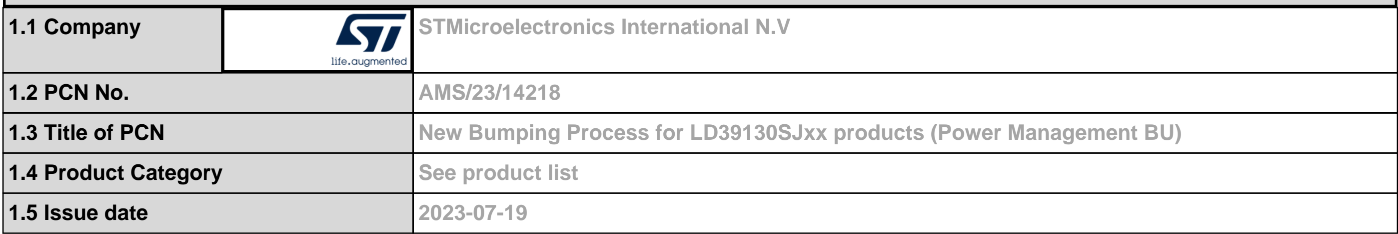
**PRODUCT / PROCESS CHANGE NOTIFICATION**



| 1. PCN basic data | |
|---|---|
| 1.1 Company | STMicroelectronics International N.V |
| 1.2 PCN No. | AMS/23/14218 |
| 1.3 Title of PCN | New Bumping Process for LD39130SJxx products (Power Management BU) |
| 1.4 Product Category | See product list |
| 1.5 Issue date | 2023-07-19 |

| 2. PCN Team | |
|---|---|
| **2.1 Contact supplier** | |
| 2.1.1 Name | Robert Goodman |
| 2.1.2 Phone | +1 6024856271 |
| 2.1.3 Email | robert.goodman@st.com |
| **2.2 Change responsibility** | |
| 2.2.1 Product Manager | Marcello SAN BIAGIO |
| 2.1.2 Marketing Manager | Salvatore DI VINCENZO |
| 2.1.3 Quality Manager | Giuseppe LISI |

| 3. Change | | |
|---|---|---|
| **3.1 Category** | **3.2 Type of change** | **3.3 Manufacturing Location** |
| Transfer | Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Wafer fabrication | SCS (Stats Chippac Singapore) |

| 4. Description of change | | |
|---|---|---|
| | **Old** | **New** |
| 4.1 Description | Printing Bumping Process \| ASE, Taiwan | Ball Drop Bumping Process \| SCS (Stats Chippac Singapore) |
| 4.2 Anticipated Impact on form,fit, function, quality, reliability or processability? | No impact on the Electrical, Mechanical, Quality and Reliability Characteristics. | |

| 5. Reason / motivation for change | |
|---|---|
| 5.1 Motivation | Following ASE communication about the termination of the current Printing Bumping Process, by DEC 2022, the Power Management BU plans to qualify and implement a New Bumping Process for LDO Devices. The new Bumping process will be implemented in SCS (Stats Chippac Singapore) OSAT. No change to the Package Outline Assembly (mechanical) and electrical characteristics (datasheet). No other change is made with respect to this PCN. Wafer diffusion as well as Testing & Finishing/ DPS remain unchanged both in terms of flow and location |
| 5.2 Customer Benefit | SERVICE CONTINUITY |

| 6. Marking of parts / traceability of change | |
|---|---|
| 6.1 Description | The traceability of the new parts will be ensured by physical Die Level and Lot Level codification. |

| 7. Timing / schedule | |
|---|---|
| 7.1 Date of qualification results | 2023-07-12 |
| 7.2 Intended start of delivery | 2023-10-30 |
| 7.3 Qualification sample available? | Upon Request |

| 8. Qualification / Validation | | | |
|---|---|---|---|
| 8.1 Description | 14218 13522 RER 1705W2022 LD39130SJ18R LD39130SJ33R WLCSP STS rev1.pdf | | |
| 8.2 Qualification report and qualification results | Available (see attachment) | Issue Date | 2023-07-19 |

| 9. Attachments (additional documentations) |
|---|
| 14218 Public product.pdf<br>14218 13522 RER 1705W2022 LD39130SJ18R LD39130SJ33R WLCSP STS rev1.pdf |

| 10. Affected parts | | |
|---|---|---|
| 10. 1 Current | | 10.2 New (if applicable) |
| 10.1.1 Customer Part No | 10.1.2 Supplier Part No | 10.1.2 Supplier Part No |
| | LD39130SJ10R | |
| | LD39130SJ12R | |
| | LD39130SJ25R | |
| | LD39130SJ29R | |
| | LD39130SJ30R | |
| | LD39130SJ41R | |

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# Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

***PCN Title :*** New Bumping Process for LD39130SJxx products (Power Management BU)

***PCN Reference :*** AMS/23/14218

***Subject :*** Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

| | | |
|---|---|---|
| LD39130SJ10R | LD39130SJ30R | LD39130SJ41R |
| LD39130SJ12R | LD39130SJ29R | LD39130SJ25R |

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# Reliability Evaluation Report

LD39130SJ18R, LD39130SJ33R
New Bumping Process SCS

| General Information | |
|---|---|
| Product Line | UAD601, UAP101 |
| P/N | LD39130SJ33R, LD39130SJ18R |
| Product Division | AMS |
| Package | Ultra-small CSP 4 |
| Silicon Process Technology | BCD8SP |

| Location | |
|---|---|
| Wafer Fab | AR2F-Agrate R2 |
| Assembly plant | SCS - Stats Chippac Singapore |
| **Results** | |
| Reliability Assessment | PASS |

## DOCUMENT INFORMATION

| Version | Date | Pages | Prepared by | Approved by | Comment |
|---|---|---|---|---|---|
| 1.0 | 5/11/2022 | 4 | Ivan Grasso | Giuseppe Lisi | |

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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# 1 APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description |
|---|---|
| JESD47 | Stress-Test-Driven Qualification of Integrated Circuits |
| 062-0101 Rev AD | General Qualification Procedure For Integrated Circuits |

# 2 GLOSSARY

| | Short description |
|---|---|
| Tj | Temperature at junction of the device |
| $T_A$ | Temperature of ambient air |
| RH | Relative Humidity |
| Vcc max | Max Operative Voltage |

# 3 RELIABILITY EVALUATION OVERVIEW

## 3.1 Objectives

This document is intended to provide reliability plan for LD39130SJ18R and LD39130SJ33R in BCD8 process technology, a very low quiescent current linear regulator IC in Ultra small CSP 4 at SCS - Stats Chippac Singapore.

## 3.2 Conclusion

Qualification requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). The stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

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# 4 TESTS RESULTS SUMMARY

ST refers to the JEDEC standard JESD47 when conducting reliability tests for the qualification of new product.

## 4.1 Test plan and results summary

Table 1. Package qualification tests

| Stress (Abbv.) | Ref. | Conditions | Requirements | | | | Notes |
|---|---|---|---|---|---|---|---|
| | | | # Lot | SS | Duration | Pass Criteria (Fails / Tested) | |
| MSL Preconditioning Must be performed prior to: THB, HAST, TC, AC, & UHAST | JESD22 A113 J-STD-020 | Preconditioning: (Test @ Rm) SMD only; Moisture Preconditioning for THB/HAST, AC/UHST, TC, & PTC; Peak Reflow Temp = 260C | MSL1 | | | | |
| High Temperature Storage Life (HTSL) | JESD22 A103 | $T_A \geq$ 150°C | 3 Lots | 231 | 1000hrs | 0/231 | |
| Temperature-HumidityBias (THB) | JESD22 A101 | THB, 85°C, 85% RH Vcc max | 3 Lots | 231 | 1000hrs | 0/231 | 1 |
| Unbiased HAST (UHAST) | JESD22 A118 | 130 °C / 85% RH | 3 Lots | 231 | 96hrs | 0/231 | 1 |
| Temperature Cycling (TC) | JESD22 A104 | G -40°C to +125°C | 3 Lots | 231 | 850cycles | 0/231 | 1 |

Table 2. Assembly integrity Tests

| Stress (Abbv.) | Ref. | Conditions | Requirements | | | Notes |
|---|---|---|---|---|---|---|
| | | | # Lot | SS | Pass Criteria (Fails / Tested) | |
| Solderability | J-STD-002 | >95% Lead coverage | 3 | 5 units / 60 terminations | 0/60 | |
| Solder Ball Shear | JESD22 B117 | Characterization (all balls for 10 units) | 3 | 5 units / All balls | 0/60 | |

Notes:

1. Preconditioning with soak per J-STD-020 at rated moisture sensitivity level prior to acceleration stress testing.

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